Direct measurement and analysis of total ionizing dose effect on 130 nm PD SOI SRAM cell static noise margin*

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In this work, the total ionizing dose (TID) effect on 130 nm partially depleted (PD) silicon-on-insulator (SOI) static random access memory (SRAM) cell stability is measured. The SRAM cell test structure allowing direct measurement of the static noise margin (SNM) is specifically designed and irradiated by gamma-ray. Both data sides' SNM of 130 nm PD SOI SRAM cell are decreased by TID, which is different from the conclusion obtained in old generation devices that one data side's SNM is decreased and the other data side's SNM is increased. Moreover, measurement of SNM under different supply voltages (V_{dd}) reveals that SNM is more sensitive to TID under lower V_{dd}. The impact of TID on SNM under data retention V_{dd} should be tested, because V_{dd} of SRAM cell under data retention mode is lower than normal V_{dd}. The mechanism under the above results is analyzed by measurement of *I*–*V* characteristics of SRAM cell transistors.

Keywords: silicon-on-insulator, total ionizing dose, static random access memory, static noise margin

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1. Introduction

The stability of the cell is very important for static random access memory (SRAM) cell design, determining the soft-error rate and the sensitivity of memory to process tolerances and operating conditions.[1] The static noise margin (SNM) of a cell is a measure of its stability. It can be extracted by nesting the largest possible square in the two voltage transfer curves (VTC) of the involved complementary metal-oxide-semiconductor (CMOS) inverters, as shown in Fig. 1. The total ionizing dose (TID) effect can affect the stability of the SRAM cell, because it primarily increases leakage and induces threshold shift in the transistor and SNM is determined by electrical characteristics of SRAM cell transistors.[2] Therefore, the stability of SRAM cell used in space should depend on TID that it receives in space.

The impact of TID on the stability of SRAM cell has been investigated for several decades.[3–13] TID will result in a preferred state and non-preferred state in SRAM cell. That is, SNM of data applied on cell during TID exposure is increased, whereas SNM of TID complement data is decreased. In general, SNM of SRAM before and after TID irradiation is determined by circuit simulation with the irradiated transistor model.[6,9–13] Simulation results are experimentally verified by single event upset (SEU) characterization[3,5–8] or background data[4,11] testing indirectly, according to the relationship between SNM and SEU cross section, and background data distribution. TID induced asymmetry in SRAM cell stability is experimentally verified by unbalanced SEU cross section for TID data and TID complement data, and TID pattern imprinting in background data. However, there are few studies on direct measurement of SNM changing with TID to verify the accuracy of the simulation result. The exact value of SNM changing with TID cannot be extracted from the SEU cross section and background data test results, which is important to calibrate the simulation result.

In this paper, the TID effect on 130 nm PD SOI SRAM cell was studied experimentally by the cell test structure allowing direct measurement of SNM. Moreover, supply voltages (V_{dd}) dependence was explored by measurement of SNM changing with TID under different V_{dd}, because V_{dd} of SRAM cell is lower than normal voltage during the data retention mode. The mechanism under TID effect on 130 nm PD SOI SRAM cell stability was analyzed by measurement of *I*–*V* characteristics of cell transistors.

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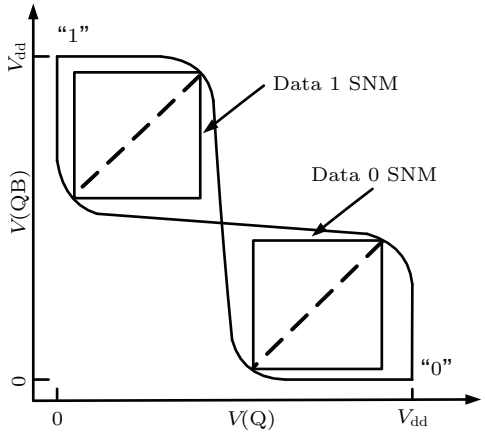


Fig. 1. The definition for SNM of SRAM cell.

2. Device and test strategy

The SRAM cell test structure was fabricated by a commercial 130 nm PD SOI process. In order to test SNM, seven terminals (BL, BLB, Q, QB, Vdd, Gnd, and WL) of a typical 6-T cell were wire-bonded to package, and definition of terminals is shown in Fig. 2. Radiation bias of cell was the standby operation (BL, BLB, Vdd, and QB were tied to 1.5 V, and Q, WL, and Gnd were tied to 0 V). Data 1 was written into the SRAM cell before TID irradiation. In our paper, Data 1 of the SRAM cell is defined as $V(\mathrm{Q}) = 0$ V and $V(\mathrm{QB}) = 1.5$ V. Oppositely, Data 0 is defined as $V(\mathrm{Q}) = 1.5$ V and $V(\mathrm{QB}) = 0$ V. SNM of the SRAM cell was determined by measuring VTC of the left hand inverter (constituted by Q1 and Q3) and the right hand inverter (constituted by Q2 and Q4). VTC of the left (right) hand inverter is measured by applying sweep voltage on Q (QB) and monitoring the voltage of QB (Q). As the state is in standby operation, Vdd, BL, and BLB terminals are tied to 1.5 V, and Gnd and WL terminals are tied to 0 V during SNM measurement. In order to analyze the mechanism under TID effect on SNM, SRAM cell transistors were fabricated in the same wafer as the cell, and packaged independently. SRAM cell transistors are T-gate body touch devices. The bias conditions of cell transistors were ON and OFF depending on the state of them in the cell during

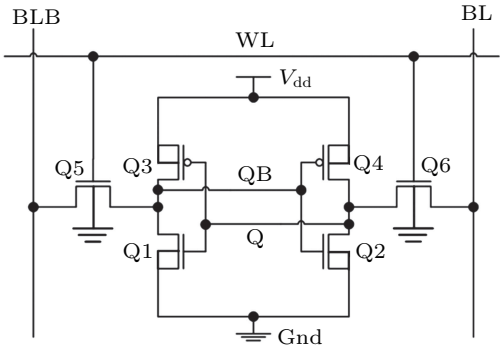


Fig. 2. Schematics of 6-T SRAM cell.

TID irradiation. Drain current (I_{ds}) versus gate to source voltage (V_{gs}) characteristics of the transistors were measured by a Keithley 4200 parameter analyzer at room temperature. TID exposures were carried out with 60Co gamma-ray in The Xinjiang Technical Institute of Physics and Chemistry, Chinese Academy Sciences, with a dose rate of 100 rad(Si)/s.

3. Experimental results

The SNM of the SRAM cell is determined experimentally by measuring VTCs of the left hand and right hand inverters, as shown in Fig. 3. Because SNM of a SRAM cell is defined as the side length of the square with the longest diagonal in closed regions of Fig. 3(a), it is determined in a 45° rotated coordinate system (see Fig. 3(b)). The left y axis of Fig. 3(b) represents VTC of inverters rotated 45° with respect to the Fig. 3(a) coordinate system, and the right y axis represents the difference between VTC rotated 45°. The maximum values of the right y axis in x axis intervals $[-1, 0]$ and $[0, 1]$ divided by $\sqrt{2}$ are Data 1 and Data 0 SNM. Seen from Fig. 3(b), both data sides' SNM are decreased by TID, which is different from the conclusion obtained in the old generation of devices that one data side's SNM is decreased and the other data side's SNM is increased.[3–8]

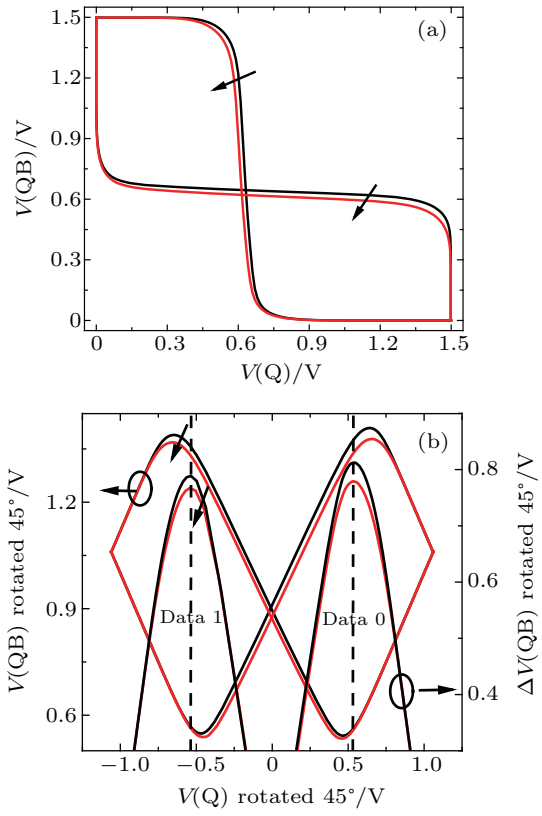


Fig. 3. (color online) The tested SNM of SRAM cell pre and post TID. The black line represents data of pre irradiation and the red line represents data post 500 krad(Si). (a) Butterfly curves pre and post 500 krad(Si). (b) SNM estimation based on maximum squares in a 45° rotated coordinate system relative to panel (a).

Figure 4 shows the extracted ΔSNM from butterfly curves as a function of TID levels, which reveals that radiation has a larger effect on Data 0 than Data 1. As discussed in Sec. 1, TID results in a preferred state and non-preferred state in the SRAM cell.

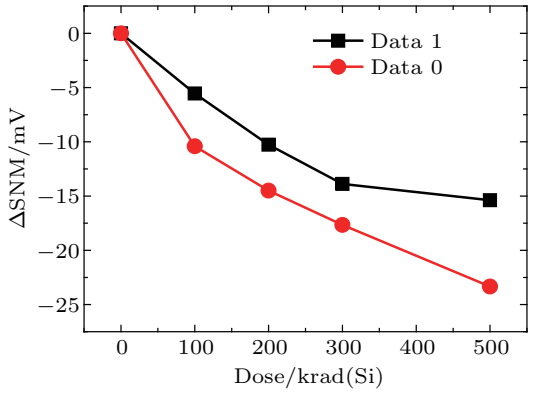


Fig. 4. (color online) The extracted ΔSNM from butterfly curves as a function of TID levels.

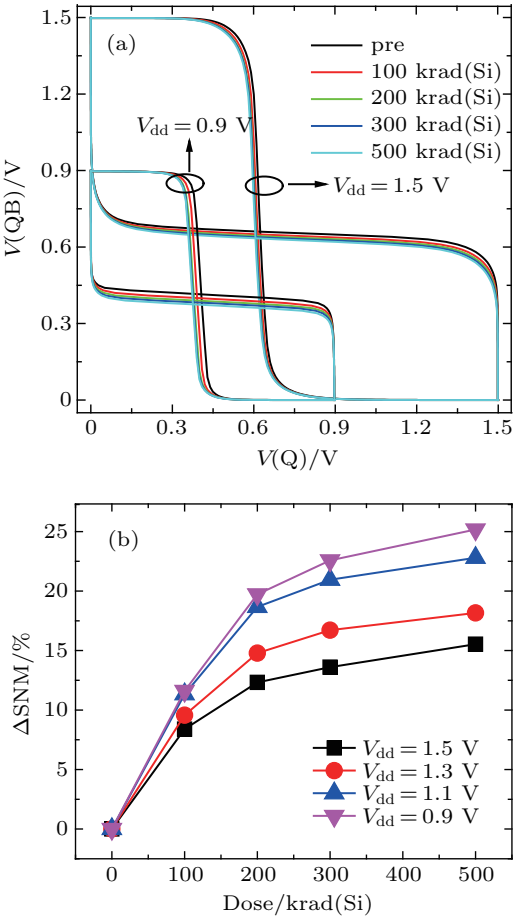


Fig. 5. (color online) The tested SNM of SRAM cell pre and post TID under different V_{dd}. (a) Butterfly curves pre and post 500 krad(Si). The black line represents data of pre irradiation and the red line represents data post 500 krad(Si). (b) The extracted SNM change percentage as a function of TID levels under different V_{dd}.

V_{dd} dependence for the TID effect on SNM is shown in Fig. 5. Seen from Fig. 5(a), SNM under lower V_{dd} is more sensitive to TID, as TID induced VTC negative shift is larger than higher V_{dd}. Figure 5(b) shows the extracted SNM change percentage as a function of TID levels under four different V_{dd}, indicating that TID effect on SNM is increased as V_{dd} drops.

4. Discussion

The mechanism of the TID effect on SNM is analyzed by measurement of I_{ds}–V_{gs} curves of SRAM cell transistors. Figure 6 shows the influence of TID on I_{ds}–V_{gs} curves of SRAM cell transistors. Except edge leakage, the threshold of 130 nm PD SOI n metal-oxide-semiconductor field effect transistor (NMOSFET) with ultra-thin gate oxide is negatively shifted by TID (easier to turn ON, see Fig. 6(a)), but the mechanism is different from old generation devices with thick gate oxide. The threshold shift of 130 nm PD SOI NMOSFET is caused by radiation induced charges trapped in shallow trench isolation (STI) rather than in gate oxide for old generation devices. The minimum or nearly minimum-geometry transistors are commonly used in SRAM cells. The influence of TID induced charge trapped in STI on the electric potential of the body region cannot be ignored in minimum-geometry transistors. Therefore, the threshold of SRAM cell transistors will be impacted, known as the radiation induced narrow channel effect (RINCE).[14,15] Seen from Fig. 6(a), TID induced drain current increase in NMOSFET can be divided into three regions. The drain current increase in Region I is caused by TID induced edge leakage. Edge leakage in narrow width NMOSFET is less affected by gate voltage, because it is brought about by TID induced charges trapped in the bottom of STI where the electric field applied by the gate voltage is very weak. In region III, the drain current increase is mainly caused by negative threshold shift, because the edge leakage is too small compared to the pre drain current. Region II is both affected by edge leakage and negative threshold shift. Known from Fig. 6(b), the threshold of the pull-up p metal-oxide-semiconductor field effect transistor (PMOSFET) is positively shifted by RINCE (harder to turn ON).

Known from Fig. 3, VTC negative direction shifts for left hand and right hand inverters result in a decrease of SNM. We find that VTC negative shift is closely related to drain current increase of pull-down NMOSFET at region V_{gs} from 0.3 V to 0.9 V. TID effect on SNM and I_{ds}–V_{gs} curves of pull-down NMOSFET are shown in Fig. 7. As discussed above, drain current increase of pull-down NMOSFET at region V_{gs} from 0.3 V to 0.9 V is caused by TID induced negative threshold shift. The switch point (V_M) of VTC is determined by the threshold of pull-up PMOSFET and pull-down NMOSFET, as

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{dd} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1+r},$$

$$r = \frac{W_{\rm P}}{W_{\rm N}}, \tag{1}$$

where $V_{\rm Tn(p)}$, $V_{\rm DSATn(p)}$, and $V_{\rm n(p)}$ are threshold voltage, saturation drain voltage, and width of pull-down (up) NMOSFET (PMOSFET), respectively.[16] The switch point of VTC will be negatively shifted by TID induced negative threshold shift in pull-down NMOSFET. Moreover, TID induced positive threshold shift in pull-up PMOSFET also makes the VTC have negative direction shifts, depending on the relationship between the switch point of the VTC and the transistor threshold.

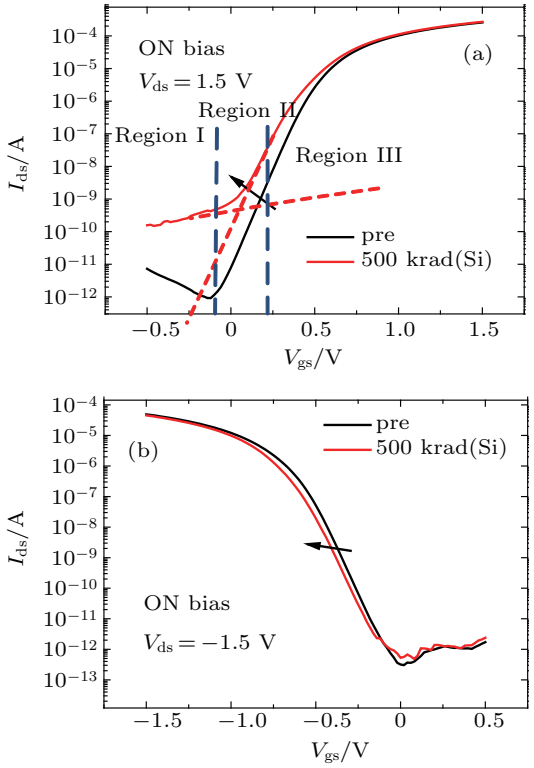


Fig. 6. (color online) TID effect on $I_{\rm ds}$–$V_{\rm gs}$ curves of SRAM cell transistors. (a) $I_{\rm ds}$–$V_{\rm gs}$ curves of pull-down NMOSFET pre and post 500 krad(Si) of irradiation under ON bias. (b) $I_{\rm ds}$–$V_{\rm gs}$ curves of pull-up PMOSFET pre and post 500 krad(Si) of irradiation under ON bias.

TID induced edge leakage in pull-down NMOSFET has a negligible influence on SNM. As shown in Fig. 7, the high output voltage of the inverter almost has no change before and after TID. In spite of the resistance of off-state NMOSFET being decreased by TID induced edge leakage, it is still much larger than on-state pull-up PMOSFET due to its strong drive ability. The on-state current of pull-up PMOSFET is 1.06×10^{-5} A, and off-state leakage of pull-down NMOSFET is increased to 7.96×10^{-10} A after 500 krad (Si). As a result, the off-state leakage of NMOSFET is compensated by pull-up PMOSFET and only lower down a tiny output voltage.

Because BL and BLB are tied to 1.5 V, pass gate NMOSFETs (Q5 and Q6) are connected in parallel to pull-up PMOSFET. The low output voltage of the inverter will be pulled up by the TID induced edge leakage in pass gate NMOSFET. However, TID induced edge leakage in pass gate NMOSFETs is not large enough to induce an obvious output voltage rising, since pass gate NMOSFETs biases OFF or TG during irradiation, as shown in Fig. 8.

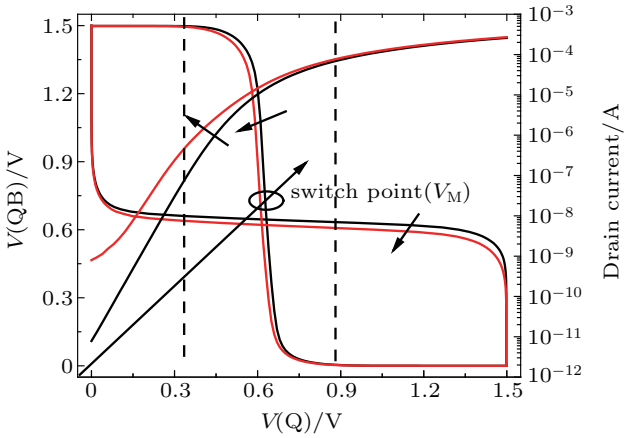


Fig. 7. (color online) SNM (left y axis) and $I_{\rm ds}$–$V_{\rm gs}$ curves of pull-down NMOSFET (right y axis) pre and post 500 krad(Si) TID irradiation.

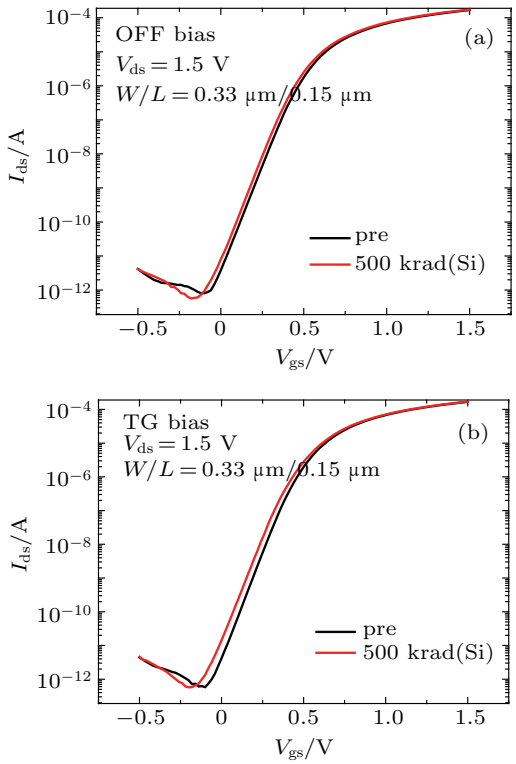


Fig. 8. (color online) TID effect on $I_{\rm ds}$–$V_{\rm gs}$ curves of pass gate NMOSFETs. (a) OFF bias. (b) TG bias.

TID induced asymmetry in SNM of 130 nm PD SOI SRAM cell is due to bias dependence of TID induced threshold shift in cell transistors. As shown in Fig. 9, TID induced threshold shift is bias dependent and the effect of radiation is larger at ON bias both for NMOSFET and PMOSFET. Above bias dependence indicates that the change of right hand inverter VTC is mainly caused by NMOSFET Q2 (see Fig. 2),

because it biases ON during TID irradiation. Accordingly, left hand inverter VTC shift is mainly caused by PMOSFET Q3 (see Fig. 2). The left hand inverter VTC negative shift is larger than the right hand inverter, leading to a larger decrease in Data 0 SNM, since radiation induced threshold shift in NMOSFET is larger than PMOSFET, as well as r in Eq. (1) is lower than 1 indicating that NMOSFET has a larger effect on $V_{\rm M}$ than PMOSFET when their threshold shift is the same.

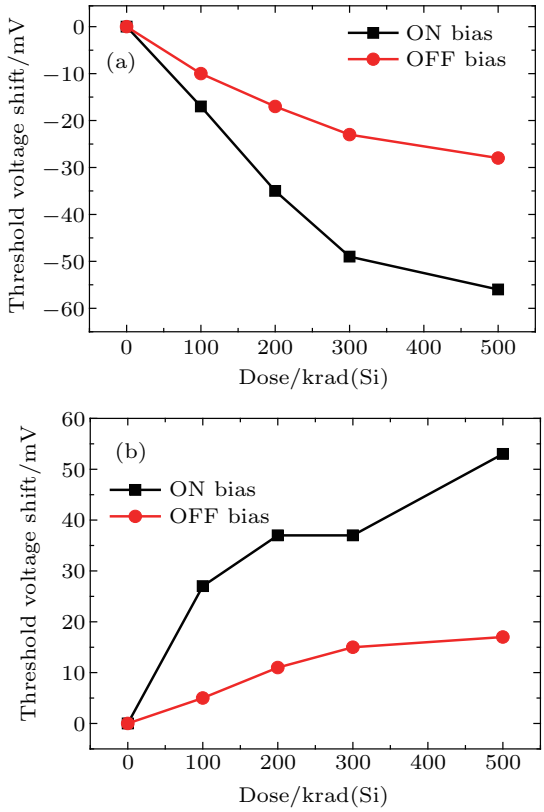


Fig. 9. (color online) Bias dependence of TID induced threshold shift in SRAM cell transistors. (a) Pull-down NMOSFETs. (b) Pull-up PMOSFETs.

Both data sides' SNM of 130 nm PD SOI SRAM cell are decreased, which is different from the conclusion obtained in old generation devices that one data side's SNM is decreased and the other data side's SNM is increased. The different bias dependence of TID induced threshold shift in PMOSFET is responsible for the above complicating conclusions. The threshold shift of OFF bias PMOSFET is larger than ON bias for the old generation device.[17] On the contrary, the effect of radiation is larger at ON bias for 130 nm PD SOI PMOSFET. Because NMOSFET and PMOSFET of old generation devices have a larger threshold shift in one side inverter of the SRAM cell, the VTC shift of one side inverter is much larger than the other side inverter. The VTC shift of the inverter with larger threshold shift plays a major role in SNM of SRAM cell, resulting in one increased SNM data side and the other decreased SNM data side, as shown in Fig. 10. But for the 130 nm PD SOI device in this paper, NMOSFET with larger threshold shift is in another inverter from PMOSFET with larger threshold shift. Therefore, VTC shifts of both inverters are near and SNM of both data sides are decreased. The opposite bias dependence of TID induced threshold in old generation PMOSFET and 130 nm PD SOI PMOSFET can be explained by the electric field direction in oxide. For old generation PMOSFET, radiation induced charges are pushed to the upper interface of the gate oxide under ON bias, having less effect on the threshold than the bottom interface. While radiation induced charges in 130 nm PD SOI PMOSFET are pushed to the upper region of STI under ON bias, and only charges trapped in the upper region of STI have an effect on the threshold, so that the threshold shift of 130 nm PD SOI PMOSFET under ON bias is larger than OFF bias.

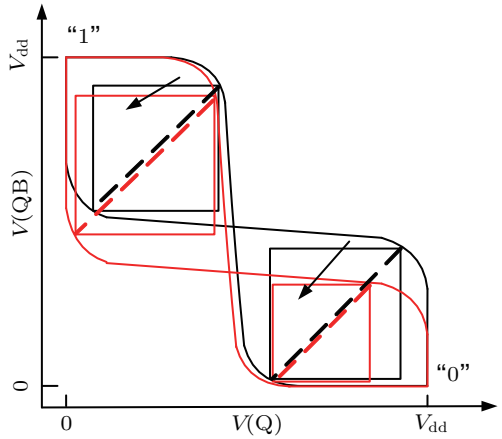


Fig. 10. (color online) Schematic of TID effect on SNM of old generation SRAM. The black line represents VTC of pre irradiation and the red line represents VTC post irradiation.

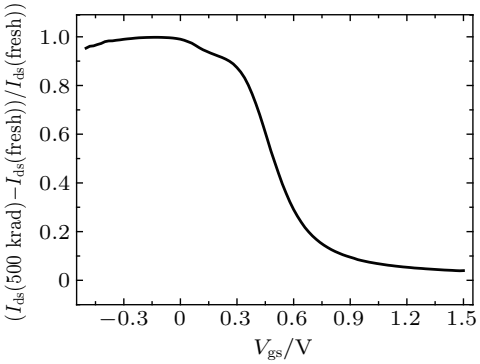


Fig. 11. TID induced drain current increase in pull-down NMOSFET relative to fresh value changing with gate voltage.

Figure 11 shows TID induced drain current increase in pull-down NMOSFET relative to fresh value, which reveals that drain current under lower gate voltage is more sensitive to TID. Moreover, the V(Q) and V(QB) region of VTC ($V_{\rm dd} = 0.9$ V) affected by TID is from 0.2 V to 0.5 V (see Fig. 5(a)), which is lower than VTC ($V_{\rm dd} = 1.5$ V). Therefore, TID induced SNM change under lower $V_{\rm dd}$ is larger than that under high $V_{\rm dd}$.

5. Conclusion

TID effect on 130 nm PD SOI SRAM cell stability is experimentally explored in this work. The SNM of the SRAM cell is directly measured by the test structure specifically designed for SNM testing. Experimental results show that both data sides' SNM are decreased due to the negative shift of VTC induced by TID, and TID has a larger effect on SNM of TID complement data. Moreover, V_{dd} dependence was explored by measurement of SNM under different supply voltages changing with TID, and experimental result reveals that SNM under lower V_{dd} is more sensitive to TID. The mechanism of the TID effect on SNM is analyzed by measurement of I_{ds}–V_{gs} curves of cell transistors. The threshold shift of cell transistors caused by RINCE is responsible for the decreased SNM. Because NMOSFET and PMOSFET have larger threshold shift in different inverters, both data sides' SNM are decreased by TID rather than that one data side's SNM being decreased and the other data side's SNM being increased in old generation devices. SNM is more sensitive to TID under lower V_{dd}, since SNM under lower V_{dd} is affected by the lower V_{gs} region of I_{ds}–V_{gs} curves of NMOSFET, and TID has a larger impact on the lower V_{gs} region of I_{ds}–V_{gs} curves.

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