Horizontal InAs nanowire transistors grown on patterned silicon-on-insulator substrate*

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High-density horizontal InAs nanowire transistors are fabricated on the interdigital silicon-on-insulator substrate. Hexagonal InAs nanowires are uniformly grown between face-to-face (111) vertical sidewalls of neighboring Si fingers by metal–organic chemical vapor deposition. The density of InAs nanowires is high up to 32 per group of silicon fingers, namely an average of 4 nanowires per micrometer. The electrical characteristics with a higher on/off current ratio of 2×10^5 are obtained at room temperature. The silicon-based horizontal InAs nanowire transistors are very promising for future high-performance circuits.

Keywords: InAs nanowires, Si substrate, interdigital structure, MOSFET

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1. Introduction

III–V materials have drawn a great deal of attention for their higher carrier mobility and better optoelectronic characteristics. Unlike Si, bulk III–V materials are quite expensive and brittle. Hence, the integration of III–V material with Si possesses the advantages of both materials. However, lattice-mismatch and thermal-mismatch of the III–V planar layer on Si substrate induced by traditional heterostructure will dramatically worsen the device characteristics.[1] It is noteworthy that epitaxial III–V nanowires without defects on Si substrate can be grown more readily than the two-dimensional III–V layer growth.[2]

Many relevant published reports have proved the feasibility of III–V nanowires grown on Si substrate.[3] Si-based III–V nanowire transistors based on the as-grown vertical nanowires, such as tunneling junction[4] and heterostructure pillar,[5] were realized, but these vertical transistors need an additional process to form drain and source contacts. Thus the process of vertical transistors may be more complex. Meanwhile, the horizontal epitaxy of III–V nanowires on Si substrate by metal catalyst or templates has also been reported.[6,7] However, non-uniform direction and lower density are still critical issues for the horizontal nanowire devices.

In this paper, a novel method is introduced to fabricate horizontal InAs nanowire transistors on interdigital silicon-on-insulator (SOI) substrate. High-density hexagonal InAs nanowires are uniformly grown by metal–organic chemical vapor deposition (MOCVD) without the assistance of the metal-catalyst or template on SOI substrate. Room-temperature electrical characteristics of the Si-based horizontal InAs nanowire transistors (NWTs) reveal the potential as the next generation of nanoelectronic devices.

2. Device fabrication

We used (110)-oriented SOI substrate with an 88-nm-thick top Si layer. First, a 20-nm-thick SiO_2 layer was formed by dry oxidation at 900 °C for 40 min. The SiO_2 layer acted as a mask in the wet etch, the buffer layer of the doping and isolation layer of the InAs growth. The SOI substrate was heavily implanted by phosphorous ion with a dose of 5×10^{13} cm^{-2}, which corresponded to a doping concentration of 4×10^{18} cm^{-3}. The dumbbell-like isolation was formed by ultraviolet lithography. The exposed part was totally removed and the buried oxide of SOI substrate emerged (Fig. 1(b)). The patterned SOI substrate with interdigital structure was made by electron beam lithography (EBL), inductively coupled plasma (ICP), and wet etching, as shown in Fig. 1(c). The Si fingers with a width of around 350 nm in the interdig-

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ital structure were attached to the source and the drain mesas to increase the growth area of InAs nanowires. The space between Si fingers was designed as 200 nm for growing the InAs nanowires. As shown by the chart in Fig. 1(d), InAs nanowires were grown by selective-area metal–organic chemical vapor deposition (SA-MOCVD).

With a trimethylindium flow rate of 0.8×10^{-6} mol/min and an AsH_3 flow rate of 2.0×10^{-4} mol/min, the InAs nanowires began to synthesize and grow at 565 °C for 100 s, and the corresponding V/III ratio was about 250. Additionally, dislocation in the hetero-interface between Si and InAs nanowire is reduced[8] based on the nanowire structure. After the epitaxy, the substrate was dipped in dilute hydrofluoric acid (HF) solution (5% in volume) for a few seconds to eliminate nature oxides attached to the InAs nanowire, and the top SiO_2 layer was also removed (Fig. 1(e)). The sample was covered with 15-nm-thick Al_2O_3 by means of atomic layer deposition (ALD) at 300 °C immediately. Next, Ni/Al layers were deposited orderly by electron beam evaporation in the contact windows of source and drain regions, and the ohmic contact was formed by the following rapid annealing at 500 °C for 2 min in N_2 atmosphere. Finally, Ti/Al layers were defined to cover the Al_2O_3-wrapped InAs nanowires via electron beam evaporation, as well as the Si interdigital structure unintentionally. The critical steps are illustrated in Fig. 1.

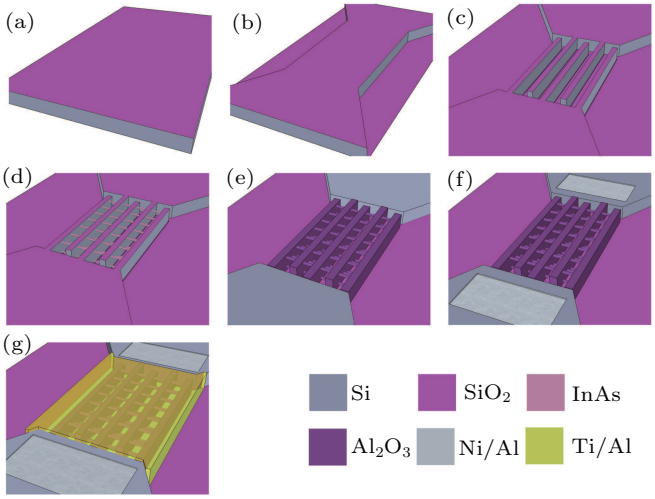


Fig. 1. (color online) Schematics illustrating the fabrication process flow. (a) Dry oxidation and ion implantation. (b) Formation of dumbbell-like isolation. (c) Defining the interdigital structure on the top Si layer. (d) Epitaxy of horizontal InAs nanowires by MOCVD. (e) Deposition of Al_2O_3 gate dielectrcs on InAs nanowires. (f) Metal doposition and ohmic contact for S/D. (g) Gate electrode doposition.

3. Results and discussion

High-density horizontal InAs nanowires are obtained, which are uniform epitaxy between face-to-face (111) vertical sidewalls of adjacent Si fingers. It has been reported in an earlier reference[9] that III–V nanowires were horizontally grown in random directions between vertical sidewalls on a planar Si substrate. The majority of InAs nanowires are vertical to the Si (111) sidewalls in this experiment, which is similar to the result in a previous report.[10] It is assumed that indium atoms nucleate more easily than arsenide atoms on the (111) facet, and Si ⟨111⟩ tends to the growth orientation when the V/III ratio is higher. In the case of arsenide enrichment, InAs nanowires grow fast in Si ⟨111⟩ direction for the competition of arsenide atoms between the top indium droplet and Si sidewall. Radial growth, in turn, can take place under the As-limited condition.[11]

The formation of smooth Si sidewalls is the most critical step since InAs nanowires here grow vertically on Si (111) facet. In the case of a rough surface, inclined InAs nanowires will be grown on the Si sidewalls due to the appearance of facets other than (111). Here, the adjacent Si fingers are treated as one group, and the InAs nanowire quantity of each group has been counted. Within the finger length of 8 μm, the number of InAs nanowires is up to 32 in each group, namely 4 nanowires μm^{-1} averagely. It is assumed that the interdigital structure decelerates the flow of precursors, and the atomic groups could absorb, nucleate and grow spontaneously on a large-area surface of the (111) facet.

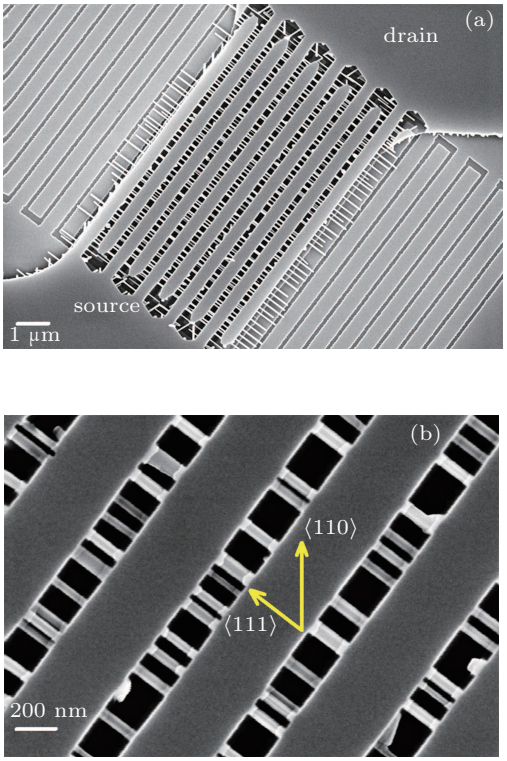


Fig. 2. (color online) SEM images of the InAs nanowires grown between two Si sidewalls. (a) Top view of interdigital structure and horizontal InAs nanowires. (b) Nanowires uniform in the ⟨111⟩ direction and the orientation of the top silicon layer vertical to the nanowires.

Around 300 InAs nanowires can be obtained in the device. The average diameter and length are about 60 nm and 200 nm respectively. The sizes of InAs nanowires basically depend on the height and spacing of Si sidewalls, although the nanowire diameter varies from 40 nm to 100 nm with

the size of self-organizing indium droplet at the beginning and the radial growth at the end. The hexagonal morphology of InAs nanowire as shown in Fig. 2(b) accords well with the crystal lattice of the Si (111) facet. Moreover, the natural InAs nanowire length without restraint is around 1 μm as the longer nanowires grow on the outmost Si fingers shown in Fig. 2(a). In addition, fabricated horizontal InAs NWT is shown in Fig. 3. The pink part is covered with native oxide. The interdigital structure is wrapped with gate electrode. It is worth noting that the tilted transistor results from the angle between ⟨111⟩ of the InAs nanowire and ⟨001⟩ of the SOI sample.

The electrical characteristics at room temperature are measured by an Agilent B1500 semiconductor parameter analyzer. Output characteristics of the InAs NWT are shown in Fig. 4(a). Obviously, nonlinear behaviors are not observed at the initial stage of drain–source voltage (V_{DS}). There should exist a barrier at the InAs-Si hetero-interface according to the Poisson equation, which may induce a turn-on voltage in the output curve. However, Fermi energy level (E_F) is shifted up to the conduction band edge (E_C) due to the n-type heavy doping of Si fingers, which reduces the potential barrier at the hetero-interface. Electrons overcome the barrier easily in this condition. The higher resistances of Si fingers (denoted as R_D and R_S in Fig. 4(c)) and complete depletion of InAs nanowires jointly cause the off state. The resistance is about 250 kΩ at $V_{GS} = 4$ V according to the output characteristics. The parallel InAs nanowire array reduces the resistance while the channels emerge as displayed in Fig. 4(d), and R_O represents the total resistance of InAs nanowires. The transistor then enters into a saturation regime (as shown by the equivalent current source I_D in Fig. 4(e)) at $V_{DS} = 2$ V when V_{GS} is kept at 4 V, which means lower power consumption.

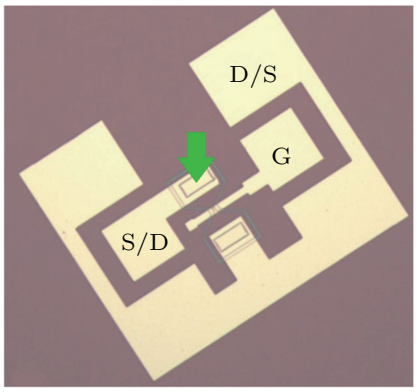


Fig. 3. (color online) Fabricated Si-based horizontal InAs NWT under optical microscope. Drain, source, and gate electrodes are marked separately. The green arrow points to the contact window of S/D.

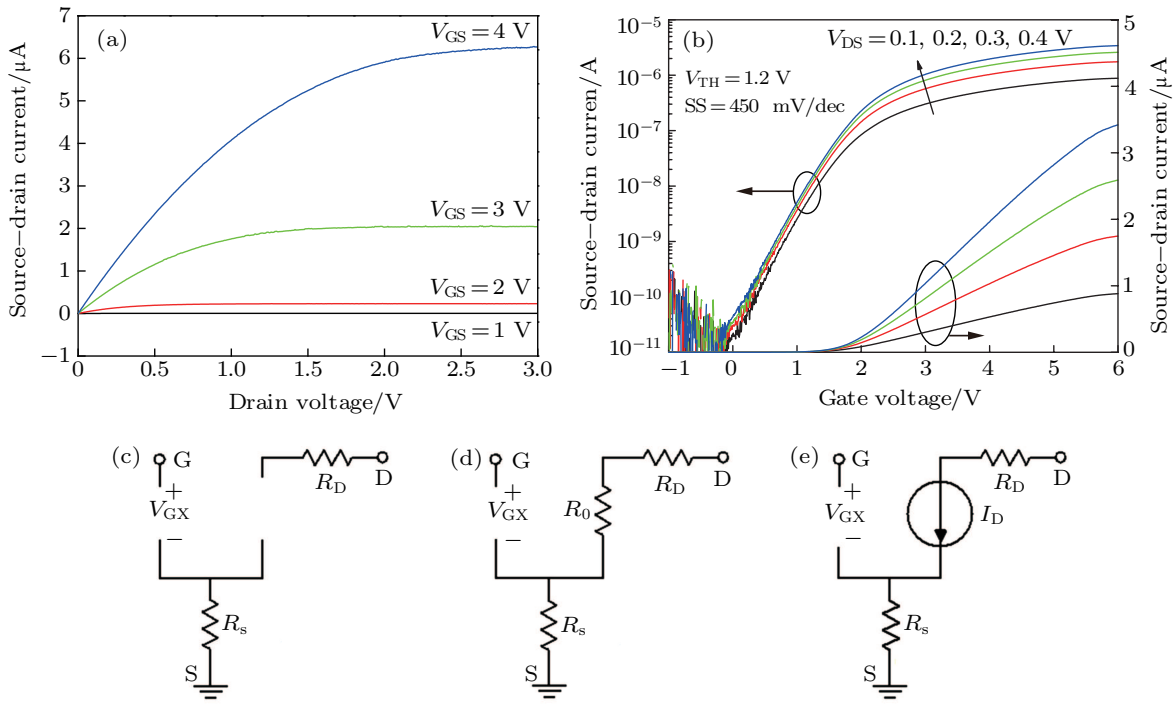


Fig. 4. (color online) Room-temperature electrical performances. (a) Output curves with V_{GS} set varying from 1 V to 4 V, and the voltage spacing is 1 V. (b) Transfer characteristic with V_{GS} at 0.1, 0.2, 0.3, and 0.4 V, respectively. (c)–(e) Equivalent large signal circuit models of the transistor presenting orderly corresponding operation states: off regime, Ohmic regime, and saturation regime.

Room-temperature threshold voltage (V_{TH}) of the transistor is about 1.2 V, which indicates an n-type enhancement mode. The subthreshold swing (SS) of 450 mV/dec implies much lower series capacitance due to a small dielectric constant of gate insulator and dense density of interface states (D_{it}) at the InAs–Al_2O_3 interface. Despite the surface treatment, the D_{it} still acts as the charge center and attracts massive negative charges to form parasitic capacitance. The D_{it} here is estimated to be about 2.2×10^{13} $eV^{-1}\cdot cm^{-2}$ at room temperature from the improved formula

$$SS = \frac{k_B \cdot T}{q} \cdot \ln 10 \cdot \left(1 + \frac{q^2 \cdot D_{it}}{C_{ox}}\right)$$

based on Ref. [12], where k_B is the Boltzmann constant (1.38×10^{-23} J/K), C_{ox} is the gate capacitance per unit area (5.3×10^{-7} F/cm^2), and q is the electron charge (1.6×10^{-19} C). The co-action of small gate capacitance and parasitic capacitance leads to a lower series capacitance. Additionally, a higher on-off ratio (I_{ON}/I_{OFF}) of 2×10^5 is achieved, which shows the ability to control static consumption. Besides, the variation of V_{TH} with ambient temperature is illustrated in Fig. 5. The temperature coefficient of about -3 mV/K demonstrates preferable stability of V_{TH} in a larger temperature range.

As illustrated in Table 1, the common fabrication approach in the listed references is the combination of bottom-up and transfer technology, which indeed enhances the process complexity remarkably. Hence the superiority of this experiment is the compatibility with the planar process, and also the simplification. The average nanowire diameter obtained by this method is about 60 nm, which is not inferior to the vertical nanowires based on bottom-up technology. Compared with the negative V_{TH} presented in Refs. [15] and [16], etc., positive V_{TH} of the horizontal InAs NWT is achieved in this experiment. Possessing a positive V_{TH} means that a transistor needs a constant negative gate voltage to switch off the state, and the static power consumption can increase remarkably. Besides, higher I_{ON}/I_{OFF} of 2×10^5 than those of other listed devices implies better gate-controlled capability and an excellent InAs-Si interface. To achieve higher performance, the Si-based horizontal InAs NWTs still need to promote with the following optimization despite the temporary disadvantages, such as dense D_{it}.

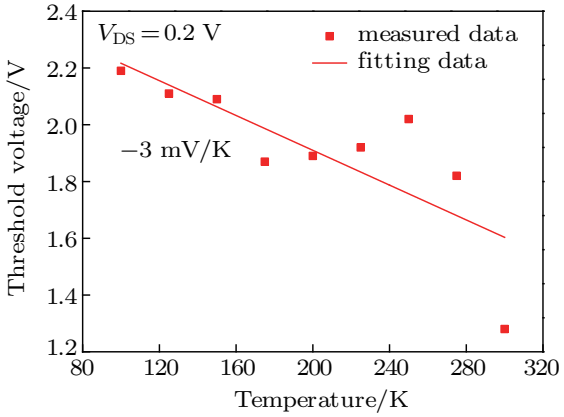


Fig. 5. (color online) Relationship between V_{TH} and temperature of InAs NWT. The dots are the measured data and the line represents fitting data. This measurement is conducted at $V_{DS} = 0.2$ V.

Table 1. Comparison among relevant parameters of various InAs-based nanowire devices at 300 K.

Reference	Approach/structure	Diameter/nm	V_{TH}/V	I_{ON}/I_{OFF}
This work	bottom-up/horizontal	60	1.2	10^5
Konar *et al.*[13]	bottom-up and transfer/horizontal	62	–0.55[a)]	–
Memišević *et al.*[14]	bottom-up and etching/vertical	25	~ -0.3[b)]	10^4
Li *et al.*[15]	bottom-up and transfer/horizontal	~ 20	~ -0.7[c)]	10^4
Burke *et al.*[16]	bottom-up and transfer/horizontal	~ 130	~ -0.5[d)]	10^4
Sasaki *et al.*[17]	bottom-up and transfer/horizontal	70	~ 0.4	$\sim 10^3$
Cutaia *et al.*[18]	top-down and bottom-up/vertical	~ 100	~ -0.1[e)]	10^6[f)]

[a)–e)]Negative threshold voltage will increase static power consumption.

[f)]This device is a p-type vertical tunneling field effect transistor. The higher I_{ON}/I_{OFF} results from the extremely low I_{OFF}.

4. Conclusions

By a catalyst-free growth approach, we acquire the horizontal InAs nanowire transistors on patterned SOI substrate with interdigital structure, in which high-density InAs nanowires bridging neighboring vertical Si (111) sidewalls are grown uniformly. Furthermore the novel approach may offer a prospective thought for obtaining the dense and uniform horizontal III–V nanowires with different lengths. Normal electrical characteristics of the transistors have proved the feasibility for future high-performance circuits. Moreover, the horizontal InAs nanowire transistors on SOI substrates shed light on the application of Si-based III–V integration circuits in massive production.

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