Improvement of the high-κ/Ge interface thermal stability using an *in-situ* ozone treatment characterized by conductive atomic force microscopy*

Ji-Bin Fan(樊继斌)[1,†], Xiao-Jiao Cheng(程晓姣)[1], Hong-Xia Liu(刘红侠)[2], Shu-Long Wang(王树龙)[2], and Li Duan(段理)[1]

[1] *School of Materials Science and Engineering, Chang'an University, Xi'an* 710061, *China*
[2] *School of Microelectronics, Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, Xidian University, Xi'an* 710071, *China*

(Received 6 March 2017; revised manuscript received 14 April 2017; published online 20 June 2017)

In this work, an *in-situ* ozone treatment is carried out to improve the interface thermal stability of HfO_2/Al_2O_3 gate stack on germanium (Ge) substrate. The micrometer scale level of HfO_2/Al_2O_3 gate stack on Ge is studied using conductive atomic force microscopy (AFM) with a conductive tip. The initial results indicate that comparing with a non *in-situ* ozone treated sample, the interface thermal stability of the sample with an *in-situ* ozone treatment can be substantially improved after annealing. As a result, void-free surface, low conductive spots, low leakage current density, and relative high breakdown voltage high-κ/Ge are obtained. A detailed analysis is performed to confirm the origins of the changes. All results indicate that *in-situ* ozone treatment is a promising method to improve the interface properties of Ge-based three-dimensional (3D) devices in future technology nodes.

Keywords: high-κ, conductive atomic force microscopy, *in-situ* ozone, annealing

PACS: 77.55.D–, 82.80.Pv **DOI:** 10.1088/1674-1056/26/8/087701

1. Introduction

Germanium (Ge) has recently been regarded as a promising channel material for metal–oxide–semiconductor field-effect transistor (MOSFET) due to its high hole and electron mobilities, which are 4.2 and 2.6 times higher than those of Si, respectively.[1–3] To obtain Ge MOSFET with superior electrical properties, it is essential to realize a high-κ/Ge gate stack with ultrathin equivalent oxide thickness (EOT) and good high-κ/Ge interface. However, direct deposition of high-κ dielectric on the Ge surface results in poor interface quality and high interface state density.[4,5] Moreover, due to Ge oxides inevitably forming at the high-κ/Ge interface, the formation and desorption of GeO at high-κ/Ge interface generate a huge number of defects and traps in the high-κ film in the deposition process or subsequent annealing treatment.[6,7] To cope with these challenges, various techniques such as GeO_xN_y passivation layer, stress-relieved pre-oxide method and plasma post oxidation (PPO) method have been proposed.[8–11] These techniques have been proven to work very well on planar devices. However, with the continuous development and popularization of three-dimensional (3D) devices (FinFET etc.), these techniques become challenging to controlling the non-planar interface. For example, application of the PPO method to 3D structures is challenging due to an anisotropic nature of plasma processing. Thus, new techniques to improve the high-κ/Ge interface are desirable to realize high performance 3D devices. Recently Ando *et al.* reported that an *in-situ* ozone treatment can improve the interface quality of SiGe FinFET due to the spatial diffusivity of the gas.[12] In addition, using *in-situ* cycling ozone treatment to improve the interface of Al_2O_3/GeO_x/Ge gate stack planar device has been investigated by Yang *et al.*[13] The good electrical behavior of high-κ material has been gained from measurements performed on macroscopic transistors using a standard electrical characterization method. However, the mechanism of this method to improve the high-κ/Ge interface is still unclear. Due to the fact that the conductive atomic force microscopy (CAFM) is able to characterize the gate dielectric on a nanometer/micrometer scale, showing properties to which the standard electrical characterization techniques are blind.[14,15] Therefore, in this paper, an *in-situ* ozone treatment is used to improve the interface quality of the high-κ/Ge structure deposited by atomic layer deposition (ALD). The mechanism of this method to improve the high-κ/Ge interface is investigated by conductive atomic force microscopy and x-ray photoelectron spectroscopy (XPS).

2. Experiment

Prior to the dielectric stack formation, p-type (100) Ge substrates with a resistivity of 0.1 Ω·cm∼1.0 Ω·cm were cleaned by acetone, de-ionized water, and dilute HF (hydroflu-

*Project supported by the National Natural Science Foundation of China (Grant No. 61604016), China Postdoctoral Science Foundation (Grant No. 2017M613028), and the Fundamental Research Funds for the Central Universities, China (Grant Nos. 310831161003 and CHD2017ZD142).

†Corresponding author. E-mail: jbfan@chd.edu.cn

© 2017 Chinese Physical Society and IOP Publishing Ltd

oric acid:de-ionized water = 1 : 500) aqueous solution etching to remove the native oxide. After a pre-clean, ~ 0.5-nm Al_2O_3 was deposited by ALD at 300 °C using TMA and H_2O as precursors, followed by an *in-situ* ozone treatment for 120 s at 300 °C. The gas flow of O_3 was 200 sccm, corresponding to the vapor pressure of 15 hPa. Then 4-nm HfO_2 was deposited by ALD at 300 °C using TEMAHf and H_2O as precursors. The sequence was performed continuously without breaking. HfO_2/Al_2O_3 gate stacks with *in-situ* ozone treatment were donated as sample A, and gate stacks without *in-situ* ozone treatment were donated as sample B. After that, the post deposition annealing (PDA) was performed for the HfO_2/Al_2O_3 gate stacks at 500 °C in N_2 ambient for 60 s, which was compatible to the source/drain formation activation annealing process. Then, the CAFM (Bruker Dimension Edge system) was used to study the electrical properties of gate stack dielectrics on a micrometer scale. A Pt-coated conductive tip of the CAFM on the bare high-κ dielectric was used as a gate electrode of an MOS structure. The XPS (Thermo Scientific K-alpha system) was used by adopting the monochromatic Al K_α source ($h\nu$ = 1486.7 eV) to investigate the origin change of the HfO_2/Al_2O_3 gate stack on Ge.

3. Results and discussion

Figure 1 shows the surface roughness of the HfO_2/Al_2O_3 gate stacks on Ge before and after annealing. Surface roughness of all films is extracted from the AFM images and expressed as the root mean square (RMS) value. As shown in Fig. 1, uniform surface morphology is observed for all the samples and nearly identical RMS value (~ 0.1 nm) is obtained except the annealed sample B. Furthermore, the RMS value of sample A decreases from 0.088 nm to 0.064 nm after annealing, whereas that of sample B increases from 0.102 nm to 0.211 nm after annealing. Commonly, the densification of the film results in the decrease of the RMS value. The increase of the RMS value suggests that the different changes occur in sample B after annealing. Moreover, after annealing, a large number of voids are observed in sample B. For the HfO_2/Al_2O_3 gate stacks on Ge substrate, the voids may be attributed to the volatilization of GeO during the annealing. Because the formation and desorption of GeO occur in a uniform or nonuniform model for the high-κ/Ge system, the volatilization of GeO results in the formation and growth of the voids.[16,17] The results suggest that the HfO_2/Al_2O_3 gate stacks on Ge with an *in-situ* ozone treatment can suppress the volatilization of GeO after annealing, which is of benefit to improving the interface thermal stability of HfO_2/Al_2O_3 gate stacks on Ge.

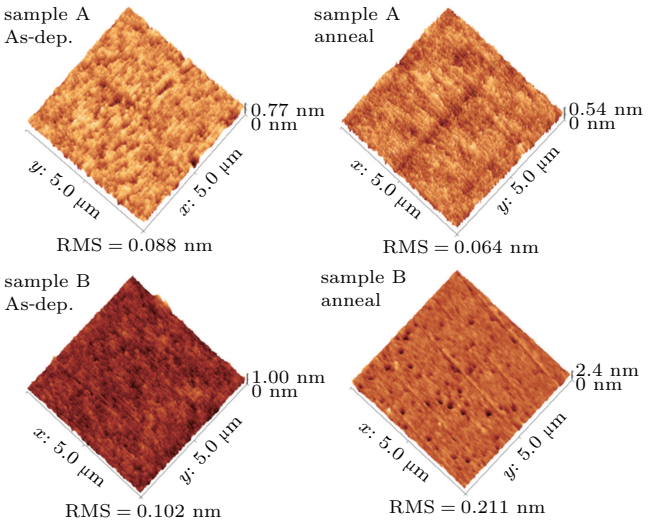


Fig. 1. (color online) AFM surface images of the HfO_2/Al_2O_3/Ge structure before and after annealing.

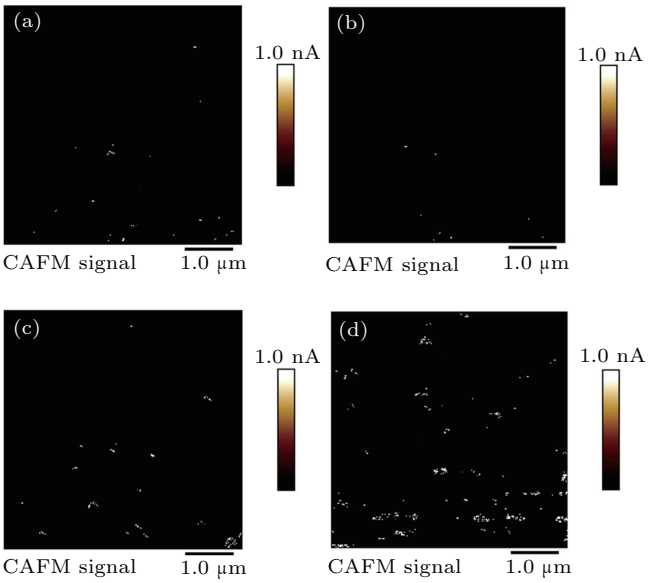


Fig. 2. (color online) CAFM images of sample A ((a) as-deposited and (b) annealed) and sample B ((c) as-deposited, (d) annealed).

Figure 2 shows the current images of the HfO_2/Al_2O_3 gate stacks on Ge substrate before and after annealing. Current images are measured by conductive AFM when applying a sample bias of 10 V. The current images will provide information about the spatial distribution of the HfO_2/Al_2O_3 gate stacks conductivity. As shown in Figs. 2(a) and 2(b), the density of leakage spots in as-deposited sample A decreases significantly after annealing. It can be explained by the fact that the impurity concentration and defects decrease due to the thermal annealing supplying enough thermal energy for the by-products residing and dangling bonds decomposition and re-composition, leading to the HfO_2/Al_2O_3 gate stack becoming a good gate dielectric insulator.[18,19] However, as shown in Figs. 2(c) and 2(d), the density of leakage spots in sample B increases significantly after annealing, which indicates that the

conductive paths increase significantly. This may be caused by the fact that the formation and desorption of GeO lead to the local fluctuations in composition and/or structures, and/or by defects in the HfO_2/Al_2O_3 gate stacks. It deteriorates the interface and high-κ film quality and leads to the gate leakage spots increasing obviously.

The conductions of the samples are analyzed in more detail through the *I*–*V* curves measured on fixed locations. Figure 3 shows the *I*–*V* curves measured by conductive AFM using a Pt-coated tip at room temperature. As shown in Fig. 3, the breakdown oxide voltage of 7.67 V for the as-deposited sample A is measured at the leakage current of 1 nA while that of the as-deposited sample B is 7.16 V. After an *in-situ* ozone treatment, the increase of the breakdown oxide voltage may be related to the increase of high Ge^{4+} density at the interface, and improve the interface quality due to the strong oxidation ability of ozone.[9] After the samples experience the thermal treatment, the breakdown oxide voltage of sample A increases to 8.19 and that of sample B decreases to 5.26 V. The results indicate that the *in-situ* ozone treatment improves the thermal stability of the high-κ/Ge interface due to the suppression of the GeO volatilization. As a result, the electrical characteristics of the HfO_2/Al_2O_3 gate stacks on Ge substrate are substantially improved after annealing.

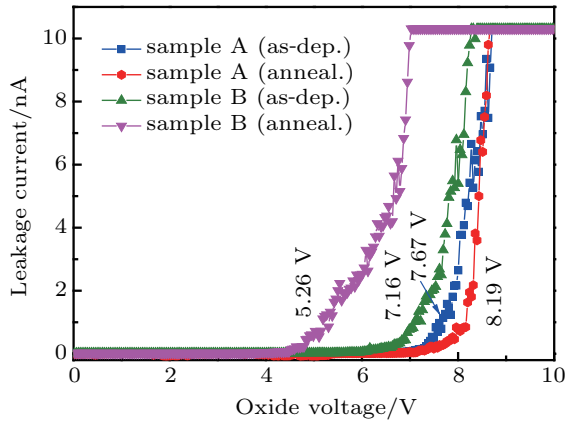


Fig. 3. (color online) *I*–*V* curves of the HfO_2/Al_2O_3 gate stacks on Ge substrate measured at the positions of conductive spots in CAFM images using a Pt-coated tip.

We analyze the forward *I*–*V* curves in terms of various conduction mechanisms to find that the data can be fitted best to the Frenkel–Poole (FP) mechanism.[20] The Frenkel–Poole mechanism refers to a conduction mediated by carrier-trap states, which gives the *J*–*E* relation as follows:[21]

$$J = AE \times \exp\left(-\frac{q\phi_t}{kT} + \frac{\sqrt{q^3 E_{b/\pi\varepsilon_0\varepsilon_s}}}{kT}\right), \tag{1}$$

where J is the current density, E the electric field over the energy barrier at the tip-semiconductor interface, q is the electron charge, k is the Boltzmann constant, ε and ε_s are the vacuum and relative dielectric permittivity of the semiconductor, respectively. T is the temperature, ϕ_t is the barrier height for electron emission from the trapped state, and C is a constant. The electric field dependency in the FP process can be linearized when plotting Eq. (1) as

$$\ln(J/E) = A(T) \times \sqrt{E} + B(T), \tag{2}$$

$$A(T) = \frac{\sqrt{q^3/\pi\varepsilon_0\varepsilon_s}}{kT}, \tag{3}$$

$$B(T) = -\frac{q\phi_t}{kT} + \ln(C), \tag{4}$$

where $A(T)$ and $B(T)$ are the slope and y-intercept, respectively. The measured *I*–*V* curves in Fig. 3 are plotted as $\ln(J/E) \sim E^{1/2}$ as shown in Fig. 4. The measured *I*–*V* dependence generally follows a trend of Eq. (2) although they fluctuate. The fitted linear lines in Fig. 4 suggest that the conduction through the oxide is consistent with the FP mechanism. The re-plotted data show that $A(T)$ and $B(T)$ are affected by the *in-situ* ozone treatment, especially after annealing, which are related to the barrier height ϕ_t for electron emission from the trapped state and the dielectric permittivity ε_s respectively.

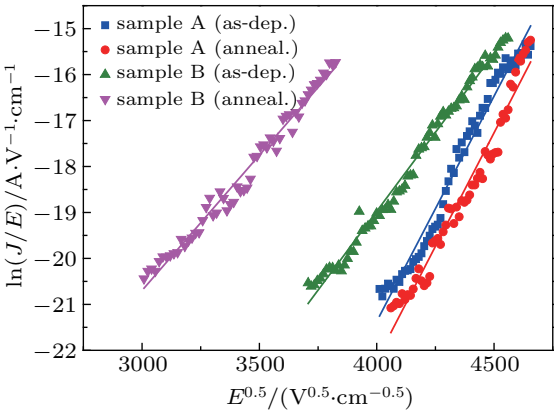


Fig. 4. (color online) $\ln(J/E) \sim E^{1/2}$ from the measured *I*–*V* curves in Fig 3.

To evaluate the variation of the barrier height ϕ_t and the dielectric permittivity ε_s for HfO_2/Al_2O_3 gate stacks on Ge substrate slope and y intercept values of the fit (solid) lines in Fig. 4 are shown in Fig. 5. According to Eq. (3), the dielectric constant of the HfO_2/Al_2O_3 gate stacks on Ge substrate can be qualitatively analyzed. For sample A, the slope of the HfO_2/Al_2O_3 gate stacks on Ge increases from 0.00881 to 0.00889 after annealing, which indicates that the dielectric constant of the high-κ gate stack decreases slightly after annealing. It may be caused by the growth of the interfacial layer with low dielectric constant after annealing. However, the slope value of sample B decreases from 0.00687 to 0.00589 after annealing, which indicates that the dielectric constant increases after annealing. This may be explained by the fact that

the thickness of the interfacial layer with low dielectric constant decreases due to the GeO volatilization, which leads to the total dielectric constant of $HfO_2/Al_2O_3/GeO_x$ gate stacks increasing after annealing. Moreover, the intercept value of sample A increases a little after annealing, whereas that of sample B decreases significantly after annealing. It is considered that the density of trap centers in sample A is higher than that in sample B when the trap barrier heights for both samples are assumed to be identical. Although sample B has larger dielectric constant values than sample A, the electrical charactersitics of the HfO_2/Al_2O_3 gate stack on Ge are totally deteriorated due to the GeO volatilization. The results indicate that an *in-situ* ozone treatment can improve the interface thermal stability of the HfO_2/Al_2O_3 gate stack on Ge, making it become a promising method to improve the interface properties of the Ge-based 3D devices.

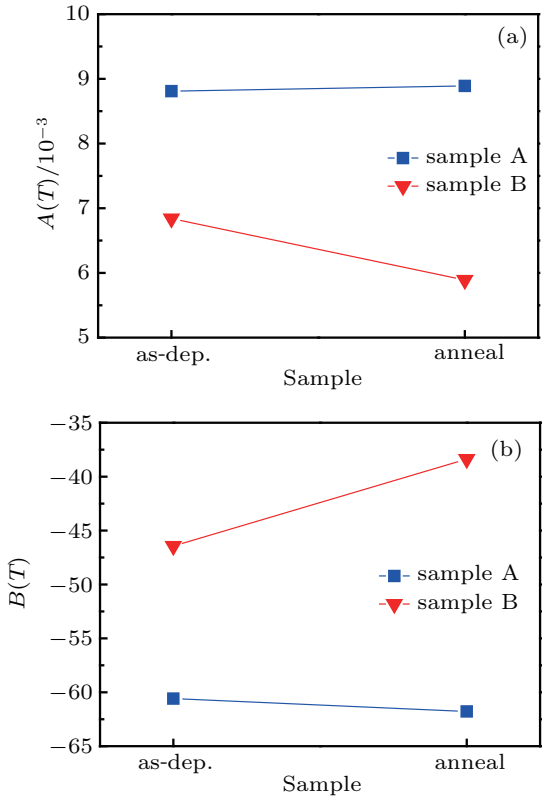


Fig. 5. (color online) (a) Slope and (b) *y*-intercept values of the fit (solid) lines in Fig. 4.

In order to investigate the origin changes of the HfO_2/Al_2O_3 gate stacks on Ge substrate before and after annealing, figure 6 shows the XPS core-level spectra of Ge_{3d} for HfO_2/Al_2O_3 gate stacks on Ge substrates measured by XPS. All peaks are referenced to those of the Ge substrate at a binding energy of 29.4 eV. As shown in Fig. 6, the Ge_{3d} peak of sample A can be fitted to four peaks, which are located at the binding energy of 29.4 eV, 30.0 eV, 31.1 eV, and 33.2 eV, respectively. They are attributed to the Ge substrate, GeO_x or germanate, GeO_2, respectively.[22] After annealing, the peak intensities of GeO_2 and GeO_x or germanate peaks increase a little due to the diffusion of the atoms, and the peak composition of GeO_x or germanate increases from 7.91 at.% to 10.54 at.%. For sample B, the Ge_{3d} peak can also be fitted to four peaks, which are located at the binding energies of 29.4 eV, 30.0 eV, 31.0 eV, and 33.1 eV, respectively. They are attributed to the Ge substrate, GeO_x or germanate, GeO_2, respectively.[22] After annealing, the peak intensities of GeO_2 and GeO_x or germanate peaks decrease significantly. It can be explained by the fact that the GeO volatilization is caused by the GeO_2/Ge interface reaction through the $GeO_2+Ge\rightarrow 2GeO(\uparrow)$.[23] The GeO_2 and Ge suboxide are consumed by the reaction of the GeO generation. The GeO diffusing out to the air generates a number of voids in the HfO_2/Al_2O_3 gate stack, which is confirmed by AFM results. Houssa *et al.* demonstrated that Al incorporation close to the dielectric/Ge interface tends to form germanate layers.[24] Moreover, Shibayama *et al.* reported that AlGeO appears at the interface of Al_2O_3 on Ge substrate after the O_2 annealing at 550 °C, and it is located at a binding energy of 31.6 eV.[25] Therefore, we conclude that the peak of sample A located at the binding energy of 31.1 eV is more likely to be that of a germanate or germanate mixed with the germanium suboxide, which acts as a barrier and suppresses the GeO volatilization after annealing. In addition, the peak of sample B located at the binding energy of 31.0 eV should be more likely to be that of germanium suboxide instead of a germanate.[8]

Figure 7 shows the Al_{2p} spectra of the HfO_2/Al_2O_3 gate stacks on Ge substrate before and after annealing. The Al_{2p} spectrum of Al_2O_3 with a thickness of 20 nm deposited by ALD is given as the reference. The binding energy of Al_{2p} in the 20-nm Al_2O_3 is located at 74.5 eV, which indicates the oxidation state of Al in the Al_2O_3 deposited by ALD is 3+.[26] For sample A, the binding energy of the Al_{2p} decreases from 74.3 eV to 74.1 eV after annealing. Compared with the Al_{2p} peak of bulk Al_2O_3, the Al_{2p} peaks of sample A undergo a shift toward lower binding energy. This behavior may be caused by the formation of aluminum germanate,[26] which is consistent with the Ge_{3d} spectra. For sample B, no change is observed in the binding energy of the Al_{2p} before and after annealing. Moreover, the binding energy of 74.4 eV is very close to the Al_{2p} peak of bulk Al_2O_3, which indicates that nearly no germanate is formed. From these XPS analyses, it can be concluded that sample A with an *in-situ* ozone treatment can suppress the formation and desorption of GeO during annealing, and the interface thermal stability of the high-κ/Ge gate stack is improved.

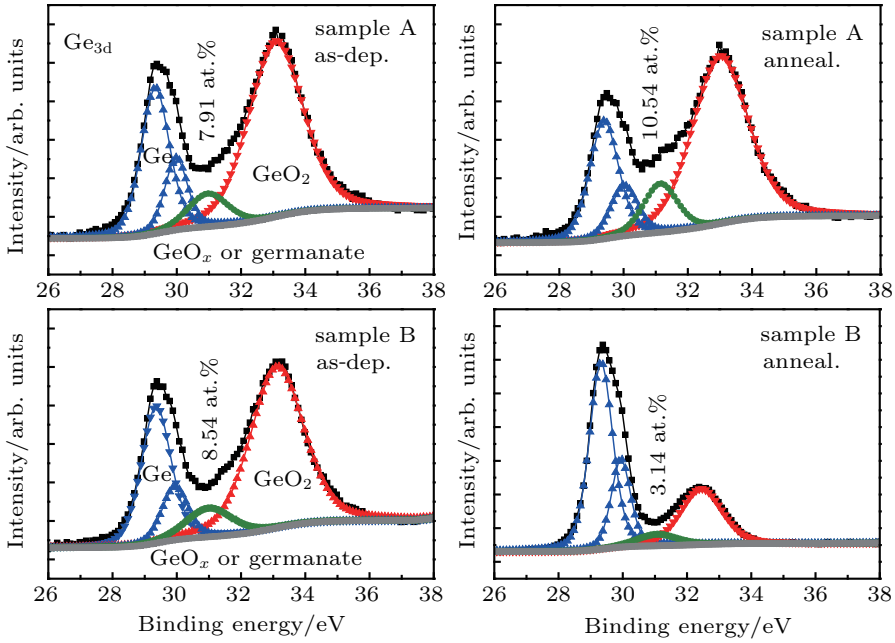


Fig. 6. (color online) Ge_{3d} spectra of the HfO_2/Al_2O_3 gate stacks on Ge substrate before and after annealing.

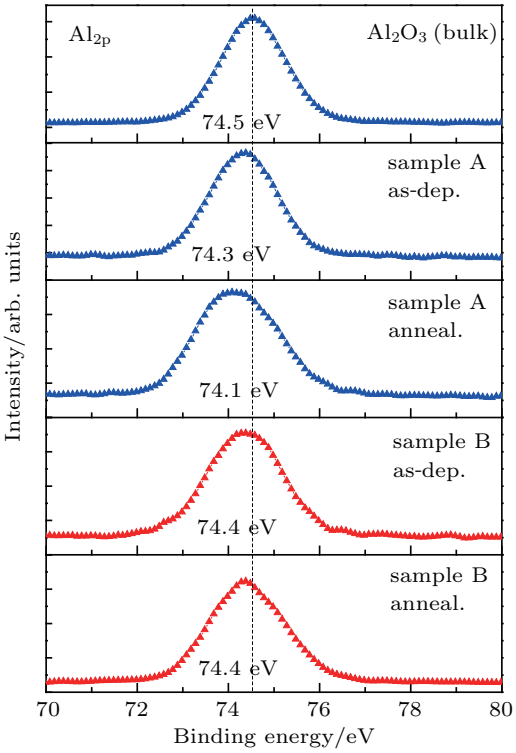


Fig. 7. (color online) Al_{2p} spectra of the HfO_2/Al_2O_3 gate stacks on Ge substrate before and after annealing.

4. Conclusions

In this work, an *in-situ* ozone treatment is carried out to improve the interface thermal stability of HfO_2/Al_2O_3 gate stack on Ge substrate. The micrometer scale level of the HfO_2/Al_2O_3 gate stack on Ge is studied using CAFM with a conductive tip. The initial results indicate that *in-situ* ozone treatment can form an interfacial germanate to suppress the GeO volatilization after annealing, which is confirmed by AFM and XPS results. For the HfO_2/Al_2O_3 gate stack on Ge with an *in-situ* ozone treatment void-free surface, low conductive spots, low leakage current density, and relative high breakdown voltage, high-κ/Ge are obtained after annealing. The electrical properties of the high-κ/Ge with an *in-situ* ozone treatment can be substantially improved compared with those of non *in-situ* ozone treated high-κ/Ge samples. All testing results indicate that *in-situ* ozone treatment is a promising method to improve the interface thermal stability of non-planar Ge-based devices in future technology nodes.

References

[1] Zhang R, Tang X, Yu X and Li J 2016 *IEEE Electron Dev. Lett.* **37** 831
[2] Asahara R, Hideshima I, Oka H, Minoura Y, Ogawa S, Yoshigoe A, Teraoka Y, Hosoi T, Shimura T and Watanabe H 2015 *Appl. Phys. Lett.* **106** 233503
[3] Tan T T, Liu Z T and Li Y Y 2011 *Chin. Phys. Lett.* **28** 086803
[4] Shin Y, Chung W, Seo Y, Lee C H, Sohn D K and Cho B J 2014 *VLSI Symp. Tech. Dig.* pp. 1–2
[5] Takagi S, Noguchi M, Kim M, Kim S H, Chang C Y, Yokoyama M, Nishi K, Zhang R, Ke M and Takenaka M 2016 *Solid-State Electron.* **125** 82
[6] Kita K, Suzuki S, Nomura H, Takahashi T, Nishimura T and Toriumi A 2008 *Jpn. J. Appl. Phys.* **47** 2349
[7] Golias E, Tsetseris L, Dimoulas A and Pantelides S T 2011 *Microelectron. Eng.* **88** 427
[8] Xie Q, Deduytsche D, Schaekers M, Caymax M, Delabie A, Qu X P and Detavernier C 2011 *Electochem. Solid-State Lett.* **14** G20
[9] Fan J B, Ding X F, Liu H X, Xie P F, Zhang Y T and Liao Q L 2016 *Chin. Phys. B* **25** 027702
[10] Ke M, Yu X, Chang C, Takenaka M and Takagi S 2016 *Appl. Phys. Lett.* **109** 032101
[11] Zhang R, Huang P C, Lin J C, Taoka N, Takenaka M and Takagi S 2013 *IEEE Trans. Electron Dev.* **60** 927
[12] Ando T, Hashemi P, Bruley J, Rozen J, Ogawa Y, Koswatta S, Chan K, Cartier E A, Mo R and Narayananet V 2017 *IEEE Electron Dev. Lett.* **38** 303
[13] Yang X, Wang S K, Zhang X, Sun B, Zhao W, Chang H D, Zeng Z H and Liu H G 2014 *Appl. Phys. Lett.* **105** 092101

[14] Bayerl A, Lanza M, Aguilera L, Porti M, Nafría M, Aymerich X and Gendt S 2013 *Microelectron. Reliab.* **53** 867
[15] Adachi M, Kato Y, Kato K, Sakashita M, Kondo H and Takeuchi W, Nakatsuka O and Zaima S 2011 *Jpn. J. Appl. Phys.* **50** 584
[16] Wang S K, Kita K, Lee C H, Tabata T, Nishimura T, Nagashio K and Toriumi A 2010 *J. Appl. Phys.* **108** 054104
[17] Wang S K, Kita K, Nishimura T, Nagashio K and Toriumi A 2011 *Jpn. J. Appl. Phys.* **50** 10PE04
[18] Chang H S, Baek S K, Park H, Hwang H, Oh J H, Shin W S, Yeo J H, Hwang K H, Nam S W, Lee H D, Song C L, Moonand D W and Cho M H 2004 *Electochem. Solid-State Lett.* **7** F42
[19] Fei C, Liu H, Wang X, Zhao L, Zhao D and Feng X 2017 *Nanoscale Res. Lett.* **12** 218
[20] Couso C, Iglesias V, Porti M and Claramunt S 2016 *IEEE Electron Dev. Lett.* **37** 640
[21] Rao P K, Park B, Lee S T, Noh Y K, Kim M D and Oh J 2011 *J. Appl. Phys.* **110** 025015
[22] Van Elshocht S, Caymax M, Conard T, De Gendt S, Hoflijk I, Houssa M, De Jaeger B, Van Sttebergen J, Heyns M and Merius M 2006 *Appl. Phys. Lett.* **88** 141904
[23] Wang S K, Kita K, Nishimura T, Nagashio K and Toriumi A 2011 *Jpn. J. Appl. Phys.* **50** 04DA01
[24] Houssa M, Pourtois G, Caymax M, Meuris M and Heyns M M 2008 *Appl. Phys. Lett.* **92** 242101
[25] Shibayama S, Kato K, Sakashita M, Takeuchi W, Nakatsuka O and Zaima S 2012 *Thin Solid Films* **520** 3397
[26] Bellenger F, Merckling C, Penaud J, Houssa M, Caymax M, Meuris M, De Meyer K and Heyns M M 2008 *ECS Trans.* **16** 411