Stress-induced leakage current characteristics of PMOS fabricated by a new multi-deposition multi-annealing technique with full gate last process*

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In the process of high-*k* films fabrication, a novel multi deposition multi annealing (MDMA) technique is introduced to replace simple post deposition annealing. The leakage current decreases with the increase of the post deposition annealing (PDA) times. The equivalent oxide thickness (EOT) decreases when the annealing time(s) change from 1 to 2. Furthermore, the characteristics of SILC (stress-induced leakage current) for an ultra-thin SiO_2/HfO_2 gate dielectric stack are studied systematically. The increase of the PDA time(s) from 1 to 2 can decrease the defect and defect generation rate in the HK layer. However, increasing the PDA times to 4 and 7 may introduce too much oxygen, therefore the type of oxygen vacancy changes.

Keywords: high-*k*/metal gate, multi deposition multi annealing, stress-induced leakage current, post deposition annealing

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1. Introduction

The continuous scaling of device dimension has aggravated the problem of leakage current and gate oxide reliability. HfO_2 as a promising high-*k* material has replaced the traditional SiO_2 in the fabrication of nanometer devices;[1,2] it is widely used in the 22-nm node metal–oxide–semiconductor field-effect transistor (MOSFET).[3] The introduction of a high-*k*/metal gate (HK/MG) into manufacturing has enabled the continuance of device scaling. However, the multi-layer structure also brings reliability problems[4,5] such as stress-induced leakage current (SILC)[6,7] especially in the gate last process. One of the reasons that leads to a severe reliability problem is the small thermal budget. The small thermal budget leads to more traps in the dielectric and a larger gate leakage current. Therefore, the annealing process, namely, post deposition annealing (PDA) would be a beneficial method to improve the reliability of the metal–oxide–semiconductor (MOS) devices.[8] Generally, simple annealing is applied in the manufacturing process. It is discovered that this cannot optimize the reliability problem. Then a new annealing method is proposed.[9,10] But more detailed and systematic analysis about the influence of MDMA on the reliability characteristic, including SILC, is absent. In this paper, the annealing time effects on the SILC characteristic are studied.

2. Experiment

In this experiment, (100) n-type Si wafers with resistivity of 2 Ω ∼4 Ω are prepared by diluted buffered oxide etch solution (NH4F:HF D 7:1). The SiO_2/HfO_2/TiN gate stack is fabricated with the Si wafer by a gate-last process. The interface layer (IL) is grown using the O-zone method, and the 28 cycles of HfO_2 films are deposited by atomic layer deposition (ALD) using the multi-deposition multi-annealing (MDMA) technique. Four samples with different deposition and annealing (D & A) cycles are prepared. The D & A cycle(s) of samples A, B, C, and D are 1, 2, 4, and 7 respectively as shown in Table 1; for each D & A cycle of these samples, the film is annealed at 450 °C in an N_2/O_2 (N_2:O_2 = 10:1) ambient for 15 s. The stacked metal gate consists of 2-nm TiN, 2-nm Ti, TiN, and 75 nm·W.

The TiN as a barrier layer is deposited by atomic layer deposition (ALD). In this process the cycles of HfO_2 are kept the same for these four samples. Then Ti is formed by physical vapor deposition (PVD) followed by ALD W as the gate elec-

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trode. After preparation of the devices, the capacitance (C) and leakage current (I_g) are measured with a Keithly 4200-SCS semiconductor parameter analyzer. Then the reliability characteristics are evaluated with an Agilent 4156C. In the SILC test, MOS capacitors are stressed in the accumulation area for constant voltage stress (CVS). The areas under test are all 100 μm^2.

Table 1. MDMA details of these four samples.

Sample	A	B	C	D
D & A cycles	1	2	4	7
ALD HfO_2 cycles/D & A Cycle/n)	28	14	7	4
Annealing time/D & A cycle/s	15	15	15	15
Total ALD HfO_2 cycles	28	28	28	28
Total annealing time/s	15	30	60	105

3. Results and discussion

3.1. Basic electrical characterization

Generally, the HfO_2 film is treated with one-time PDA, and its C–V and I–V characteristics are shown in Fig. 1 comparing with other multi-annealing samples.

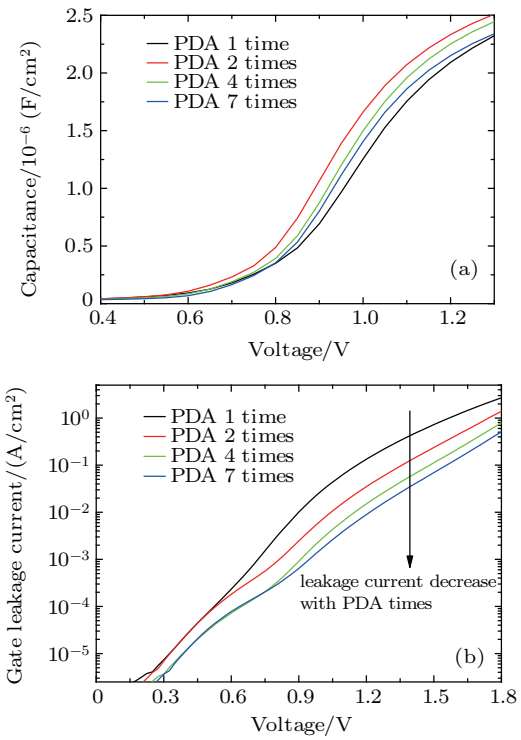


Fig. 1. (color online) (a) The C–V curve of p-MOSCAPs. (b) The I_g–V_g characteristics of p-MOSCAPs.

The EOTs of the four samples are shown in Fig. 2(a). The EOT is extracted from the C–V curves measured at 1 MHz using the UC-Berkley quantum-mechanical C–V simulator. It demonstrates that increasing the PDA times properly can improve the electrical characteristics of the devices including the EOT and gate leakage current. But when the PDA times increase to 7, the EOT of the device increases which was not expected. Then it is deduced that to improve the electrical properties of the devices of sub-1nm EOT, the MDMA technique can be applied and the D & A cycles must be chosen properly.

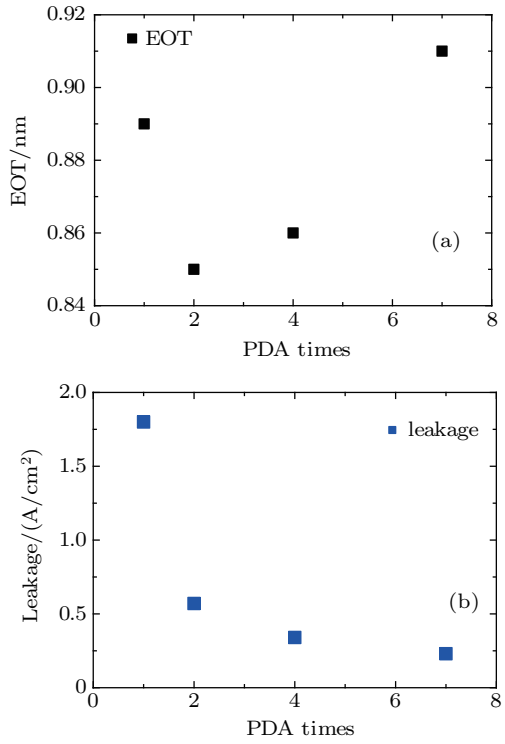


Fig. 2. (color online) (a) EOT versus PDA times. (b) Gate leakage current @$V_{fb}+1$ V versus PDA time.

3.2. Physical characterization

The TEM results are shown in Fig. 3.[11] Generally the physical thicknesses of the interface layer (IL) and the high-k layer are consistent with the EOT of each sample except sample 2. The physical thickness of sample 1 is bigger than that of sample 2, while the leakage of sample 1 is larger than that of sample 2. Therefore, it is deduced that the quality of the high-k layer of sample 2 is better than that of sample 1. The content of oxygen in HfO_2 of each sample is shown in Fig. 4. The atom number percent O/Hf of sample 2 is closer to the ideal number 2 than sample 1. This is consistent with the above deduction.

3.3. Stress-induced leakage current

The results of the electric characteristics test have shown that proper PDA cycles can contribute to the improvement of the basic performance of the device. To further verify that this MDMA technique can be applied in the manufacturing of the devices, the reliability properties SILC of the devices are studied. The sense-stress-sense method is used. The constant voltage is applied to each sample at a certain time. After the stress, the I_g–V_g relationship of the device is recorded. The stress voltage in our experiment is 2 V. The results of the SILC test of the four samples are shown in Fig. 5. The trap generation rates are sensed at 1.0 V as shown in Fig. 6.

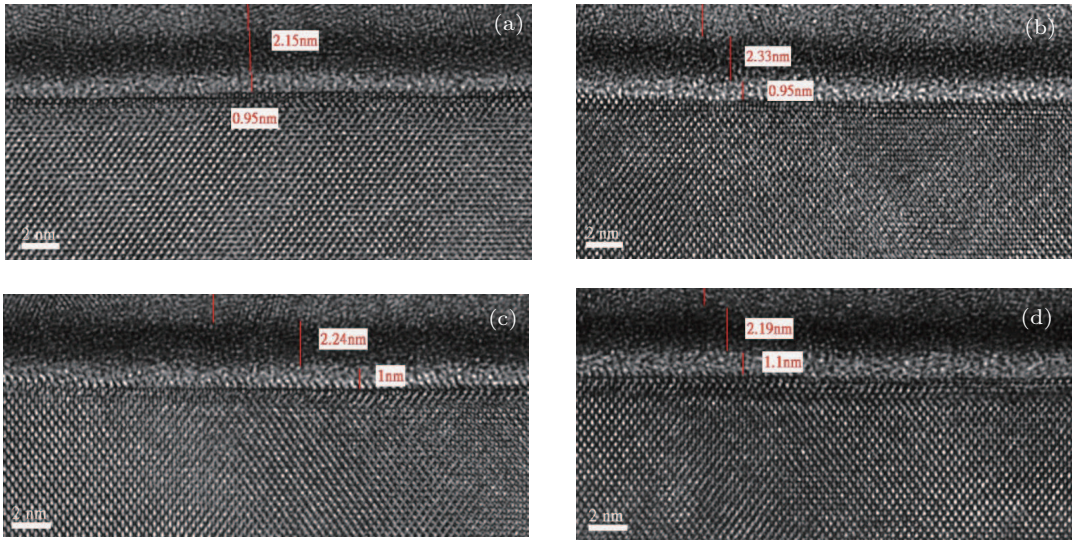


Fig. 3. (color online) TEM pictures show the EOT of these four samples: (a) PDA 15-s 1 time. (b) PDA 15-s 2 times. (c) PDA 15-s 4 times. (d) PDA 15-s 7 times.

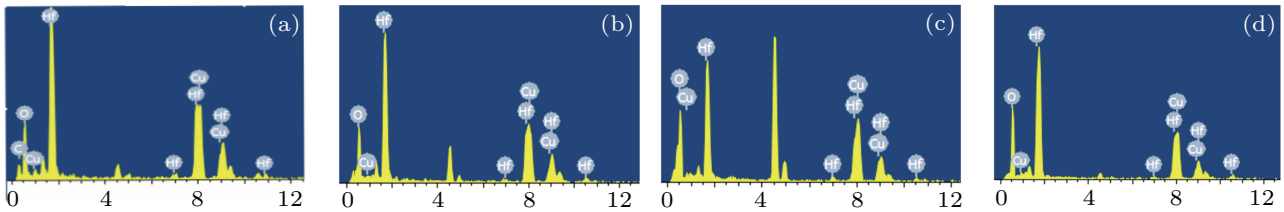


Fig. 4. (color online) EDX spectrum of HK layers of the samples with (a) PDA 15-s 1 time: oxygen content 59.41%, (b) PDA 15-s 2 times: oxygen content 64.67%, (c) PDA 15 s 4 times: oxygen content 74.46%, and (d) PDA 15-s 7 times: oxygen content 77.19%.

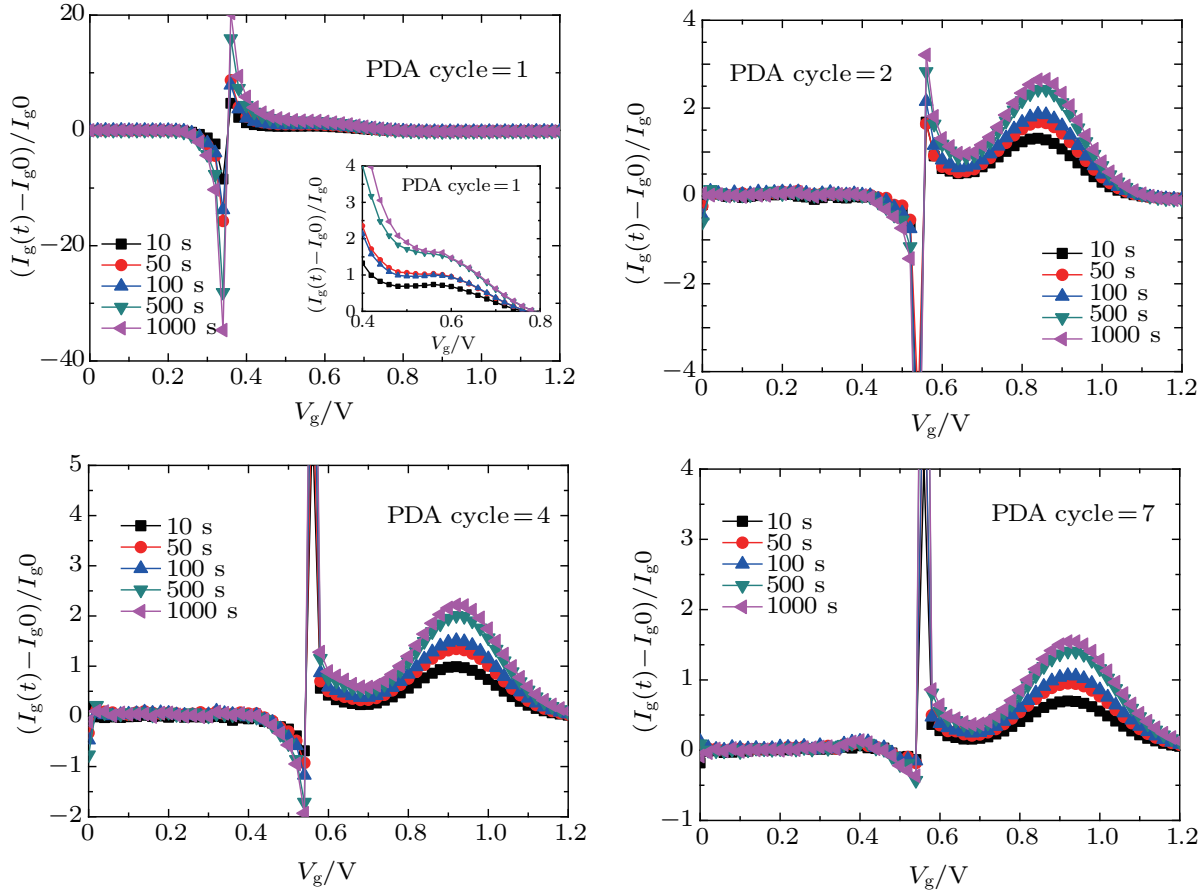


Fig. 5. (color online) The SILC characteristics of the four samples.

The increase of PDA times can decrease the generation rate of the devices. It is reported that the SILC is induced by an increase in the amount of shallow defect levels.[12] The two most likely intrinsic defects in terms of their formation energies are the oxygen vacancy and oxygen interstitial.[13–15] The energy of the oxygen interstitial is deeper as calculated by K. Xiong,[15] therefore, the most likely kind of defect that leads to SILC is the oxygen vacancy. The EDX spectra results as shown in Fig. 4 indicate that the atom number percent O/Hf of sample 1 and sample 2 is less than 2, while the atom number percent O/Hf of sample 3 and sample 4 is more than 2. This means that the type of oxygen vacancy of these four samples are different. It is conjectured that the oxygen vacancy of sample1 and 2 may be V^+ and that the oxygen vacancy of samples 3 and 4 may be V^-.

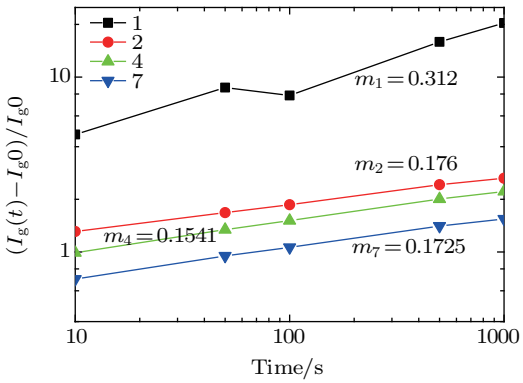


Fig. 6. (color online) The trap generation rates at the sense voltage (SILC peak) of the four samples.

4. Conclusion

The MDMA technique applied in the HKMG gate-last process is certified to reduce the gate leakage and affect the SILC characteristic of the devices. The increase of the PDA time(s) from 1 to 2 can decrease the defect in the HK layer. However increasing the PDA times to 4 and 7 may introduce too much oxygen which is to the disadvantage of the reliability characteristics of the devices. In order to optimize the performance of the devices, proper PDA times should be chosen.

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