Double-gate-all-around tunnel field-effect transistor*

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In this work, a double-gate-all-around tunneling field-effect transistor is proposed. The performance of the novel device is studied by numerical simulation. The results show that with a thinner body and an additional core gate, the novel device achieves a steeper subthreshold slope, less susceptibility to the short channel effect, higher on-state current, and larger on/off current ratio than the traditional gate-all-around tunneling field-effect transistor. The excellent performance makes the proposed structure more attractive to further dimension scaling.

Keywords: gate-all-around (GAA), tunnel field effect transistor (TFET), drain induced barrier thinning (DIBT)

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1. Introduction

Since the tunnel field-effect transistor (TFET) is a gated p-i-n transistor with a gate voltage that controls the tunneling width at the source/channel junction, carriers can be transported from the source region to the channel region by the band-to-band tunneling mechanism. The special working mechanism makes it possible for the TFET to achieve a low off-state current, a high ratio of on-state current to off-state current (I_{ON}/I_{OFF}), and a steep subthreshold slope (SS). Therefore, the TFET can work at the ultralow supply voltage and has become a promising device candidate to replace the metal-oxide-semiconductor field-effect transistor (MOSFET) in future low power applications.[1–10] However, with the further dimension scaling, short channel effects (SCEs) such as drain induced barrier thinning (DIBT) will become intolerable and deteriorate the SS, I_{ON}/I_{OFF} ratio, and the leakage current of the TFET seriously.[11] The multi-gate structures such as the double-gate,[12–15] asymmetry-gate,[16,17] and gate-all-around (GAA)[18–23] structures have been used to suppress SCEs by improving the gate control, among which the vertical GAA-TFET has received more and more attention due to its superior electrostatic performance in low power and high speed applications and the advantages of high three-dimensional (3D) integration and compatibility with existing CMOS technology.[21] Several studies based on the vertical GAA-TFET, e.g., hetero-junction,[22,23] and hetero-gate-dielectric,[24] have been made to improve the on-state current of the device. A silicide source[21] was introduced into the process of the vertical GAA-TFET to reduce the parasitic resistances.

Inspired by the nanotube FET,[31] we introduce a novel TFET in this work by adding a core gate to the GAA-TFET, which is called the double-gate-all-around TFET (DGAA-TFET). The performance of the novel device is studied by numerical simulation, and the obtained results show that the DGAA-TFET achieves improved I_{ON}/I_{OFF}, subthreshold slope, SCEs, and on-state current, as compared with the GAA-TFET.

2. Basic device concept

The 3D structure and schematic cross section of the DGAA-TFET are shown in Figs. 1(a) and 1(b), respectively, and the corresponding structure and cross section of the GAA-TFET are also shown in Figs. 1(c) and 1(d) respectively for comparison. The fabrication process of the vertical DGAA-TFET, which is similar to that of the vertical GAA-TFET,[21] is depicted in Fig. 1(e).

In the present study, the lengths of the drain and source regions are both fixed at 20 nm, and the channel length ranges from 10 nm to 60 nm. The doping concentrations of the drain, channel, and source regions are 1×10^{20} cm^{-3}, 1×10^{16} cm^{-3}, and 1×10^{19} cm^{-3}, respectively. The work function φ_{M1} of the outer gate M1 is fixed at 4.2 eV, whereas the work function $\varphi_{M2}$of the core gate M2 varies from 4.2 eV to 4.8 eV. The thickness of the gate dielectric HfO_2 is 2 nm. The body diameter of the GAA-TFET is 20 nm, which is equal to the outer diameter of the DGAA-TFET.

Simulation is conducted using Silvaco ATLAS.[24] Since the tunneling process is nonlocal, we use a nonlocal band-to-band tunneling (BTBT) model which takes into account the spatial variation of the energy bands. The trap-assist-tunneling model (tunnel.trap) is also considered to calculate the tun-

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neling current, and Fermi–Dirac statistics, while Shockley–Read–Hall (SRH) recombination models are included for calculating the transport characteristics. Since the drain and source regions are both highly doped, the band gap narrowing model (BGN) is included. The Lombardi mobility model (CVT) is used for the mobility effect, and the quantum confinement (QC) effect is considered, but the gate leakage is neglected in the simulation.

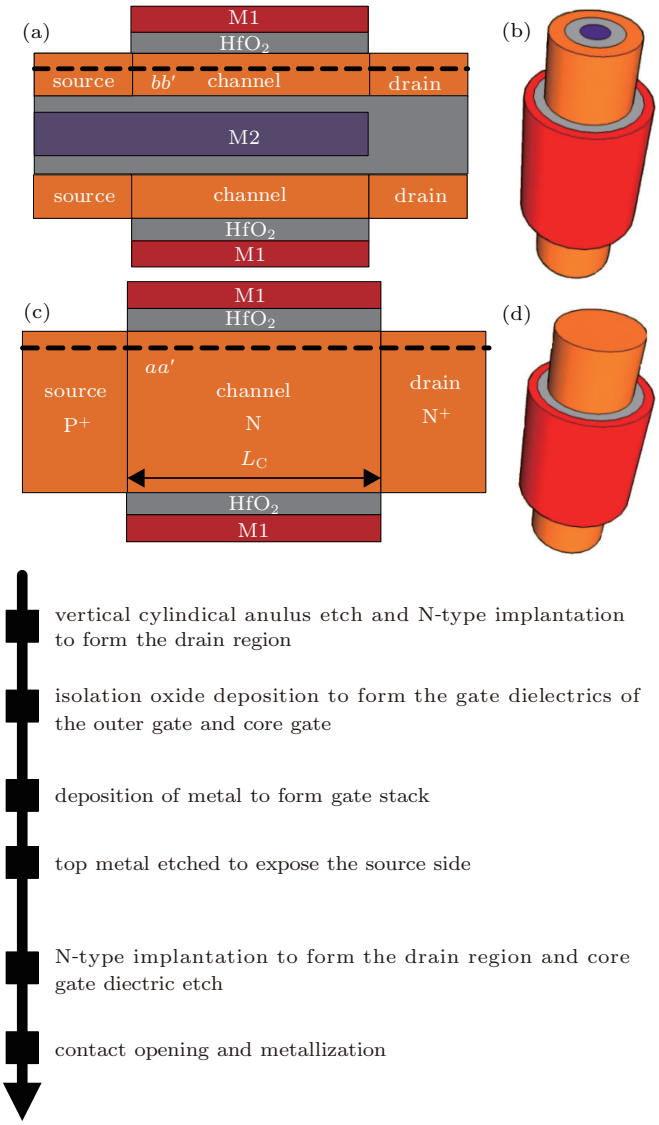


Fig. 1. (color online) (a) Schematic cross-section of the DGAA-TFET. (b) 3D structure of the DGAA-TFET. (c) Schematic cross-section of the GAA-TFET. (d) 3D structure of the GAA-TFET. (e) Fabrication process of the DGAA-TFET.

3. Simulation results and discussions

Figure 2 exhibits the transfer characteristics of the DGAA-TFET and GAA-TFET with the channel lengths of 10 nm and 40 nm. From Fig. 2, it is obvious that when the channel length decreases from 40 nm to 10 nm, the leakage current of the GAA-TFET at $V_{gs} = 0$ V deteriorates seriously (from 10^{-13} A/μm to 10^{-10} A/μm), whereas the DGAA-TFET shows less sensitivity to the channel length.

Figure 3 shows the comparison between the DGAA-TFET and GAA-TFET in terms of I_{ON}/I_{OFF} ratio, in which the on-state current of each device is obtained under $V_{DS} = 1$ V and $V_{GS} = V_{TH} - 0.4$ V, and the off-state current is obtained under $V_{DS} = 1$ V and $V_{GS} = V_{TH} + 0.6$ V. It can be seen that the DGAA-TFET outperforms the GAA-TFET in terms of the I_{ON}/I_{OFF} ratio. When the channel length decreases to 10 nm, I_{ON}/I_{OFF} of the GAA-TFET is seriously deteriorated, whereas the DGAA-TFET shows less sensitivity to the channel length, which results from its thinner body[16] and additional core gate.

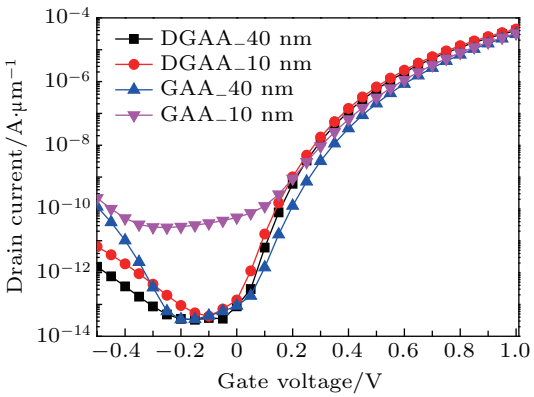


Fig. 2. (color online) Transfer characteristics of DGAA-TFET and GAA-TFET with channel lengths of 10 nm and 40 nm ($\varphi_{M2} = 4.6$ eV).

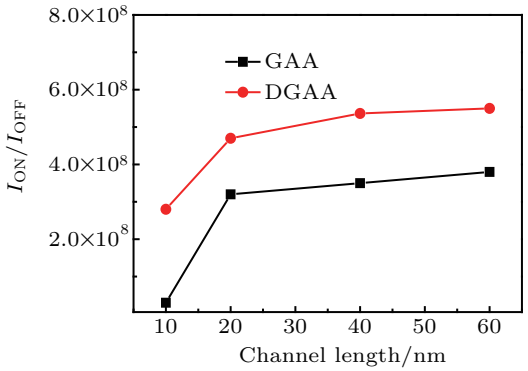


Fig. 3. (color online) Plots of I_{ON}/I_{OFF} ratio versus channel length ($\varphi_{M2} = 4.6$ eV, $L_C = 10$ nm, 20 nm, 30 nm, 40 nm, 50 nm, 60 nm).

The plots of transconductance (g_m) and transconductance-to-drive current ratio (g_m/I_D) versus overdrive voltage ($V_{GT} = V_G - V_{TH}$) for the DGAA-TFET are depicted in Fig. 4. For comparison, the corresponding characteristics of the GAA-TFET are also shown in Fig. 4. It can be found that with the increase of the gate voltage, the conductance increases. Higher g_m of the DGAA-TFET than the GAA-TFET shows that the proposed device has stronger gate control. Additionally, the g_m/I_D ratio is higher in the DGAA-TFET than in the GAA-TFET. The g_m/I_D is an important device performance parameter for the analog circuit, since the transconductance represents the amplification delivered by the device, and the drain current represents the power dissipation to obtain the

amplification.[29] It is concluded that the DGAA-TFET is capable of providing a higher gain than the GAA-TFET at the same power level.

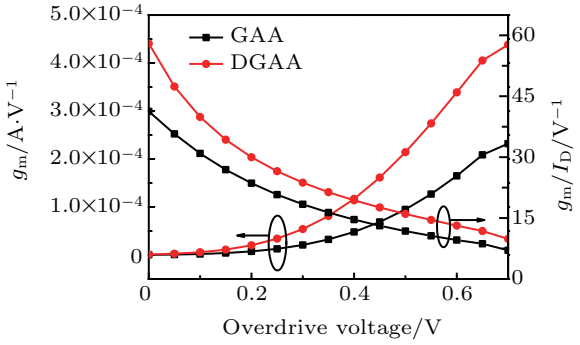


Fig. 4. (color online) Plots of transconductance (g_m) and transconductance-to-drive current ratio (g_m/I_d) versus overdrive voltage of the DGAA-TFET and GAA-TFET with a channel length of 10 nm ($\varphi_{M2} = 4.6$ eV).

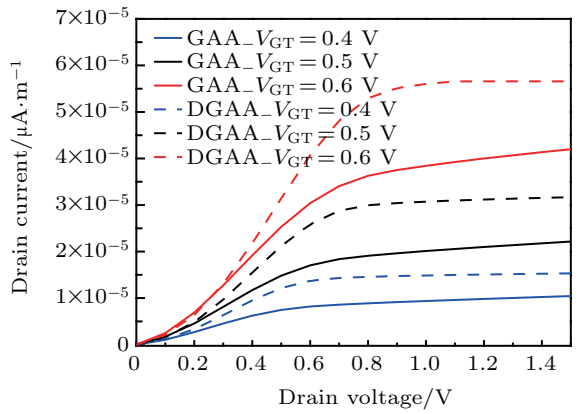


Fig. 5. (color online) Output characteristics for three different gates. The channel length is 10 nm and $\varphi_{M2} = 4.6$ eV.

Figure 5 shows a comparison of the output characteristic between the DGAA-TFET and the GAA-TFET at 10 nm channel length. Initially, the drain currents of two devices increase very rapidly with increasing drain voltage, and then the rates of increase in the drain currents decrease. Finally, the DGAA-TFET shows a good saturation of drain current at higher drain voltage. However, the GAA-TFET exhibits a different behavior at higher drain voltage, and the drain current of the GAA-TFET improves slowly with the increase of the drain voltage. To explain the phenomenon mentioned above, figures 6(a) and 6(b) are depicted, which show the energy band diagrams for different drain voltages corresponding to $V_{GT} = 0.4$ V of the DGAA-TFET and the GAA-TFET, respectively. For both devices, when the drain voltage is small, the band of the channel region is pinned by the drain potential. The drain voltage appears across the tunneling junction.[30] The tunneling widths of two devices decrease with the increase of the drain voltage, and the drain currents are increased rapidly. For the DGAA-TFET, when the drain voltage is large enough, the tunneling junction is no longer affected by the increase of the drain voltage and shows a good saturation of the drain current. For the GAA-TFET, however, when the drain voltage is large enough, the change of tunneling width cannot be neglected, and the drain current is increased slightly with the increase of the drain voltage and shows a bad saturation of drain current.

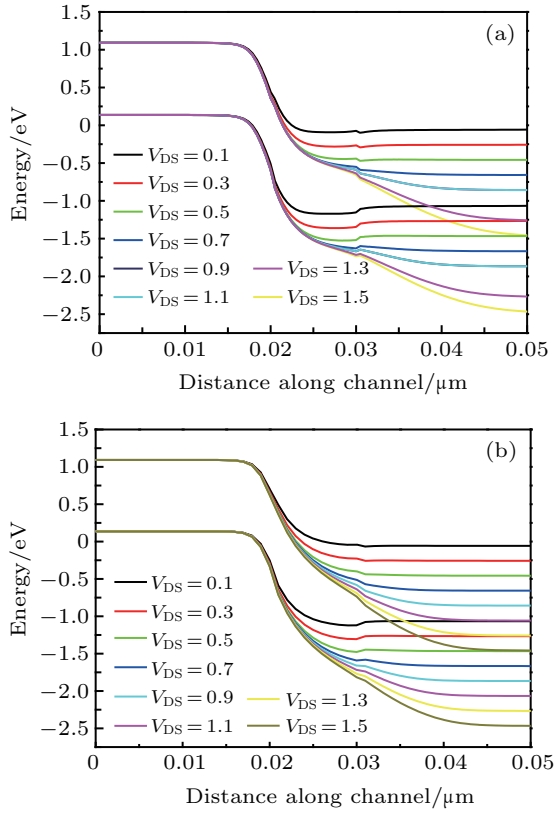


Fig. 6. (color online) (a) Energy band diagrams for different values of V_{DS} at $V_{GT} = 0.4$ V for the DGAA-TFET. (b) Energy band diagrams for different values of V_{DS} at $V_{GT} = 0.4$ V for the GAA-TFET. $\varphi_{M2} = 4.6$ eV, $L_C = 10$ nm, $V_{DS} = 0.1$ V, 0.3 V, 0.5 V, 0.7 V, 0.9 V, 1.1 V, 1.3 V, 1.5 V.

Figure 7 displays the plots of DIBT versus channel length of the DGAA-TFET and GAA-TFET, which is defined as the difference between the threshold voltages when the drain voltages are 0.1 V and 1.0 V. It can be seen when the channel length is large enough, the DIBT of the DGAA-TFET (45 mV/V) is smaller than that of the GAA-TFET (53 mV/V). We can also find that a shorter channel length will worsen DIBTs of both the DGAA-TFET and the GAA-TFET, but the DGAA-TFET shows better DIBT suppression than the GAA-TFET. In order to explain the difference, figure 8 depicts the energy band diagrams of the GAA-TFET along the cutline aa' and the DGAA-TFET along the cutline bb' (2 nm away from the interface between the body and the oxide). It can be seen from Figs. 8(a) and 8(b) that when the channel length is large (40 nm), the drain voltage increases from 0.1 V to 1.0 V and the gate voltage keeps a constant ($V_{GS} = V_{TH}$), the tunneling barrier width of the DGAA-TFET changes little, whereas the tunneling barrier width of the GAA-TFET changes obviously. The DGAA-TFET shows much less sensitivity to the drain voltage and therefore much better DIBT suppression than the

GAA-TFET. When the channel length decreases from 40 nm to 10 nm, the tunneling barrier thinning of the two devices are much more obvious than that of 40 nm. However, the variation of the tunneling barrier width of the DGAA-TFET is less than that of the GAA-TFET, which means that the DGAA-TFET shows less sensitivity to the channel length than the GAA-FET. With a thinner body and a core gate, the DGAA-TFET shows stronger gate control and less sensitivity to the channel length than the GAA-TFET.

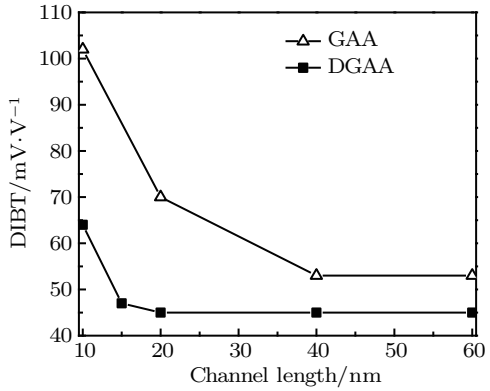


Fig. 7. Drain induced barrier thinning effects of the DGAA-TFET and GAA-TFET versus channel length. $\varphi_{M2} = 4.6$ eV, $L_C = 10$ nm, 20 nm,30 nm, 40 nm, 50 nm, 60 nm.

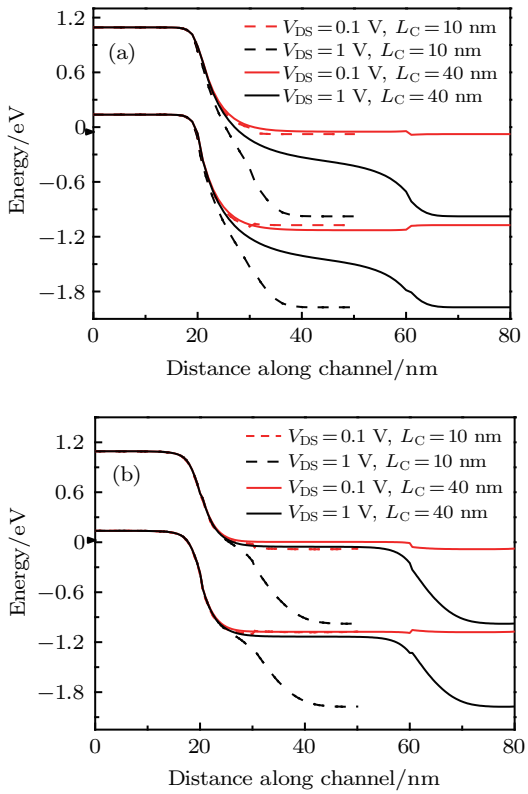


Fig. 8. (color online) (a) Energy band of GAA-TFET along aa'. (b) Energy band of DGAA-TFET along bb'. Both aa' and bb' are 2 nm away from the interface between the outside oxide and silicon.

Considering that the SS of the TFET is gate voltage dependent rather than a constant, the point subthreshold slope (SS_{POINT}) and average subthreshold slope (SS_{AVR}) are used together to depict the subthreshold characteristics. SS_{POINT} is defined as the minimum swing value at all points on the I_D–V_{GS} curve, whereas SS_{AVR} is calculated between the point at which the current begins to increase with the increasing gate voltage, and the point at which the current reaches 1×10^{-7} A/μm.[27] Figure 9 compares the DGAA-TFET with GAA-TFET in terms of SS. It can be seen that the DGAA-TFET exhibits better SS than the GAA-TFET. When the channel length decreases to 10 nm, SS_{AVR} and SS_{POINT} of the GAA-TFET are seriously deteriorated, whereas the DGAA-TFET shows less sensitivity to the channel length, which results from its thinner body[27–30] and core gate.

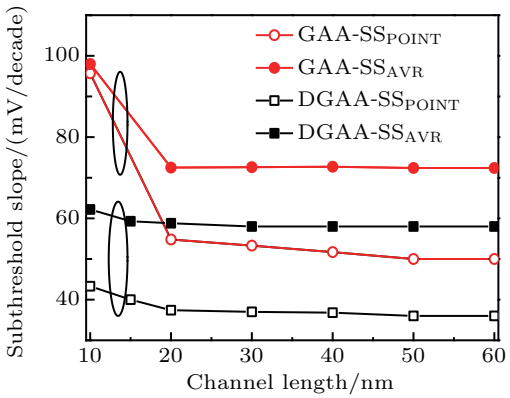


Fig. 9. (color online) Plots of subthreshold slope versus channel length. $\varphi_{M2} = 4.6$ eV.

As shown above, the advantages of the DGAA-TFET result from its thinner body and extra core gate. To investigate the effect of the work function φ_{M2}, figure 10 shows the plots of the drain current of the DGAA-TFET versus gate voltage for different values of φ_{M2}. From Fig. 10, it can be seen that when φ_{M2} decreases from 4.8 eV to 4.2 eV, the saturation current is increased, which results from the increasing tunneling probability on the source side,[2] caused by increasing the band overlap and reducing tunneling barrier width. However, it can also be found that when reducing φ_{M2}, the leakage current is deteriorated. Therefore, a trade-off should be taken into account between the on-state and off-state currents when determining the work function of the core gate.

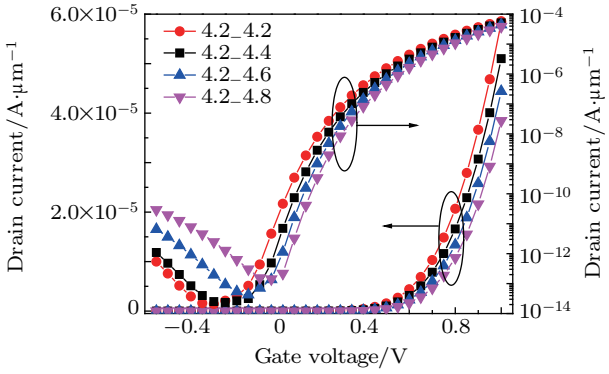


Fig. 10. (color online) Transfer characteristics of DGAA-TFET with different core gate work functions. The channel length is 10 nm.

4. Conclusions and perspectives

In this work, a novel double-gate-all-around tunnel field effect transistor (DGAA-TFET) is proposed. Compared with the conventional GAA-TFET, the DGAA-TFET exhibits high on-state current, good subthreshold slope, and small susceptivity to SCEs, which results from the extra core gate and thinner body. These excellent electrical characteristics make the proposed device a more attractive candidate to the further dimension scaling.

References

[1] Chen Q, Agrawal B and Meindl J 2002 *IEEE Trans. Electron Dev.* **49** 1086

[2] Saurabh S and Jagadesh Kumar M 2011 *IEEE Trans. Electron Dev.* **58** 404

[3] Wang H, Chang S, Hu Y, He J, Huang Q J, He F and Wang G F 2014 *IEEE Trans. Electron Dev.* **35** 798

[4] Nagavarapu V, Jhaveri R and Woo J C S 2008 *IEEE Trans. Electron Dev.* **55** 1013

[5] Sharma A, Goud A A and Roy K 2014 *IEEE Trans. Electron Dev.* **35** 1221

[6] Verhulst A S, Vandenberghe W G, Maex K, De Gendt S, Heyns M M and Groeseneken G 2008 *IEEE Trans. Electron Dev.* **29** 1398

[7] Agarwal S, Klimeck G and Luisier M 2008 *IEEE Trans. Electron Dev.* **31** 621

[8] Toh E H, Wang G H, Chan L, Sylvester D, Heng C H, Samudra G S and Lee Y C 2008 *Jpn. J. Appl. Phys.* **47** 2593

[9] Schlosser M, Bhuwalka K K, Sauter M, Zilbauer T, Sulima T and Eisele I 2008 *IEEE Trans. Electron Dev.* **31** 621

[10] Kim S H, Agarwal S, Jacobson Z A, Matheu P, Hu C and Liu T J K 2010 *IEEE Electron Dev. Lett.* **31** 1107

[11] Marcio D V, Martino J A and Paula G D Agopian 2014 *IEEE* 29*th Mircroelectronics Technology and Devices (SBMicro)* p. 1

[12] Shih C H and Chien N D 2011 *IEEE Electron Dev. Lett.* **32** 1498

[13] Shibir Basak, Pranav Kumar Asthana, Yogesh Goswami and Bahniman Ghosh 2014 *Appl. Phys. A* **118** 1527

[14] Kao K H, Verhulst A S, Vandenberghe W G and Meyer K De 2013 *IEEE Electron Dev. Lett.* **60** 6

[15] Guan Y H, Li Z C, Luo D X, Meng Q Z and Zhang Y F 2016 *Chin. Phys. B* **25** 108502

[16] Jhan Y R, Wu Y C and Hung M F 2013 *IEEE IEEE Electron Dev. Lett.* **34** 1482

[17] Wang Y, Wang X, Xue W and Cao F 2016 *Superlattices and Microstructures* **91** 216

[18] Min Jin Lee and Woo Young Choi 2012 *IEEE Electron Dev. Lett.* **33** 1459

[19] Moselund K E, Schmid H, Bessire C, Björk M T, Ghoneim H and Riel H 2012 *IEEE Electron Dev. Lett.* **33** 1453

[20] Rooyackers R, Vandooren A, Verhulst A S, Walke A, Devriendt K, Locorotondo S, Demand M, Bryce G, Loo R, Hikavyy A, Vandeweyer T, Huyghebaert C, Collaert N and Thean A *Proc. IEEE Int. Electron Devices Meeting,* Dec. 2013, pp. 4.2.1–4.2.4

[21] Gandhi R, Chen Z, Singh N, Banerjee K and Lee S 2011 *IEEE Electron Dev. Lett.* **32** 437

[22] Felipe S Neves, Paula G D Agopian, Joao Antonio Martino, Bogdan Cretu, Rita Rooyackers, Anne Vandooren, Eddy Simoen, Aaron Voon-Yew Thean and Cor Claeys 2016 *IEEE Trans. Electron Dev.* **63** 1658

[23] Lee H, Park J D and Shin C 2011 *IEEE Electron Dev. Lett.* **63** 1827

[24] ATLAS Device Simulation Software, Silvaco, Version 5.18.20R, 2010

[25] Guin S, Chattopadhyay A, Karmakar A and Mallik A 2014 *IEEE Trans. Electron Dev.* **61** 2515

[26] Boucart K and Ionescu A M 2007 *IEEE Trans. Electron Dev.* **54** 1725

[27] Wang Y, Wang Y F, Sun L L, Wei X and Cao F 2016 *Micro & Nano Lett.* **11** 472

[28] Zhang Q, Zhao W and Seabaugh A 2006 *IEEE IEEE Electron Dev. Lett.* **27** 297

[29] Abhijit Mallik and Avik Chattopadhyay 2012 *IEEE Trans. Electron Dev.* **59** 888

[30] Abhijit Mallik and Avik Chattopadhyay 2011 *IEEE Trans. Electron Dev.* **58** 4025

[31] Daniel Tekleab 2014 *IEEE IEEE Electron Dev. Lett.* **35** 506