High holding voltage SCR for robust electrostatic discharge protection*

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A novel silicon controlled rectifier (SCR) with high holding voltage (V_h) for electrostatic discharge (ESD) protection is proposed and investigated in this paper. The proposed SCR obtains high V_h by adding a long N+ layer (LN+) and a long P+ layer (LP+), which divide the conventional low voltage trigger silicon controlled rectifier (LVTSCR) into two SCRs (SCR1: P+/Nwell/Pwell/N+ and SCR2: P+/LN+/LP+/N+) with a shared emitter. Under the low ESD current (I_{ESD}), the two SCRs are turned on at the same time to induce the first snapback with high V_h (V_{h1}). As the I_{ESD} increases, the SCR2 will be turned off because of its low current gain. Therefore, the I_{ESD} will flow through the longer SCR1 path, bypassing SCR2, which induces the second snapback with high V_h (V_{h2}). The anti-latch-up ability of the proposed SCR for ESD protection is proved by a dynamic TLP-like (Transmission Line Pulse-like) simulation. An optimized V_{h2} of 7.4 V with a maximum failure current (I_{t2}) of 14.7 mA/μm is obtained by the simulation.

Keywords: electrostatic discharge, holding voltage, latch-up-free, failure current

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1. Introduction

With the continuing development of Si technology, the feature size of semiconductors is decreasing, which implies that the possibility of damage from electrostatic discharge (ESD) is becoming increasingly serious. Conventional ESD devices such as diodes or gate grounded N-channel metal oxide semiconductors (GGNMOS) also consume a relatively large silicon area because of their low current capability. Among ESD devices, the low voltage trigger silicon controlled rectifier (LVTSCR) has been considered as an on-chip ESD protection structure because of its lower on-state resistor, high current capability, and low trigger voltage (V_{t1}). When the chip is powered off, the SCR has the strongest ESD robustness in the smallest layout area.[1] However, particularly for the case of a supply clamp, the low V_h will prevent the structure from turning off after the ESD pulse. The transient-induced latch-up effect is a fatal defect, which affects the reliability of ICs. Moreover, the error triggered by the noises[2] also affects the stability of the IC. If the V_h of the SCR is higher than the normal supply voltage, it will be free of such issues.[2] The methods to improve the V_h of SCRs have motivated many research teams.[3–17] One method is the segmented technique, which was proposed in Refs. [3] and [14] to reduce the emitter injection efficiency. The V_h can be adjusted by optimizing the N+/P+ ratio. However, the I_{t2} is decreased, because the higher V_h leads to a higher generation of heat under the same current distribution. The stacking technique was proposed in Refs. [6] and [8]. It can improve the V_h linearly by increasing the number of unit devices. However, it not only needs a trigger circuit to ensure an acceptable V_{t1} but also requires more stacking units to achieve a higher V_h. The huge chip area occupation makes it unsuitable for use in high voltage ICs. The emitter voltage clamp is a good way to improve the V_h without additional masks under the same technological processes.[5] However, the non-adjustability of V_h is a limitation.

In this paper, a novel high V_h SCR, which features a long N+ (LN+) layer and a long P+ (LP+) layer is proposed. In the low I_{ESD} condition, the LN+ layer and the LP+ layer form two high concentration base regions of parasitic NPN and PNP, which decrease the current gain of SCR2 to improve the V_{h1}. In the high I_{ESD} condition, the low current gain of SCR2 restrains the surface current and extends the ESD path of SCR1, which induces the second snapback with high V_{h2}. As the deeper current path avoids surface current crowding, a strong ESD robustness can be obtained. Moreover, the device is entirely compatible with the technology of LVTSCRs without additional masks or process steps.

2. Device structure and mechanism

Figures 1(a) and 1(b) show the schematic cross-sectional view of the conventional LVTSCR and its layout diagram. With the increase in the ESD voltage at the anode, the breakdown of the drain PN junction of the parasitic GGNMOS (M1) enhances the trigger speed, then the avalanche current triggers

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the parasitic transistors (Q1 and Q2) by the parasitic resistors (R1 and R2). The strong positive feedback of the PNP and NPN causes strong snapback with a low V_h (about 1–2 V). Due to the low V_h, the LVTSCR cannot be used in the power clamp of the chip because of its huge risk of the latch-up effect occurring and the error trigger issue.

In order to prevent the aforementioned issues, a novel SCR is proposed in this paper. Figures 1(c) and 1(d) show the schematic cross-sectional view of the proposed SCR and its layout diagram. The proposed SCR features an LN+ layer and an LP+ layer, which constitute two high concentration base regions of parasitic PNP and NPN. In the low I_{ESD} condition, the SCR1 and SCR2 are turned on; the two high concentration base regions decrease the current gain of SCR2 and weaken its positive feedback. Therefore, the first snapback needs to have a high V_{h1} to maintain the two SCRs. With the increase in I_{ESD}, the low current gain of SCR2 causes its turn-off. The majority of the current will flow through the longer SCR1 path bypassing SCR2, which induces the second snapback with high V_{h2}. Meanwhile, the breakdown of the LN+/PWELL junction also reduces the breakdown voltage (BV) to ensure an acceptable V_{t1}.

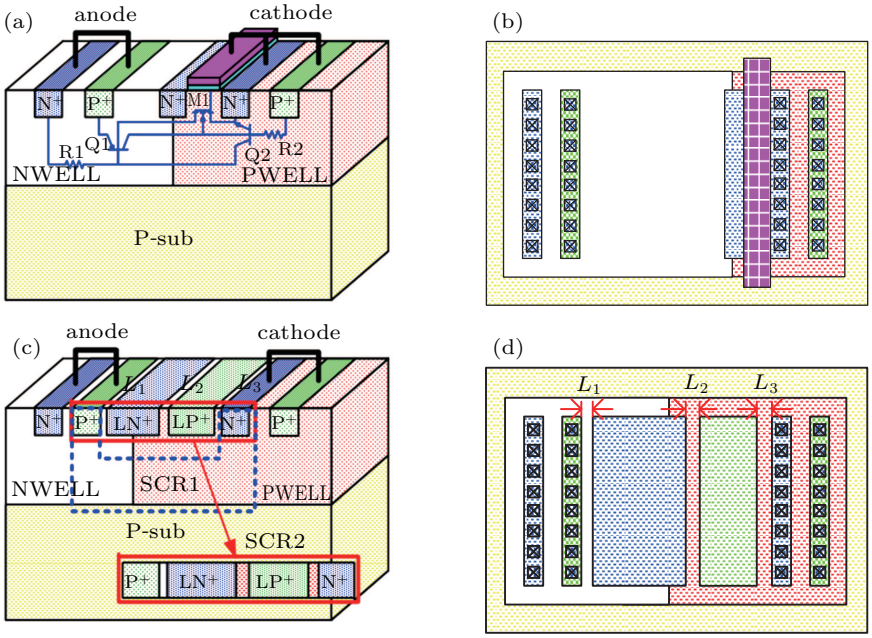


Fig. 1. (color online) (a) Cross-sectional view of the LVTSCR, (b) the layout diagram of LVTSCR, (c) the cross-sectional view of the proposed SCR, and (d) the layout diagram of the proposed SCR.

3. Results and discussion

To discuss the *I*–*V* characteristics, ESD-induced latch-up effect, and the pulse performance, the direct current (DC), dynamic TLP-like (transmission line pulse-like), and TLP multiple-pulse simulations[18–20] have been used. Figure 2 shows the dynamic TLP-like simulation and TLP multiple-pulse simulation circuit. Dynamic TLP-like simulation means a voltage pulse, which is like a TLP pulse, is applied to the anode of an LVTSCR or proposed SCR through a resistor with the anode DC voltage (V_A) equal to VDD, then a V_A-time curve, which contains the latch-up information, can be obtained. The TLP multiple-pulse simulation is similar to the actual TLP test: a series of current pulses with increasing amplitude, 10 ns of rise time, 100 ns of duration time, and 10 ns of fall time are applied to both ends of an LVTSCR or proposed SCR. Then, a series of voltage pulses can be obtained. Each current pulse and the average of 70–90% of the corresponding voltage will constitute a point on the TLP *I*–*V* curve. By linking the series of points with a line, the TLP *I*–*V* curve will be achieved. The main parameters of the proposed SCR are listed in Table 1.

The DC simulation results of the LVTSCR and proposed SCR with $L_1 = 0.3$ μm and $L_3 = 0.5$ μm are shown in Fig. 3. The V_h of the LVTSCR is 1.3 V and that of the proposed SCR is 7.4 V. In the low I_{ESD} condition, the SCR1 and SCR2 are triggered together, which need a high holding voltage ($V_{h1} = 15$ V) to maintain the two ESD paths. As the I_{ESD} increases to second holding current (I_{h2}), the SCR2 has been turned off. At this time, the SCR1 is the main path to discharge the I_{ESD}. Because the SCR1 has the longer current path, the second holding voltage (V_{h2}) will be decreased from 15 V (V_{h1}) to 7.4 V instead of 1.3 V. Meanwhile, the V_{t1} of the proposed SCR is still close to that of the LVTSCR.

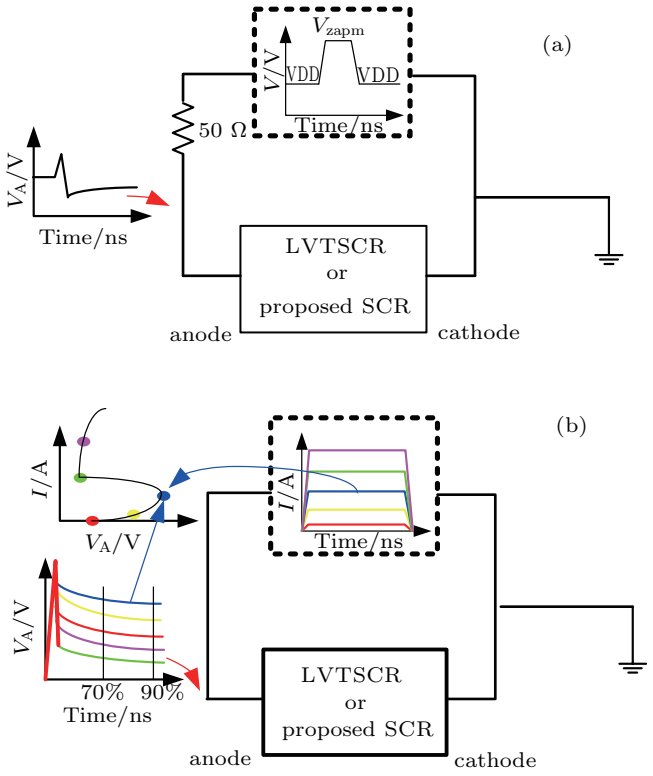


Fig. 2. (color online) (a) Dynamic TLP-like simulation circuit with V_A = VDD, and (b) TLP multiple-pulse simulation circuit.

Table 1. The main parameters of the proposed SCR.

Device parameters	Proposed SCR
Length	15 μm
The length of L_1/L_3	0.1–0.5 μm
The length of L_2	0.5 μm
NWELL concentration	5×10^{16} cm^{-3}
P-sub concentration	1×10^{15} cm^{-3}

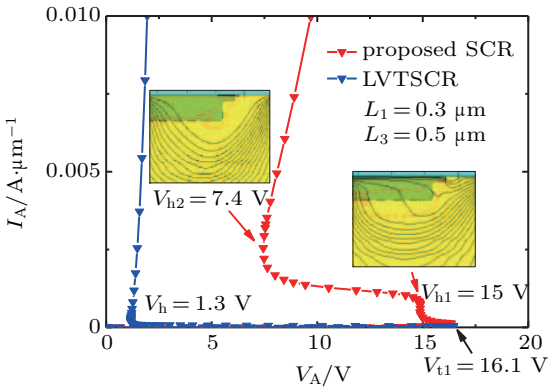


Fig. 3. (color online) DC simulation results of LVTSCR and proposed SCR with $L_1 = 0.3$ μm and $L_3 = 0.5$ μm.

According to the above theories, the V_{h2} of the proposed SCR can be adjusted by changing L_1 and L_3. Under smaller L_1 or L_3, more holes (electrons) are injected into the LN+ layer (LP+ layer), which will induce a higher I_{h2}. In addition, the longer ESD current path and the higher V_{h2} can be obtained by decreasing L_1 or L_3. Figure 4 shows the snapback I–V curves with various L_1 and L_3. These results prove the double snapback characteristic. The highest V_h of 14.6 V and V_{t1} of 16.2 V with $L_1 = 0.5$ μm and $L_3 = 0.1$ μm are obtained. When $L_1 = L_3 = 0.5$ μm, $V_{h2} = 6.1$ V: it increases up to 12.9 V when L_1 and L_3 decrease to 0.1 μm. When L_1 is fixed, the V_h will decrease with the increase in L_3. Moreover, the double snapback characteristic of the proposed SCR with $L_1 = L_3 = 0.1$ μm will disappear because V_{h2} increases up to a high value, which is close to V_{h1}, due to the longer ESD path. The V_{t1} is less sensitive to L_1 and L_3.

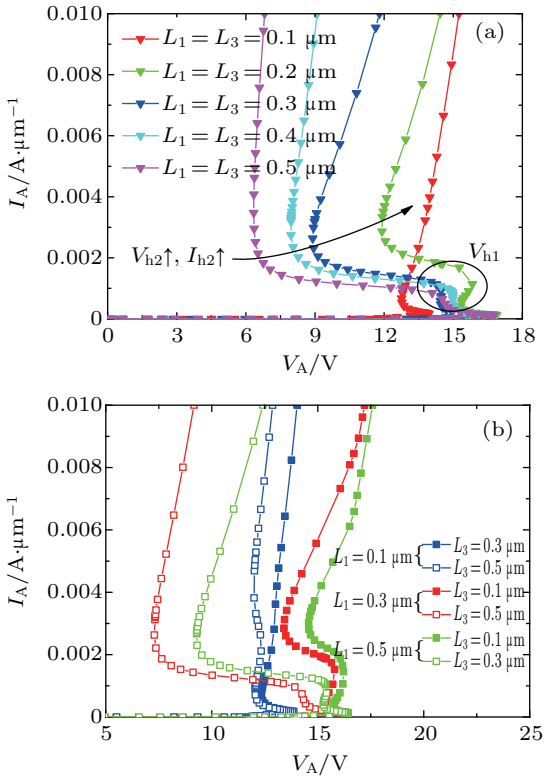


Fig. 4. (color online) (a) Snapback I–V curves of the proposed SCR with $L_1 = L_3$ increasing from 0.1 to 0.5 μm, (b) snapback I–V curves of the proposed SCR with $L_1 \neq L_3$ increasing from 0.1 to 0.5 μm.

The TLP multiple-pulse simulation has been used to analyse the pulse snapback characteristics of the LVTSCR and proposed SCR with L_1 and L_3 increasing from 0.1 to 0.5 μm. Figures 5(a) and 5(b) show the voltage response of the LVTSCR and TLP I–V curves of all SCRs when the width of the device is 50 μm. The V_h of the LVTSCR is only 1.9 V, which is far less than the highest V_h of 12.5 V with $L_1 = L_3 = 0.1$ μm. The V_{h1} will decrease to 11 V with L_1 and L_3 increasing from 0.1 μm to 0.5 μm. Meanwhile, the double snapbacks characteristic also occurs in the devices with $L_1 = L_3 = 0.3$ μm and 0.4 μm. The TLP multiple-pulse simulation shows the same trends as the DC simulation.

Figure 5(b) shows the V_{t1} of the proposed SCRs have some decreases, which are ascribed to the high concentration of the LP+ layer. The LP+ layer obstructs the depletion region extension and reduces the breakdown voltage (BV). The

simulated depletion regions are shown in Figs. 5(c) and 5(d). Figure 5(c) shows that the depletion region of the proposed SCR is obstructed on the left edge of the LP+. The avalanche breakdown of the PN junction which is formed by the LN+, P-sub, and LP+ in the proposed SCR happens easier than that of the LVTSCR, which induces the V_{t1} reduction.

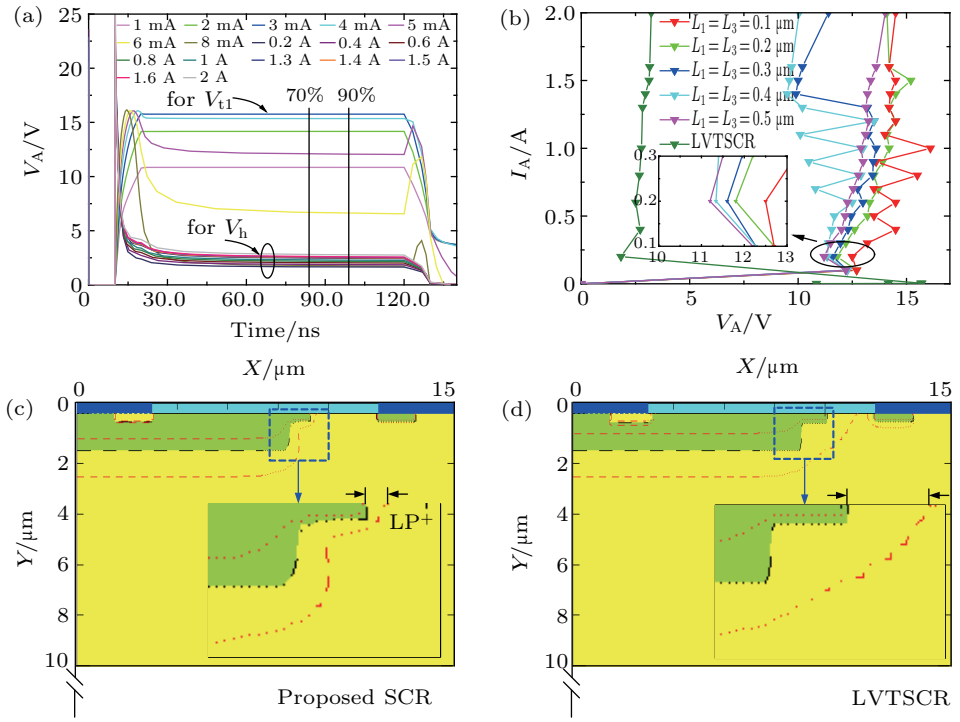


Fig. 5. (color online) (a) Example of voltage response of LVTSCR, and (b) simulated TLP I–V curves of the proposed SCR with L_1 and L_3 increasing from 0.1 to 0.5 μm. (c) Depletion region distributions of proposed SCR and (d) LVTSCR.

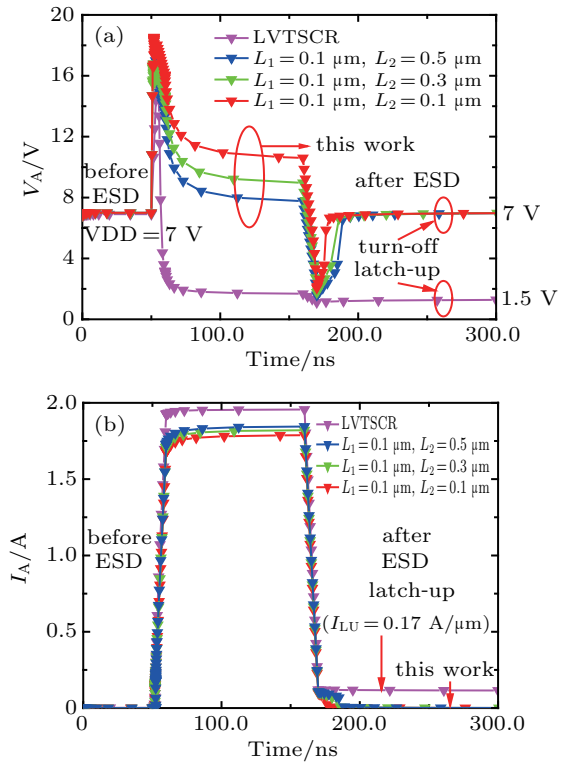


Fig. 6. (color online) (a) Voltage responses of LVTSCR and the proposed SCR with various L_1 and L_3 in 7-V circuit and (b) their corresponding current responses.

In order to analyse the transient-induced latch-up issue during normal operation, a dynamic TLP-like simulation circuit has been used. The time-domain results are shown in Fig. 6. After transient triggering, the latch-up effect may happen in the LVTSCR. The voltage is clamped down to ∼ 1.5 V and the latch-up current (I_{LU}) is 0.17 A. In contrast, the voltage of the proposed SCR is still kept at 7 V, and the I_{LU} is 0 A after the same transient pulse during normal operation in the 7 V circuit. These results prove that the proposed SCR is a high latch-up-free device for 7 V circuit ESD applications.

The maximum failure power dissipation (P_m) of the ESD device can be given by Eq. (1). The higher V_h will cause a higher power dissipation, which leads to the lower I_{t2}. Therefore, the proposed SCR with $V_h = 7.4$ V ($L_1 = 0.3$ μm, $L_3 = 0.5$ μm) is the best choice to alleviate the contradiction between V_h and I_{t2} in the 7 V circuit. Moreover, the hot area which is formed by current crowding on the right edge of the anode P+ region further causes the decrease in I_{t2}. The deeper current instead of a surface current can restrain the hot area forming and improve I_{t2}. The proposed SCR has a deeper ESD path, which will induce the lower surface temperature. Hence, it is very suitable as a device for a high level of ESD protection

$$P_m = I_{t2}\left(I_{t2}R_{device} + V_h\right) \approx I_{t2}V_h. \quad (1)$$

Figure 7 shows the detailed current distributions of the pro-

posed SCR with $L_1 = 0.3$ μm, $L_3 = 0.5$ μm under various I_{ESD}. After the proposed SCR is triggered, the majority of the current is discharged through the SCR2 path because of the lower resistance of the LN+ and LP+ regions (see Fig. 7(a)). However, the lower current gain of SCR2 causes the higher V_{h1}, which induces the higher initial surface temperature than for the LVTSCR. With the increase in I_{ESD}, figure 7(b) shows the partial current path will gradually transfer to the inner SCR1 because of its high current gain and the lower V_{h2}. The holding voltage of the device is decreasing. The total temperature will be endured by the surface lattice and inner lattice, which reduces the surface temperature rising speed. In the high I_{ESD} condition, the simulation shows that all I_{ESD} will pass through the inner SCR1 (see Fig. 7(c)). The holding voltage of the device has to drop to V_{h2}. The majority of the temperature is endured by the inner lattice, which further reduces the surface lattice temperature, so the higher I_{t2} can be obtained. Meanwhile, the longer current path makes the V_{h2} still higher than the supply power voltage to avoid the latch-up effect. Figure 7(d) also shows the current distribution of the LVTSCR under the same I_{ESD}. The surface current will increase the surface temperature and form a hot area, which is bad for its ESD robustness. Figures 8(a) and 8(b) show the temperature variation conditions of the two devices. The LVTSCR has a lower surface temperature than the proposed SCR in the low current condition ($I_{ESD} \leq 0.75 \times 10^{-2}$ A/μm) because of its lower V_h (1.3 V) than V_{h1} (15 V). However, the proposed SCR also has a high I_{t2} because the LN+ and LP+ optimize the current distribution (see Fig. 7(c)) in the high current condition ($I_{ESD} \geq 10^{-2}$ A/μm). The simulated I_{t2} of the proposed SCR with $L_1 = 0.3$ μm and $L_3 = 0.5$ μm is 14.7 mA/μm, which is even higher than that of the LVTSCR (13.6 mA/μm). Although the LVTSCR has a lower V_h than that of the proposed SCR, figure 8(c) proves that the T_{peak} of the LVTSCR has a faster rising speed than the proposed SCR with the current increasing. Figure 8(c) can be explained by the above analysis. The proposed SCR has a higher initial surface temperature than that of the LVTSCR under $I_{ESD} = 0.5 \times 10^{-2}$ A/μm. As the current transfers into the deeper body, the rising speed of the surface temperature is slowed down, which induces the higher I_{t2} the proposed SCR has under $T_{peak} = 1688$ K. Equation (1) indicates that the P_m limitation causes the contradiction between V_h and I_{t2}. The increase of P_m can not only improve the ESD robustness, but also enhance the V_h to avoid the latch-up effect. Figure 8(d) shows the on-state ESD P_m limitation curves based on the simulated data above. The proposed SCR with $L_1 = 0.3$ μm, $L_3 = 0.5$ μm can achieve a P_m of 108.78×10^{-3} W/μm, which is higher than that of the LVTSCR ($P_m = 17.68 \times 10^{-3}$ W/μm) by about 6.15 times.

The concerned parameters are contrasted in Table 2. According to the data in Table 2, the compared SCR with $L_1 = 0.3$ μm, $L_3 = 0.5$ μm has the higher P_m. The V_h of 7.4 V can avoid the transient-induced latch-up effect in the 7 V circuit. Moreover, the V_{t1} of the compared SCR is 16.1 V, which provides the same trigger speed as the LVTSCR. The higher I_{t2} (1.47×10^{-2} A/μm) is also obtained in the compared SCR. The comparison of the results shows that the compared SCR is more suitable than the LVTSCR to be used in latch-up-free robustness ESD application.

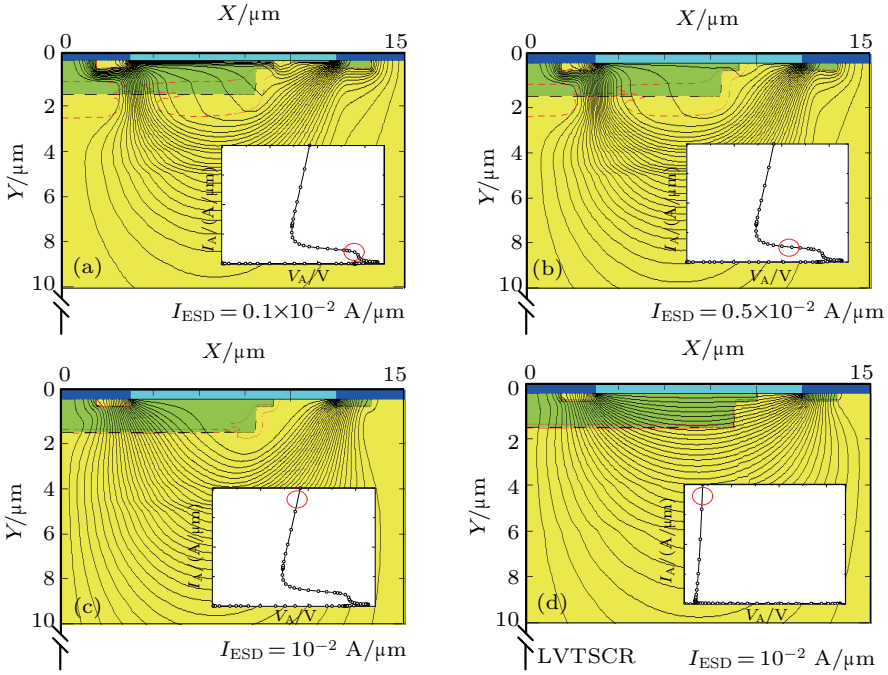


Fig. 7. (color online) Simulated current distributions of the proposed SCR with $L_1 = 0.3$ μm, $L_3 = 0.5$ μm under (a) $I_{ESD} = 0.1 \times 10^{-2}$ A/μm, (b) $I_{ESD} = 0.5 \times 10^{-2}$ A/μm, and (c) $I_{ESD} = 0.1 \times 10^{-2}$ A/μm. (d) Simulated current distributions of LVTSCR under $I_{ESD} = 1 \times 10^{-2}$ A/μm.

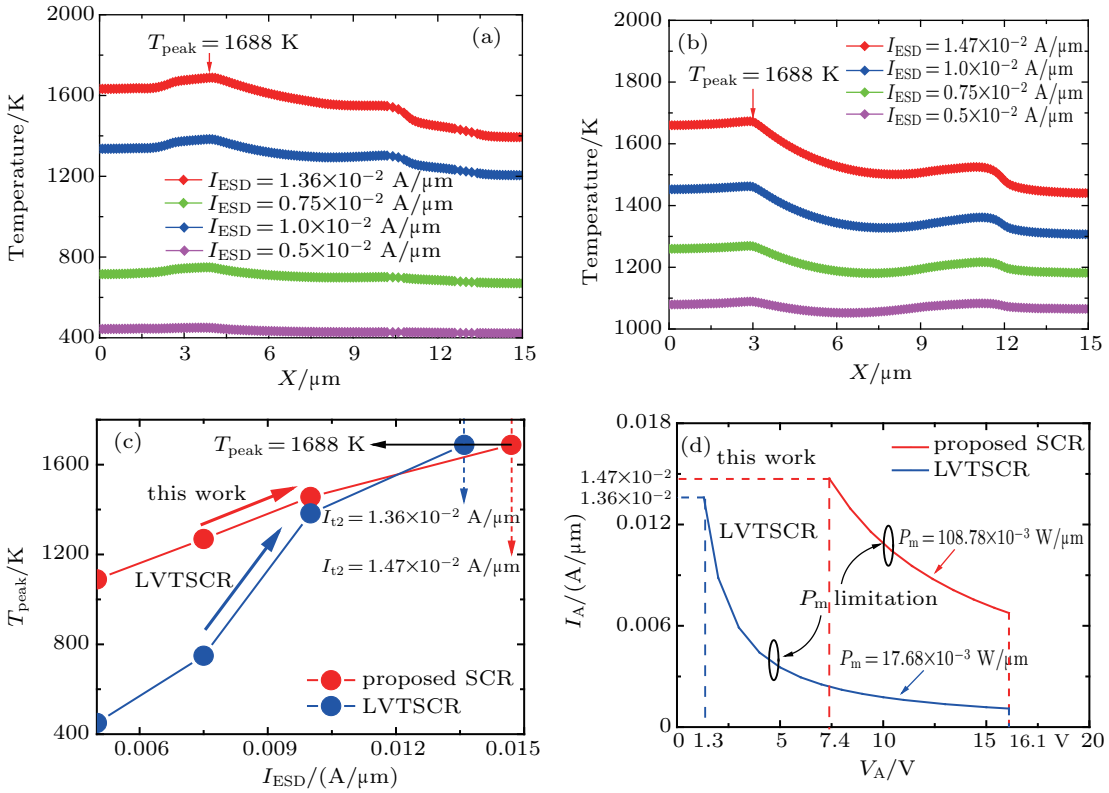


Fig. 8. (color online) (a) Simulated surface temperature distributions of LVTSCR (b) and the proposed SCR with $L_1 = 0.3$ μm, $L_3 = 0.5$ μm, (c) their T_{peak}–I_{ESD} curves, and (d) their on-state ESD P_m limitation curves.

Table 2. The parameters comparison between LVTSCR and proposed SCR.

	LVTSCR	Proposed SCR ($L_1 = 0.3$ μm, $L_3 = 0.5$ μm)
V_{t1}/V	16.1	16.1
V_h/V	1.3	7.4
I_{t2}/A·μm^{-1}	1.36×10^{-2}	1.47×10^{-2}
P_m/W·μm^{-1}	17.68×10^{-3}	108.78×10^{-3}

4. Conclusion

In this paper, we propose a high holding voltage SCR with an LN+ layer and an LP+ layer for ESD protection application, and investigate its latch-up effect, current, temperature distribution, and power limitation. A V_h of 7.4 V and V_{t1} of 16.1 V were obtained by optimizing the lengths of L_1 and L_3. The V_h can be adjusted from 6.1 V to 14.6 V by changing the lengths of LN+ and LP+ (L_1 and L_3). According to the simulated results, the proposed SCR can effectively avoid the latch-up effect without causing any degradation in its ESD robustness ($I_{t2} = 1.47 \times 10^{-2}$ A/μm) and improve the P_m from 17.68×10^{-3} W/μm to 108.78×10^{-3} W/μm without additional masks or process steps.

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