Analytical capacitance model for 14 nm FinFET considering dual-*k* spacer*

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The conformal mapping of an electric field has been employed to develop an accurate parasitic capacitance model for nanoscale fin field-effect transistor (FinFET) device. Firstly, the structure of the dual-layer spacers and the gate parasitic capacitors are thoroughly analyzed. Then, the Cartesian coordinate is transferred into the elliptic coordinate and the equivalent fringe capacitance model can be built-up by some arithmetical operations. In order to validate our proposed model, the comparison of statistical analysis between the proposed calculation and the 3D-TCAD simulation has been carried out, and several different material combinations of the dual-*k* structure have been considered. The results show that the proposed analytical model can accurately calculate the fringe capacitance of the FinFET device with dual-*k* spacers.

Keywords: fin field-effect transistor, parasitic capacitance model, conformal mapping, TCAD

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1. Introduction

With complementary metal-oxide semiconductor (CMOS) technology continuously scaling down, the three-dimensional (3-D) fin field-effect transistor (FinFET) device has become the mainstream due to its better electrostatic control and reduced junction capacitance.[1–3] However, not only does the 3-D structure lead to a new electric field distribution in the channel and affect the *I*–*V* characteristics,[4] but also it complicates the parasitic capacitance of the FinFET device. The gate-source/drain parasitic capacitance is gradually dominating the total capacitance of the device,[5–8] and a FinFET structure with dual-*k* spacer will see the more deteriorated influences.[9]

In order to account for the change of the dual-*k* spacer, it is necessary to develop an accurately analytical capacitance model. Several models have been reported. Liu *et al.*[10] proposed a compact model of fringing capacitance for planar MOSFETs. Lee *et al.*[11] provided a parasitic capacitance model for multi-fin tri-gate FinFET by conformal mapping and non-dimensionalization techniques with several fitting parameters. Chauhan *et al.*[12] came up with a common parasitic capacitance model, solving the capacitance by an electromagnetic field approximate calculation. Unfortunately, all of them failed to cover the dual-*k* materials of inter-layer dielectric (ILD) and spacer. The improved approach given by Lacord *et al.*[13,14] adopted the equivalent permittivity to cover the multi-layers materials by approximating the electric fields. However, the singularity in the formula limits its application when the two plates of the capacitor are axial symmetrical. Therefore, the analytical parasitic model for multilayer materials needs to be further explored.

In this paper, an accurate analytical model for 3-D FinFET parasitic capacitance is proposed using the conformal coordinate mapping. The model is geometry-dependent and the different dual-*k* spacer structures are thoroughly analyzed. The modeling strategy of the fringe capacitance is explained in Section 2. The transfer of the Cartesian coordinate to the elliptic coordinate and the modeling of the capacitance for the dual-*k* spacer are discussed in Section 3. Section 4 validates our proposed model by comparing the calculation with the TCAD simulation. The conclusions are given in Section 5.

2. Fringe capacitance considering dual-*k* spacer

As shown in Fig. 1, the parasitic fringe capacitance of the dual-*k* spacer FinFET device can be divided into six parts, including the gate-to-source/drain (S/D) parallel-plate capacitance C_{p0}, the gate-to-fin top capacitances C_{ftop1} and C_{ftop2}, the gate-to-fin side capacitances C_{fside1} and C_{fside2}, and the gate-to-source/drain (S/D) side C_{GEMside}. The total parasitic fringe capacitance of the FinFET device from the gate-to-source/drain can be generalized to

$$C_{\mathrm{f,S/D}} = C_{\mathrm{ftop1}} + C_{\mathrm{ftop2}} + C_{\mathrm{p0}} + 2\left(C_{\mathrm{fside1}} + C_{\mathrm{fside2}} + C_{\mathrm{GEMside}}\right). \quad (1)$$

The different materials of spacer and ILD complicate the variety of the gate around parasitic capacitance. In order to

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achieve accurate modeling of $C_{f,S/D}$, the two-layer structures must be thoroughly analyzed. C_{ftop1}, C_{ftop2}, C_{fside1}, and C_{fside2} are generalized to the vertical structure whose material boundaries adhere to the metal plates. Because $C_{GEMside}$ is only a small proportion of $C_{f,S/D}$, it can be approximated as the generalized vertical structure by replacing ε_1 with ε_2, as shown in Fig. 2. Compared with the total parasitic capacitance, the error from this approximation can be ignored. For the multi-fin structure, the fringe capacitance of gate-to-source/drain is rewritten as

$$\begin{aligned} C_{f,s} = C_{f,d} &= C_{p0} + (N-1)\,C'_{p0} + 2C_{GEMside} \\ &\quad + N\left(C_{ftop1} + C_{ftop2} + 2\left(C_{fside1} + C_{fside2}\right)\right), \end{aligned} \tag{2}$$

where N is the number of fins, and C'_{p0} is the parallel capacitance between two fins. Due to the multi-fins sharing the same raised S/D, the parallel-plate capacitors of C'_{p0} and C_{p0} can be written as

$$\begin{aligned} C_{p0} &= \varepsilon_1 \frac{L_C H_G - (H_{Fin} + T_{ox})(T_{Fin} + 2T_{ox})}{T_{spacer}} \\ &\quad \| \varepsilon_2 \frac{L_C H_G - (H_{Fin} + T_{ox})(T_{Fin} + 2T_{ox})}{D_{C2G} - T_{spacer}}, \end{aligned} \tag{3}$$

$$\begin{aligned} C'_{p0} &= \varepsilon_1 \frac{P_{Fin} H_G - (H_{Fin} + T_{ox})(T_{Fin} + 2T_{ox})}{T_{spacer}} \\ &\quad \| \varepsilon_2 \frac{P_{Fin} H_G - (H_{Fin} + T_{ox})(T_{Fin} + 2T_{ox})}{D_{C2G} - T_{spacer}}, \end{aligned} \tag{4}$$

where P_{Fin} is the fin pitch, L_G is the channel length, H_G is the distance between two top sides from fin to gate, T_{ox} is the oxide thickness, L_C is the S/D width which is smaller than P_{Fin} for $N = 1$, H_{Fin} is the fin height, T_{Fin} is the fin width, D_{C2G} is the distance from the spacer to S/D, and T_{spacer} is the spacer thickness. In general, the parallel capacitor C'_{p0} between two fins is larger than C_{p0} of the single-fin FinFET device because a larger area is introduced, as shown in Fig. 1(b).

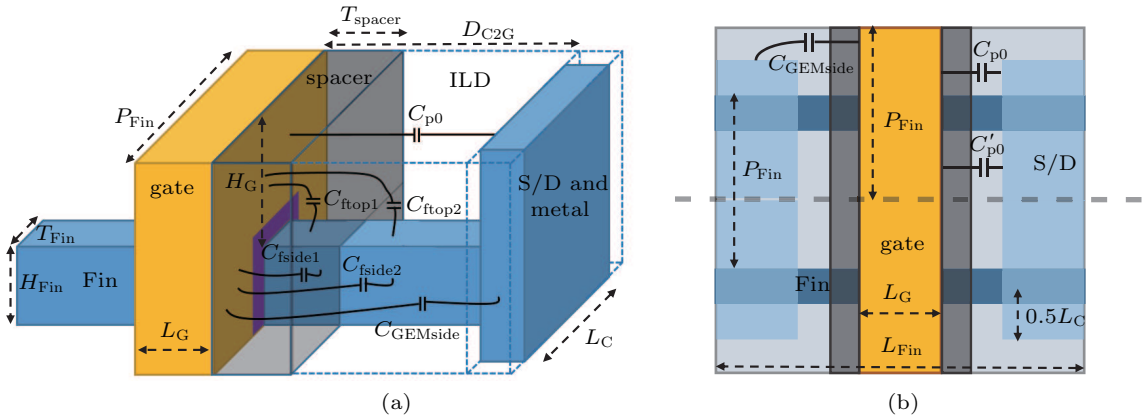


Fig. 1. (color online) (a) Gate fringe capacitance of single-fin FinFET device. (b) Multi-fin structure of FinFET device ($N = 2$).

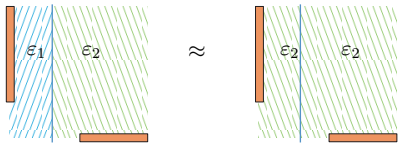


Fig. 2. (color online) Approximation for calculating $C_{GEMside}$.

3. Capacitance modeling

The generalized capacitance mentioned above consists of two parts, as shown in Fig. 3,

$$C = C_{inner} + C_0. \tag{5}$$

C_{inner} and C_0 are formed as the fusiform (purple colored) and elliptic electric field lines, respectively. Both of the confocal and non-confocal cases will be discussed. Here, the confocal condition is defined as

$$\left|x_1^2 - y_1^2\right| = \left|x_2^2 - y_2^2\right| = f^2, \tag{6}$$

where f is the focus length, and $(x_2 - x_1)$ and $(y_2 - y_1)$ represent the lengths of two plates.

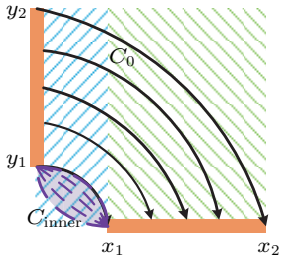


Fig. 3. (color online) Generalized capacitor includes two parts.

3.1. Confocal capacitance structure

The Cartesian coordinate system can be built-up referring to the two vertical metal plates, as shown in Fig. 4.

3.1.1. Capacitance C_0

The bent electric field lines shown in Fig. 4(a) can be transferred into the straight counterparts shown in Fig. 4(b) us-

ing a coordinate transformation. Then, the fringe capacitance can be formulated using the parallel-plate form. The distances from x_1 and y_1 to the coordinate origin decide the location of the ellipse focus, on either the Y-axis or the X-axis. The bent electrical lines (x_1, y_1, x_2, y_2) in the first quadrant can be transformed. The following mapping can be applied:[15]

$$x = f\cosh\mu\cos\nu, \tag{7}$$

$$y = f\sinh\mu\sin\nu. \tag{8}$$

As shown in Fig. 4(a), the point $A(x_1, y_A)$ indicates the cross point of the field line and the material boundary. There is

$$\nu_A = \arccos\left\{\left[\left(\frac{x_1}{f}\right)^2+\left(\frac{y_A}{f}\right)^2+1-\sqrt{\left(\left(\frac{x_1}{f}\right)^2+\left(\frac{y_A}{f}\right)^2+1\right)^2-4\left(\frac{x_1}{f}\right)^2}\right]\Big/2\right\}^{1/2}, \tag{9}$$

$$\mu_2-\mu_1 = \ln\left(\frac{y_2+\sqrt{\left(x_1^2+(y_2-y_1)^2+2y_1(y_2-y_1)\right)}}{x_1+y_1}\right) = \ln\left(\frac{x_2+y_2}{x_1+y_1}\right). \tag{10}$$

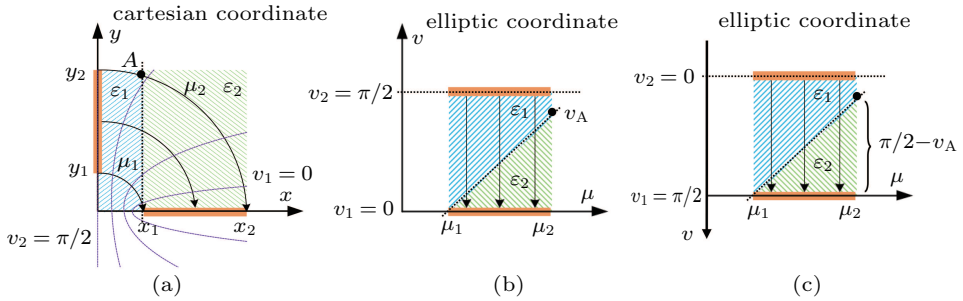


Fig. 4. (color online) Deducing C_0 capacitor model with conformal mapping approach. (a) The C_0 capacitor structure in Cartesian coordinate when $x_1 > y_1$. (b) The C_0 structure in transformed elliptic coordinate when $x_1 > y_1$. (c) The structure in transformed elliptic coordinate when $x_1 < y_1$.

Note that the equivalent cross points of the electrical lines are approximated to be on a straight line. With the help of differential quadrature element method (DQEM), the capacitance element can be considered as two capacitors connected in series as

$$\mathrm{d}C = W\left(\varepsilon_0\varepsilon_2\frac{\mathrm{d}\mu}{\frac{\nu_A(\mu-\mu_1)}{\mu_2-\mu_1}}\right) \Big|\Big| \left(\varepsilon_0\varepsilon_1\frac{\mathrm{d}\mu}{\frac{\pi}{2}-\frac{\nu_A(\mu-\mu_1)}{\mu_2-\mu_1}}\right), \tag{11}$$

where ε_0 is the vacuum permittivity, ε_1 and ε_2 are the relative dielectric constants of the spacer and ILD, respectively, and W is the width of the capacitor in z-direction. Integrating the capacitance of C_0 from μ_1 to μ_2 leads to (in units of F)

$$C_0 = \int_{\mu=\mu_1}^{\mu=\mu_2}\mathrm{d}C$$

$$= W\frac{\varepsilon_2\varepsilon_1\varepsilon_0}{(\varepsilon_1-\varepsilon_2)\nu_A}\ln\left(\frac{2}{\pi}\left(\frac{(\varepsilon_1-\varepsilon_2)\nu_A}{\varepsilon_2}\right)+1\right) \times\ln\left(\frac{x_2+y_2}{x_1+y_1}\right). \tag{12}$$

If the ILD and spacer have the same permittivity, then equation (12) can be simplified as

$$C_{0,\mathrm{single}-k} = \lim_{(\varepsilon_1-\varepsilon_2)\to 0}C_0 = W\frac{\varepsilon_2\varepsilon_1\varepsilon_0}{(\varepsilon_1-\varepsilon_2)\nu_A}\frac{2}{\pi}\left(\frac{(\varepsilon_1-\varepsilon_2)\nu_A}{\varepsilon_2}\right)\ln\left(\frac{x_2+y_2}{x_1+y_1}\right) = W\frac{2\varepsilon_1\varepsilon_0}{\pi}\ln\left(\frac{x_2+y_2}{x_1+y_1}\right). \tag{13}$$

Again, consider that the ellipse focus is on the Y-axis, giving $x_1 < y_1$. Due to the symmetry of x and y in the above formulas, after the exchange of x and y in Eqs. (7) and (8), the transformed coordinates are shown in Fig. 4(c), and the updated ν'_A is rewritten as

$$\nu'_A = \frac{\pi}{2}-\nu_A|_{x,y,\ \mathrm{exchange}} = \arcsin\left\{\left[\left(\frac{x_1}{f}\right)^2+\left(\frac{y_A}{f}\right)^2+1-\sqrt{\left(\left(\frac{x_1}{f}\right)^2+\left(\frac{y_A}{f}\right)^2+1\right)^2-4\left(\frac{y_A}{f}\right)^2}\right]\Big/2\right\}^{1/2}. \tag{14}$$

Therefore, C_0 can be obtained by Eq. (12). Depending on $x_1 < y_1$ or $x_1 > y_1$, either equation (9) or (14) will be chosen to calculate ν_A.

3.1.2. Capacitance C_{inner}

For the inner corner part, giving $x < x_1$ and $y < y_1$, the electric field lines are neither elliptical nor straight, shown as the part close to the corner in Fig. 5. For simplicity, the equivalent capacitor is considered as a parallel structure whose dielectric thickness is approximated as the distance between these two plates, denoted as L. Therefore, $D/2$ is the maximum distance between the marked line $(y_1x+x_1y-x_1y_1=0)$ and ellipse $(x=x_1\cos\theta,\ y=y_1\sin\theta)$ in the first quadrant, as shown in Fig. 5. The maximum distance between the outermost electric field lines is defined as D. Given a fixed L, the electronic field is affected by D and written as

$$L = \sqrt{x_1^2+y_1^2}, \tag{15}$$

$$\begin{aligned} D &= 2\max\left(\frac{y_1x_1\cos\theta+x_1y_1\sin\theta-x_1y_1}{\sqrt{x_1^2+y_1^2}}\right) \\ &= \frac{2(\sqrt{2}-1)x_1y_1}{\sqrt{x_1^2+y_1^2}}, \end{aligned} \tag{16}$$

where θ is the phase angle of the ellipse coordinate. Therefore, the inner capacitance can be calculated as (in units of F)

$$\begin{aligned} C_{inner} &= W\frac{\varepsilon_0\varepsilon_1 D}{L}\lambda_1 \\ &= W\frac{\varepsilon_0\varepsilon_1 2(\sqrt{2}-1)x_1y_1}{x_1^2+y_1^2}\lambda_1, \end{aligned} \tag{17}$$

where λ_1 is a fitting factor and W is the width of the capacitor in z-direction. Combining Eqs. (12) and (17), we can calculate the parasitic fringe capacitance of the dual-k spacer for a FinFET device.

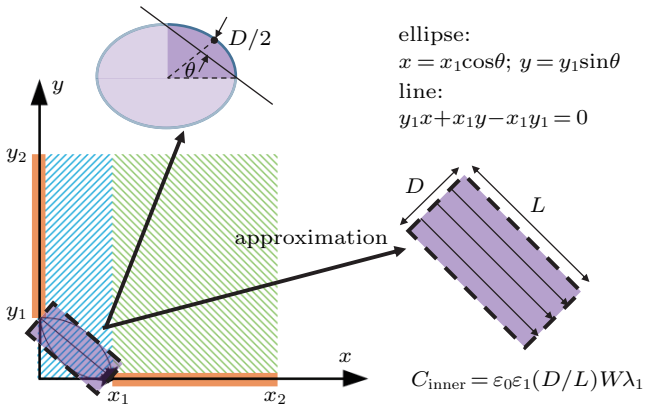


Fig. 5. (color online) Deducing capacitance C_{inner} with approximation approach.

3.2. Non-confocal condition model

Besides the confocal case, the non-confocal case is more general where (x_1, y_1, x_2, y_2) does not satisfy the confocal requirement of Eq. (6). The model under confocal should be extended to be suitable for the non-confocal situation. As shown in Fig. 6, x_2 and y_2 are replaced by the effective counterparts $x_{2,eff}$ and $y_{2,eff}$ when calculating the capacitance C_0. Here, $x_{2,eff}$ and $y_{2,eff}$ satisfy the confocal condition, and they are expressed as

$$x_1^2-y_1^2 = x_{2,eff}^2-y_{2,eff}^2 = f^2. \tag{18}$$

The non-confocal can be thought of as a confocal part and an extra part occupied by the dotted lines. According to Fig. 6, in order to make the confocal part largest, the effective lengths should be calculated by

$$x_{2,eff} = \min\left(x_2, \sqrt{y_2^2-y_1^2+x_1^2}\right), \tag{19}$$

$$y_{2,eff} = \min\left(y_2, \sqrt{x_2^2-x_1^2+y_1^2}\right). \tag{20}$$

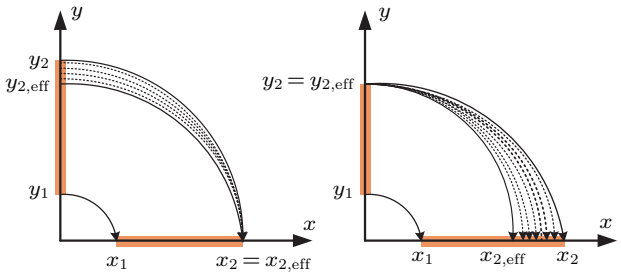


Fig. 6. (color online) Two different non-confocal structures.

For instance, giving $x_1 = 0.1$, $y_1 = 0.2$, $x_2 = 0.3$, and $y_2 = 0.4$, the effective lengths are written as $x_{2,eff} = x_2 = 0.3$, $y_{2,eff} = \sqrt{0.12} \approx 0.3464$. In view of the non-confocal impact, the factor k_{delta} is introduced to reflect the extra part, written as

$$k_{delta} = 1+\frac{x_1^2+y_1^2}{x_2^2+y_2^2}\left(\frac{x_2-x_{2,eff}}{x_{2,eff}}+\frac{y_2-y_{2,eff}}{y_{2,eff}}\right)\lambda_2, \tag{21}$$

where λ_2 is a fitting factor. Equation (3) can be written as

$$C = C_{inner}+C_0k_{delta}. \tag{22}$$

Combining Eqs. (10), (17), and (21) into Eq. (22), we can obtain the general expression of the fringe capacitance component

$$\begin{aligned} C &= W\frac{\varepsilon_0\varepsilon_1 2\left(\sqrt{2}-1\right)x_1y_1}{x_1^2+y_1^2}\lambda_1 \\ &\quad +W\frac{\varepsilon_2\varepsilon_1\varepsilon_0}{(\varepsilon_1-\varepsilon_2)\nu_A}\ln\left(\frac{2}{\pi}\left(\frac{(\varepsilon_1-\varepsilon_2)\nu_A}{\varepsilon_2}\right)+1\right) \\ &\quad \times\ln\left(\frac{x_{2,eff}+y_{2,eff}}{x_1+y_1}\right) \\ &\quad \times\left(1+\frac{x_1^2+y_1^2}{x_2^2+y_2^2}\left(\frac{x_2-x_{2,eff}}{x_{2,eff}}+\frac{y_2-y_{2,eff}}{y_{2,eff}}\right)\lambda_2\right). \end{aligned} \tag{23}$$

Table 1 summarizes all corresponding parameters for the proposed model of the generalized vertical structures. Therefore, by substituting Eq. (23) into Eq. (2) and using Table 1, we can calculate the total parasitic capacitance of the FinFET device.

Table 1. Parameters for FinFET parasitic capacitors.

Capacitor	C_{ftop1}	C_{ftop2}	C_{fside1}	C_{fside2}	C_{GEMside}
ε_1	spacer	spacer	spacer	spacer	ILD
ε_2	spacer	ILD	spacer	ILD	ILD
x_1	0	T_{Spacer}	0	T_{Spacer}	T_{Spacer}
x_2	T_{Spacer}	D_{C2G}	T_{Spacer}	D_{C2G}	$0.5(L_{\text{Fin}}-L_{\text{G}})$
y_1	T_{ox}	T_{ox}	T_{ox}	T_{ox}	0
y_2	H_{G}	H_{G}	$0.5(P_{\text{Fin}}-T_{\text{Fin}})$	$0.5(P_{\text{Fin}}-T_{\text{Fin}})$	$0.5(P_{\text{Fin}}-L_{\text{C}})$
W	T_{Fin}	T_{Fin}	H_{Fin}	H_{Fin}	$H_{\text{G}}+H_{\text{Fin}}$

3.3. Extraction of λ_1 and λ_2

The parameters λ_1 and λ_2 can be extracted by linear regression. Because equation (23) is a linear function of λ_1 and λ_2, the expression of λ_1 and λ_2 can be deduced, as shown in Fig. 7. Firstly, λ_2 can be removed by choosing the confocal structure to set $A_3 = 0$. Then, the left λ_1 can be extracted by fitting the simulation results. Secondly, once λ_1 is obtained we can substitute it into the non-confocal cases to extract λ_2. All the extracted λ_1 and λ_2 are appended in Fig. 9.

$$C = \underbrace{W\frac{\varepsilon_0\varepsilon_1\cdot 2(\sqrt{2}-1)x_1y_1}{x_1^2+y_1^2}}_{A_1}\lambda_1 + \underbrace{W\frac{\varepsilon_2\varepsilon_1\varepsilon_0}{(\varepsilon_1-\varepsilon_2)\nu_A}\cdot\ln\left(\frac{2}{\pi}\left(\frac{(\varepsilon_1-\varepsilon_2)\nu_A}{\varepsilon_2}\right)+1\right)\cdot\ln\left(\frac{x_{2,\text{eff}}+y_{2,\text{eff}}}{x_1+y_1}\right)}_{A_2} \times\left(1+\underbrace{\frac{x_1^2+y_1^2}{x_2^2+y_2^2}\cdot\left(\frac{x_2-x_{2,\text{eff}}}{x_{2,\text{eff}}}+\frac{y_2-y_{2,\text{eff}}}{y_{2,\text{eff}}}\right)}_{A_3}\cdot\lambda_2\right)$$

$$C=\lambda_1\cdot A_1+\lambda_2\cdot A_2A_3+A_2$$

confocal: $\lambda_1=\dfrac{C-A_2}{A_1}$

non-confocal: $\lambda_2=\dfrac{C-A_2-\lambda_1A_1}{A_2A_3}$

Fig. 7. (color online) Extraction procedure of λ_1 and λ_2.

4. Model validation and analysis

In order to validate our proposed model, the comparisons between the calculation and the TCAD numerical simulation have been carried out.[16] The validations consist of the single vertical dual-k capacitor and the total FinFET parasitic capacitance. Several materials are considered, including the default nitride ($\varepsilon_r = 7.5$), high-k HfO_2 ($\varepsilon_r = 22$), SiO_2 ($\varepsilon_r = 3.9$), and low-k SiO_2 ($\varepsilon_r = 2.5$) ILD.

In order to extract the total parasitic capacitance $C_{\text{total}} = C_{\text{f,s}} + C_{\text{f,d}}$, TCAD AC simulations of 3-D FinFET have been carried out. During the simulations, the fins are replaced by a metal strip to omit other capacitors of the device. The snapshot of the simulated structures and schematic are shown in Fig. 8. C_{total} can be obtained by subtracting C_{ox} from C_{gg}. The 14 nm technology node is chosen for the validation of our proposed model. Table 2 shows the default parameters of 14 nm FinFET device.[17,18]

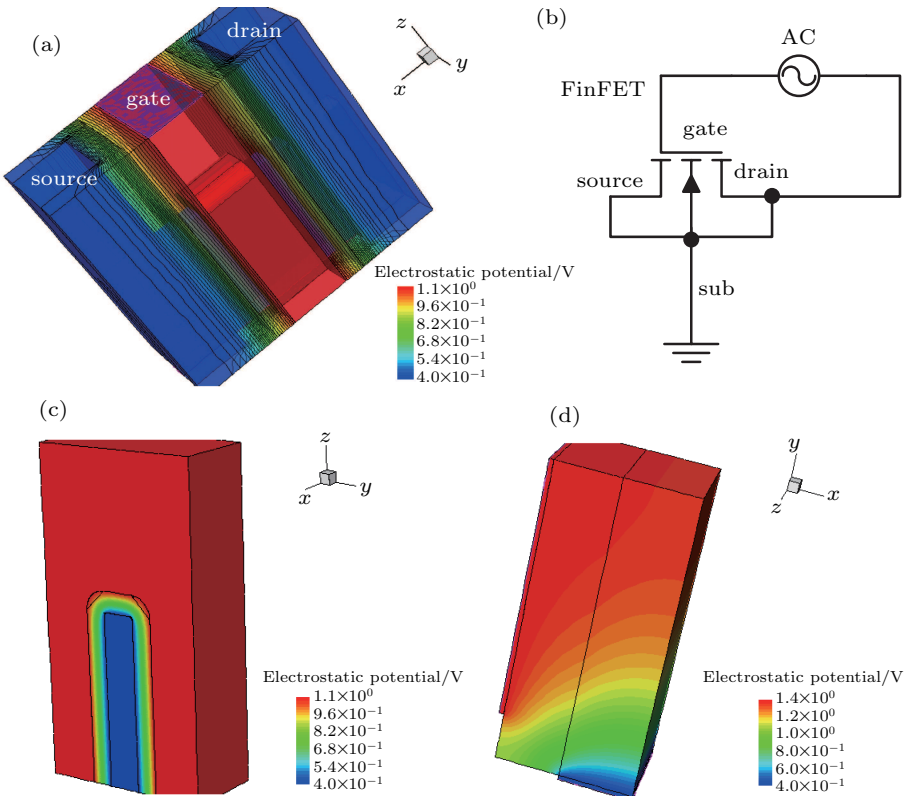


Fig. 8. (color online) (a) Snapshot of total simulation structure. (b) Equivalent schematic. (c) C_{ox} simulation structure. (d) Simulation structure of C_{fside1}, C_{fside2}, C_{ftop1}, C_{ftop2}, and C_{GEMside}.

Table 2. Default parameters of 14 nm FinFET.

Parameter	Value
L_G	20 nm
H_G	38 nm
T_{Fin}	8 nm
H_{Fin}	42 nm
P_{Fin}	42 nm
EOT	0.9 nm
T_{ox}	5.08 nm
D_{C2G}	15 nm
L_C	26 nm
L_{Fin}	90 nm
T_{Spacer}	7 nm
Gate oxide material	HfO_2 ($\varepsilon_r = 22$)
Spacer material	nitride ($\varepsilon_r = 7.5$)
ILD material	SiO_2 ($\varepsilon_r = 3.9$)

The results in Fig. 9 validate the model accuracy in different material combinations condition, including both the same and different materials. The relative errors between the numerical simulation with TCAD and our model are shown. In each subfigure, 500 simulation cycles have been carried out with randomized x_1, y_1, x_2–x_1, y_2–y_1, which independently and evenly distributed between 5 nm and 50 nm. This means that all the confocal and non-confocal conditions are covered. The most left-top subfigure shows the result of the same material ($\varepsilon_1 = \varepsilon_1 = 2.5$) adopted in the spacer and ILD. The related fitting parameters λ_1 and λ_2 are 0.7 and 2.07, respectively, and the standard deviation (σ) of the relative error is 3.51%. The

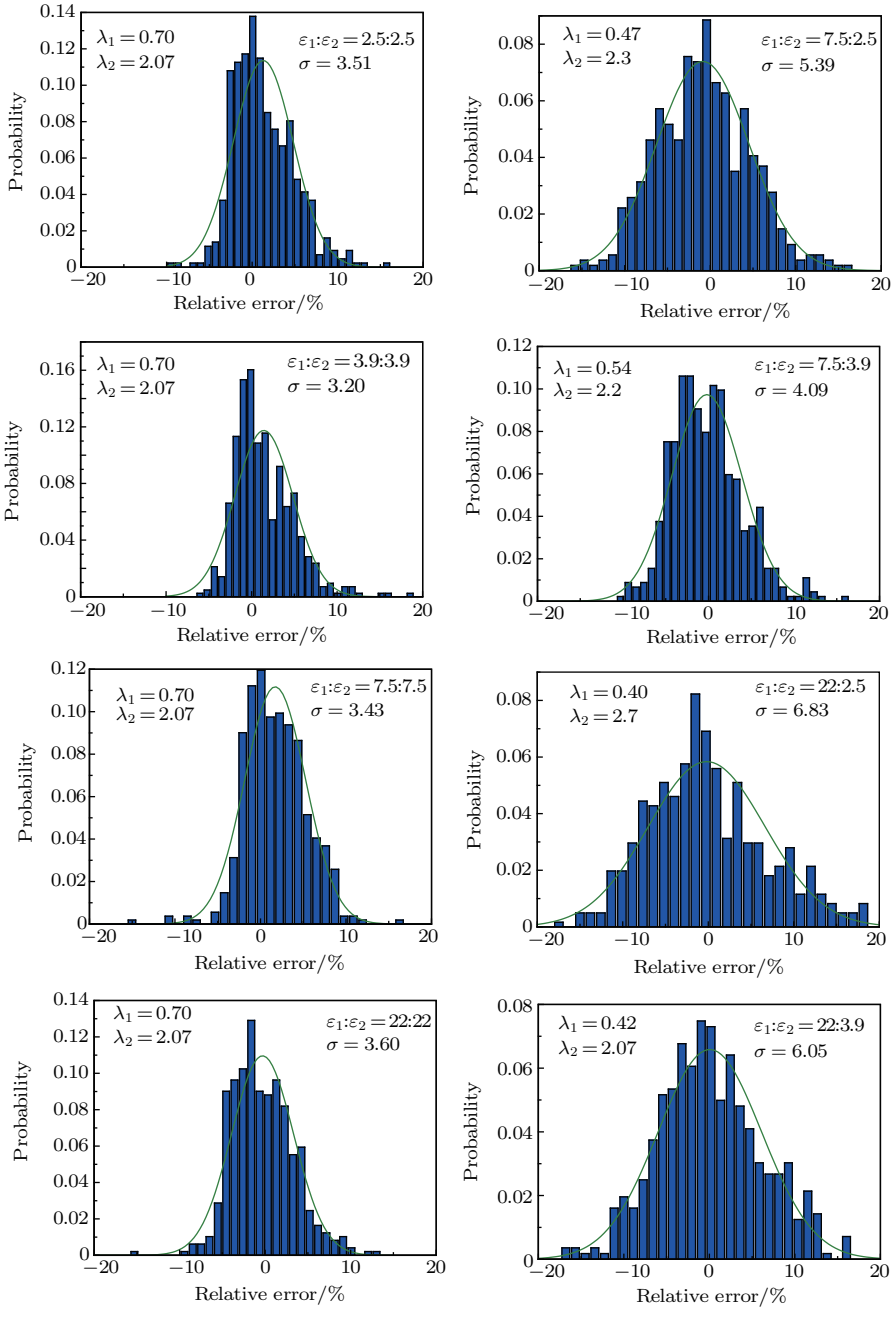


Fig. 9. (color online) Validation and comparison between the statistical simulation and model calculation.

right-top subfigure is based on different materials ($\varepsilon_1 = 7.5$ and $\varepsilon_2 = 2.5$), where the fitted λ_1 and λ_2 are 0.47 and 2.3, and the σ of the relative error is 5.39%. Comparing the lefts with the rights, we can find that the combinations of different materials have larger σ. All the relative errors fall within $\pm 15\%$, and the minimum and maximum σ of these different cases are 3.20 and 6.83, respectively. The errors become larger as the permittivity difference between the two materials increases. The approximation of materials' boundary in the elliptic coordinate and concise non-confocal treatment may be the causes.

Figure 10(a) shows that the parasitic capacitance is almost constant under varied fin width. The reason can be found in Fig. 10(b), which implies that the loss of $C_{\rm p0}$ is compensated by the increasing $C_{\rm ftop}$ with the increasing fin width. The increase of the spacer thickness from 3 nm to 10 nm can bring a relatively large change in $C_{\rm f,S/D}$, as shown in Fig. 10(c). The varied fin height and gate height maintain the similar slope for different material combinations, as shown in Figs. 10(d) and 10(e). Figures 10(f) and 10(g) indicate the influences of the fin pitch and fin number on the parasitic capacitance. Among the above parameters of FinFET, except the fin number, the parasitic capacitance is more sensitive to the spacer thickness than the others, especially for high-k spacer materials. It can be concluded that good agreement between our model and TCAD numerical simulation is obtained, even if the fin number, spacer thickness, gate height, fin pitch, or fin number is varied.

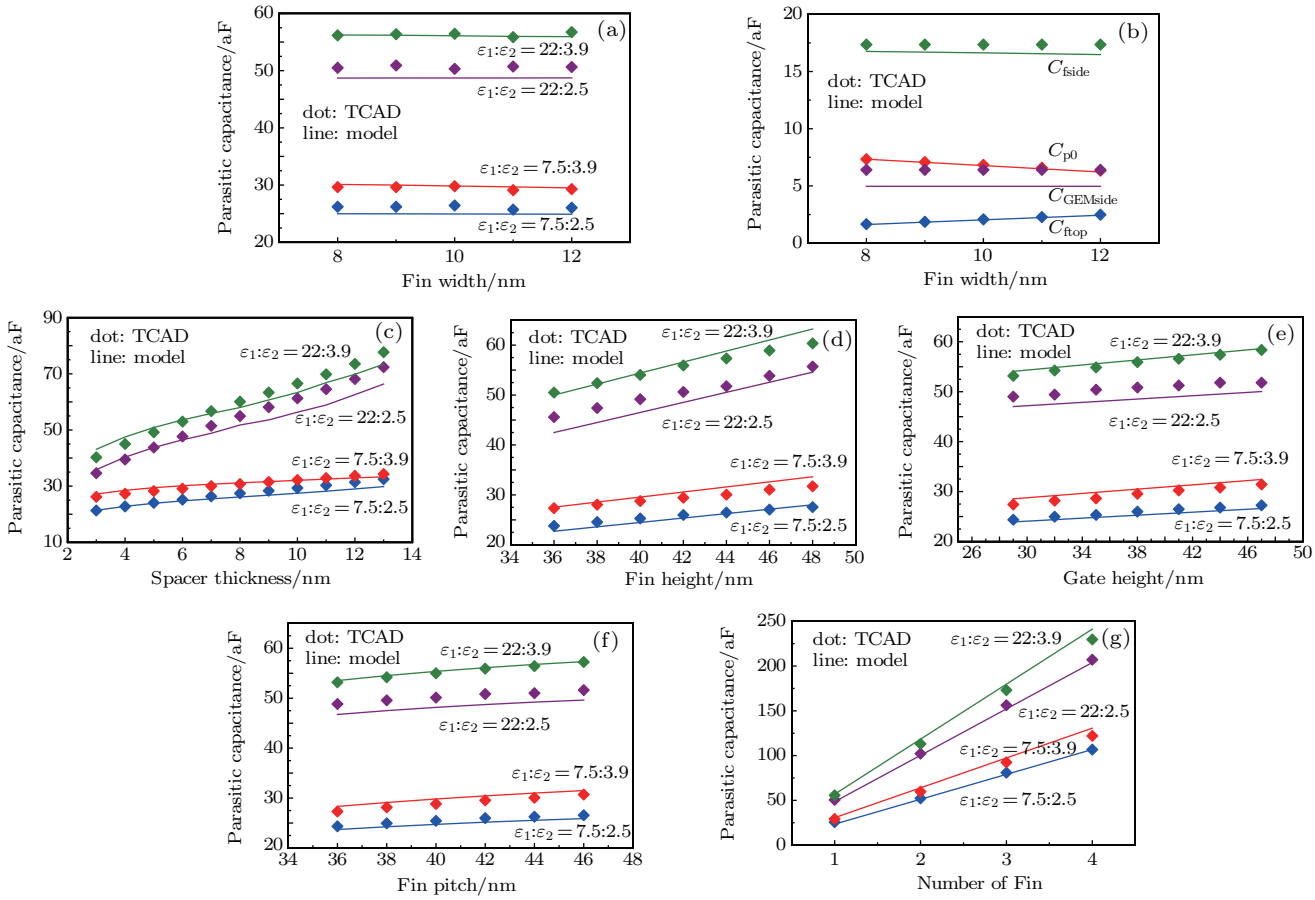


Fig. 10. (color online) Parasitic capacitance of FinFET with various (a), (b) fin width, (c) spacer thickness, (d) fin height, (e) gate height, (f) fin pitch, and (g) fin number.

5. Conclusion

An accurate analytical model of FinFET parasitic capacitance has been proposed. Not only does it cover the dual-k materials of ILD and spacer, but also it breaks the limitation in the previous capacitance model of dual-k materials. Moreover, only two fitting parameters are introduced. TCAD numerical simulations demonstrate the validation of our proposed model for FinFET parasitic capacitance.

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