Stable single-mode operation of 894.6 nm VCSEL at high temperatures for Cs atomic sensing*

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(Received 21 February 2017; revised manuscript received 21 March 2017; published online 6 June 2017)

In this paper, stable single-mode operation at high temperatures is produced by the surface-relief-integrated vertical cavity surface emitting laser (VCSEL). The gain-cavity mode detuning technique is employed to realize high operating temperatures for the VCSEL. The surface relief is etched in the centre of the top side as a mode discriminator for the fundamental mode output, and the threshold current minimum is 1.94 mA at high temperatures by the gain-cavity mode detuning technique. Maximum single-fundamental-mode output power of 0.45 mW at 80 °C is obtained, and the side mode suppression ratios (SMSRs) are more than 30 dB with increasing temperature and current, respectively.

Keywords: single-mode operation, surface relief, gain-cavity mode detuning, vertical cavity surface emitting laser (VCSEL)

PACS: 42.55.Px, 42.60.Jf, 42.62.Fi **DOI:** 10.1088/1674-1056/26/7/074209

1. Introduction

Vertical cavity surface emitting lasers (VCSELs) offer unique advantages over other laser structures, such as beam quality, wafer-level testing, small power consumption, and low threshold current.[1] Single mode VCSELs are of interest for applications in micro positioning navigation timing, chip-scale atomic clocks (CSACs), and the atomic gyroscope system.[2–4] For Cs atomic sensing, stable single mode operation of 894.6 nm VCSELs at high temperatures must be guaranteed, because the Cs atomic sensor must operate above 80 °C and the CPT effect of the Cesium D1 line must be motivated by 894.6 nm.[5] For conventional VCSELs, the oxide aperture diameter is limited to 3 μm to achieve single fundamental modes.[6–8] Unfortunately, limited oxide apertures will cause limited output powers and large resistances, consequently limiting their applications. With the increasing ambient temperature, the emission wavelength of the VCSELs will be red-shifted, which is detrimental for Cs atomic sensing. Therefore, several structures have been developed for single-mode high-power VCSELs, such as the proton-implanted structure.[9] the small oxide-confined structure,[10] the metal aperture,[11] the photonic crystal structure,[12,13] the triangular-hole structure,[14,15] and the surface relief structure.[16] In this paper, a novel surface relief VCSEL (SR-VCSEL) based on gain-cavity mode detuning technology is produced. In the novel SR-VCSEL, the gain-cavity mode detuning solves the emission wavelength shift problem, and the shallow-etched surface relief structure serves as a mode discriminator in order to suppress higher-order modes. This structure does not impair the electrical or thermal features of the VCSEL, which is significant for the applications of Cs atomic sensing.

2. Simulation and experiment

2.1. Device model and simulation

The transverse optical confinement factor $\Gamma_{\mathrm{trans},01}$ that determines the modal gain is expressed as

$$\Gamma_{\mathrm{trans},01} = \frac{\int_0^a \int_0^{2\pi} E_{01}^2 r \mathrm{d}\Phi \mathrm{d}r}{\int_0^\infty \int_0^{2\pi} E_{01}^2 r \mathrm{d}\Phi \mathrm{d}r},$$

where E_{01} is the electric field amplitude of the LP_{01} mode, and a is the radius of the VCSEL mesa. The fundamental mode LP_{01} has the highest modal gain, but for higher-order modes (LP_{11}, LP_{21}) the modal gain decreases with elevated mode order, which provides mode selectivity to obtain the fundamental mode. According to the relationship between the transverse mode distribution and the diameter of the optical field of the 7 μm oxide-confined VCSEL, the junction of LP_{01} and LP_{11}, LP_{21} is a key parameter. The higher-order modes are mainly distributed in the annular region, and the fundamental mode is mainly distributed in the central region; the diameter of the

*Project supported by the National Natural Science Foundation of China (Grant Nos. 61434005, 61474118, 11674314, 51672264, and 11404326), the Science and Technology Program of Jilin Province, China (Grant No. 20150203011GX), the Science and Technology Program of Changchun City, China (Grant No. 15SS02), and the Youth Innovation Promotion Association of China (Grant No. 2017260).

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surface relief is set to be 3 μm. In this work, we use the transfer matrix to calculate the mirror loss of the VCSEL structures. By calculating the reflectivity of the p-side of our VCSEL structure with different etching depths, the relationship of the mirror loss versus the etched depth can be obtained, as shown in Fig. 1. Due to the periodic nature of the phase variations, when a layer of about 0.5 (110 nm) or 1.5 (247 nm) pairs of P-DBRs has been removed, the mirror loss reaches a maximum. Thus, the etched regions have a maximum threshold gain and increase the losses of higher-order modes. By removing the higher-order top layer, the higher-order modes can be suppressed and the LP_{01} mode area preserved through shallow etching.

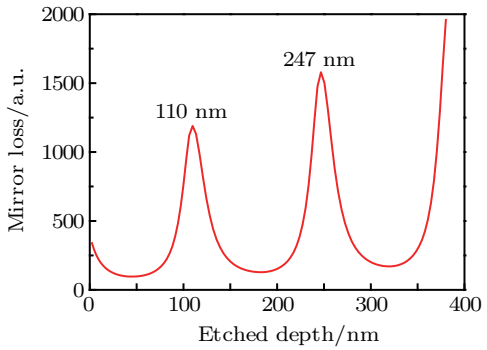


Fig. 1. (color online) Simulation result of mirror loss versus etched depth for the surface-etch 894.6 nm VCSEL.

Figure 2 illustrates the gain-cavity mode detuning technique in structural design. We can see that the temperature dependence of the cavity mode (the black line) and the gain peak wavelengths (the red line) are 0.06 and 0.3 nm/K, respectively. Therefore, with the negative gain-cavity detuning, the gain peak wavelength approaches the cavity mode in the initial heating stage, and then exceeds the cavity mode in the later heating process. As a result, the cavity mode gain (the blue line) increases at first and then decreases with the elevated temperatures. As the threshold current is inversely proportional to the cavity mode gain, the minimum threshold current would occur at the maximum of the cavity mode gain.

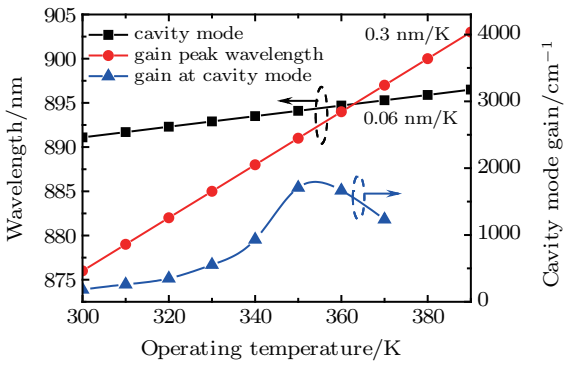


Fig. 2. (color online) The relationship between the cavity mode and gain peak wavelengths under different temperatures. The blue line indicates the cavity mode gain at different temperatures.

2.2. Device structure and fabrication

Figure 3 shows the cross-section structure of the surface relief VCSEL (Fig. 3(a)) and the conventional VCSEL (Fig. 3(b)). The epitaxial semiconductor structure of the 894.6 nm VCSEL is grown on GaAs substrate by metal-organic chemical vapour deposition (MOCVD). The active region contains three InGaAs strained quantum wells to provide optical gain, the bottom distributed Bragg reflector (N-DBR) and the top DBR consist of 34 and 22.5 pairs of high-index $Al_{0.12}Ga_{0.88}As$ and low-index $Al_{0.9}Ga_{0.1}As$ layers, respectively. In addition, a 30-nm-thick $Al_{0.98}Ga_{0.02}As$ layer is inserted between the active region and the p-DBR.

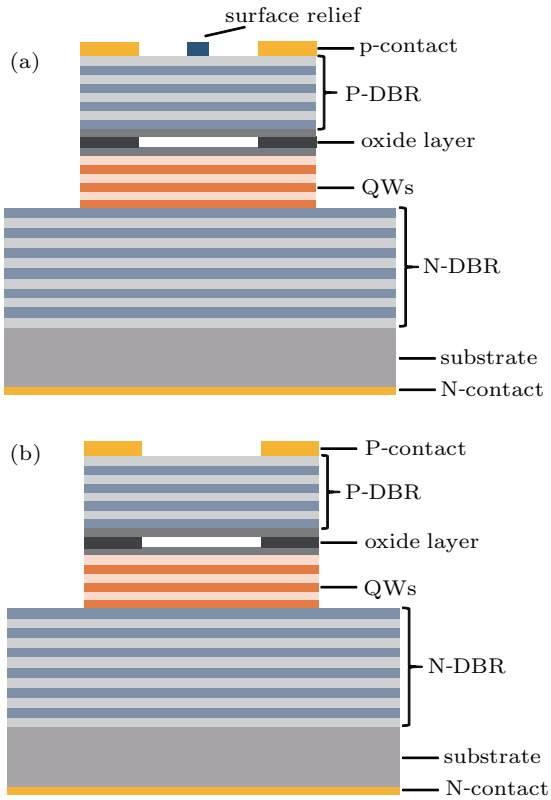


Fig. 3. (color online) Schematic cross section of surface relief VCSEL structure (a) and the conventional VCSEL structure (b).

Using SiO_2 as the etching mask, the top DBR is patterned as a circular post by inductively coupled plasma reaction ion etching (ICP-RIE). To achieve the current and light confinement, a 7-μm-diameter oxide aperture is formed by selective oxidization of the $Al_{0.98}Ga_{0.02}As$ layer. The positive electrode (Ti/Pt/Au) contact is formed on the top side after oxidation to realize ohmic contact. After that, the diameter of the surface relief is 3 μm, which is introduced into the central region on the top by one additional lithography step. Then, 1.5 pairs, (247 nm) of DBRs are etched by wet chemical etching ($CH_3OH:H_3PO_4:H_2O_2:H_2O = 6:1:1:30$) and the diameter of the etched surface relief ring is 10 μm. Finally, the n-contact (Au/Ge/Ni) is formed at the bottom of the substrate, and annealed by rapid thermal annealing at 400 °C.

3. Results and discussion

Figure 4 shows the mode characteristics of SR and conventional VCSEL, which are measured under the continuous-wave (CW) condition at room temperature. The optical spectra of the conventional VCSEL (Fig. 4(a)) shows numerous peaks at different driving currents, which means more modes appear and no significant fundamental mode is obtained. However, the optical spectra of the SR-VCSEL (Fig. 4(b)) always stay at a single peak state: the fundamental mode is still dominating and no more modes appear with increasing currents. The side mode suppression ratio (SMSR) reaches 35 dB throughout the whole current operating range. With increasing driving current above the threshold, current leakage and carrier effects, as well as increased non-radiative recombination, would lead to wavelength red-shift. The comparison of Fig. 4(a) and Fig. 4(b) proves that shallow surface relief provides mode selectivity to obtain the fundamental mode, and higher-order modes can be effectively suppressed.

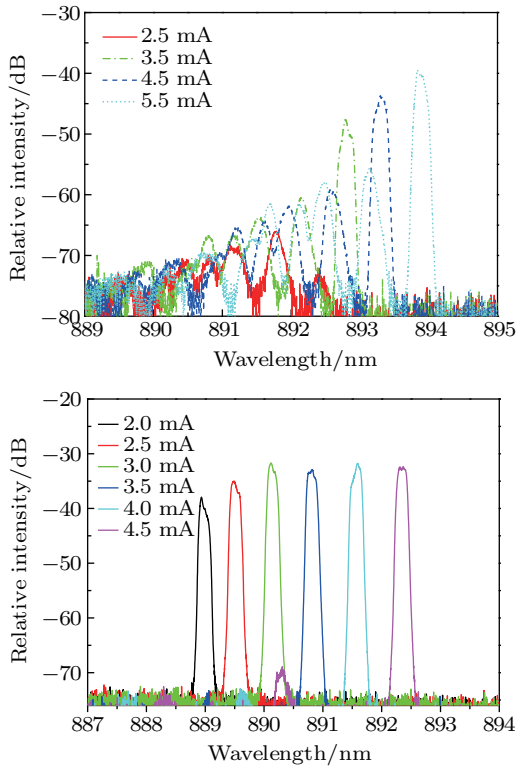


Fig. 4. (color online) (a) The spectra of the conventional VCSEL at different driving currents; (b) the surface relief VCSEL at different driving currents.

The temperature dependences of the spectrum characteristics are shown in Fig. 5. As predicted from simulations, the fundamental mode has most of its field intensity in the unetched areas, and higher-order modes experience higher cavity loss in the etched areas, thereby being suppressed. In this work, single-mode operations with side mode suppression ratios (SMSR) greater than 30 dB at different temperatures are realized. The temperature dependences of the spectrum characteristics further prove that SR-VCSELs can help to achieve stable single modes.

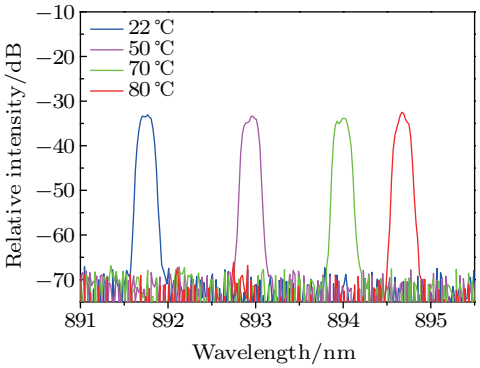


Fig. 5. (color online) The spectra of SR-VCSEL at different temperatures of 22 °C, 50 °C, 70 °C, and 80 °C. The operating current is 4 mA.

Figure 6 shows the power-current characteristics of the SR-VCSEL under different temperatures. The device exhibits a maximum output power of 0.45 mW at 80 °C, and the maximum output power gradually declines as the ambient temperature rises from 22 °C to 90 °C; meanwhile, thermal roll-over occurs earlier with the elevated driving current. It can be seen that the linear increase of the power-current curve has some slight deviation. The main reason is that the SR-VCSEL needs higher carrier densities to maintain the threshold gain, so the carrier and current leakage effects lead to this deviation; increasing non-radiative recombination would be responsible for the deviation with higher carrier densities.[17]

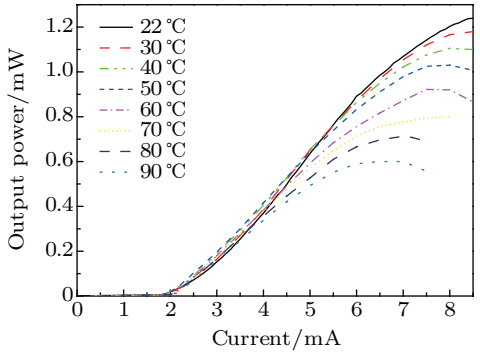


Fig. 6. (color online) The light-current characteristics of SR-VCSEL under the continuous wave condition at different temperatures.

The SR-VCSEL shows excellent wavelength performance and low threshold current owing to the gain-cavity mode detuning technique in the structural design. As shown in Fig. 7, the red line illustrates the red-shift of the emission wavelength, and the blue line represents the threshold current that varies with changing temperature. In order to reduce the threshold current, the cavity mode should receive the maximum optical gain, as simulations predicted. The threshold current exhibits a distinct minimum value of 1.94 mA when the substrate temperature is 50 °C. The threshold current of

the VCSELs usually varies with temperature and can be expressed by[18]

$$I_{\rm th}(T) = I_{\rm th,min}[1 + C_{\rm T}(T - T_{\rm min})^2],$$

where $C_{\rm T} > 0$, the threshold current will increase rapidly, no matter whether above or below $T_{\rm min}$. As a result, the temperature-dependent detuning effect has to be taken into account in the design. As the ambient temperature increases, the peak wavelength appears red-shifted mainly because of the changing average refractive index and the thermal expansion of the semiconductor layers, which would affect the thermal wavelength shift. On the other hand, the energy bandgap of semiconductor materials varies with the change in temperature; the bandgap shrinkage of quantum wells is also responsible for the red-shift.[19]

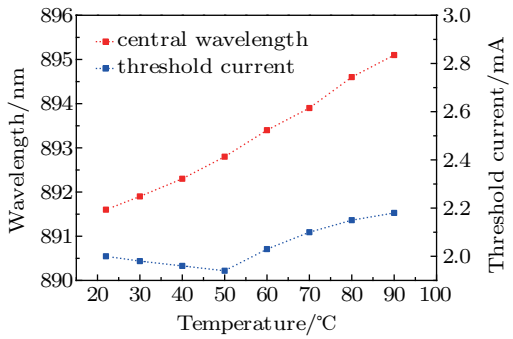


Fig. 7. (color online) (Blue) Threshold current and (red) central wavelength under the operating current of 4 mA versus different temperatures.

4. Conclusion

In summary, a surface relief structure is used to control single-mode characteristics effectively, and the low threshold current of SR-VCSEL at high temperatures is demonstrated for Cs atomic sensing applications. Numerical analysis and experimental results demonstrate that the shallow surface relief provides mode selectivity to obtain the fundamental mode and suppresses higher-order modes. Measurements reveal that at the CW condition, the single-mode output power is 0.45 mW with an SMSR greater than 30 dB at high temperatures. The threshold current minimum is 1.94 mA at 50 °C, which is beneficial for low power consumption. With further optimized structural parameters, higher performance SR-VCSELs are expected.

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