Design and characterization of a 3D encapsulation with silicon vias for radio frequency micro-electromechanical system resonator*

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In this paper, we present a three-dimensional (3D) vacuum packaging technique at a wafer level for a radio frequency micro-electromechanical system (RF MEMS) resonator, in which low-loss silicon vias is used to transmit RF signals. Au–Sn solder bonding is adopted to provide a vacuum encapsulation as well as electrical conductions. A RF model of the encapsulation cap is established to evaluate the parasitic effect of the packaging, which provides an effective design solution of 3D RF MEMS encapsulation. With the proposed packaging structure, the signal-to-background ratio (SBR) of 24 dB is achieved, as well as the quality factor (Q-factor) of the resonator increases from 8000 to 10400 after packaging. The packaged resonator has a linear frequency–temperature (f–T) characteristic in a temperature range between 0 °C and 100 °C. And the package shows favorable long-term stability of the Q-factor over 200 days, which indicates that the package has excellent hermeticity. Furthermore, the average shear strength is measured to be 43.58 MPa among 10 samples.

Keywords: 3D packaging, coupling noise, Q-factor, RF MEMS resonator

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1. Introduction

Radio frequency micro-electromechanical system (RF MEMS) resonator with high quality factor (Q-factor) is considered as a potential substitute for quartz crystal and ceramic resonators in wireless communication systems due to its small size, low cost, high performance, and complementary-metal-oxide-semiconductor (CMOS) compatible fabrication process.[1] With the development of RF MEMS resonators in integration, high frequency and low power, the packaging technology becomes more and more important.

Recently, three-dimensional (3D) wafer-level packaging of RF MEMS devices has been widely studied, since it has advantages of smaller footprint, lower power consumption, and better ability to integrate 3D microsystemthan planar interconnects packaging.[2] Conventionally, through-silicon-via (TSV) technique was often used in 3D MEMS encapsulation to achieve vertical electrical interconnection,[3–5] which utilizes electroplated Cu as the medium of electrical signal transmission and the thermal oxide layer as the insulation between metal Cu and silicon substrate. However, this technique also has disadvantages, such as complexity of process, mismatched thermal expansion coefficient, and high cost. The glass-in-silicon (GIS) reflow process has been reported as a promising technique to fabricate TSVs, which utilizes low-resistivity silicon instead of electroplated metal to transmit signals, and a thick reflowed glass layer as the insulation.[6–8] This technique has many merits, such as a superior insulation property, matched thermal expansion coefficient, low dielectric loss, simple fabrication process, etc. However, it was often used for low-frequency MEMS packages. When RF signals travel through the silicon vias, high loss of silicon and via-to-via coupling noise will debase the RF signal transmission quality. In order to reduce energy loss and mitigate noise, the design optimization of encapsulation cap is necessary for high-end RF MEMS devices.

The stable pressure environment of the packaged cavity is essential for reliable and repeatable performance over a long period of time, so that RF MEMS resonators will be protected from being potentially contaminated such as dust particles, moisture, and gas molecules. Stability characterizations of MEMS encapsulation have become more important as devices develop toward commercialization. For the MEMS resonator, resonant frequency and Q-factor stability towards temperature or long-term measurement are significant metrics to demon-

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strate its packaging reliability.[9,10]

This paper presents a 3D encapsulation with low-loss silicon vias for RF MEMS resonators. Silicon vias for transmitting RF signals are fabricated by the GIS process. The cap is designed with low resistive silicon vias, thick glass insulation, grounded substrate, and coaxial-shielding structure to ensure RF signals are transmitting without loss. Au–Sn solder bonding is adopted to provide a vacuum encapsulation as well as electrical conductions.[11–13] After packaging, RF MEMS resonators achieve excellent frequency responses. Furthermore, in this work, we systematically study the reliability performance of the packaged MEMS resonator, including frequency–temperature (f–T) characteristic, long-term hermeticity, and shear strength test.

2. Packaging design

The RF MEMS disk resonator with a resonant frequency of 150 MHz is fabricated by the three-layers poly-silicon process.[14] The resonator operates at radial-contour mode, and uses capacitive transduction to achieve electrostatic actuation and sensing. The encapsulation cap is fabricated with a low resistivity silicon wafer (0.005 Ω·cm) to achieve low-loss silicon vias as well as low grounding resistance, and utilizes reflowed glass as the insulation between silicon vias and substrate. Au–Sn solder bonding is employed to provide a vacuum encapsulation as well as electrical conductions. The schematic view of the proposed RF MEMS packaging structure is shown in Fig. 1.

In 3D packages of RF MEMS, the crosstalk between the input and output (I/O) ports will induce significant attenuation in the signal-to-background ratio (SBR). This coupling is mainly induced by the substrate coupling between I/O ports, which can be effectively suppressed through grounding the substrate and inserting a grounded shielding layer, making radiant signals flow into the ground and have no influence on the transmission. In this work, two encapsulation cap structures are designed to evaluate the influence of crosstalk on RF signal transmission as follows: a) there is reflowed glass between I/O ports, and silicon vias are not shielded (Fig. 2(a)); b) the silicon vias are coaxially shielded by the grounded silicon substrate (Fig. 2(b)).

High frequency structure simulator (HFSS) software is adopted to establish 3D cap structures, and then to simulate feed-through curves between I/O ports. Based on the electrical models of the cap structures, the coupling capacitance C_c of Fig. 2 can be extracted by fitting the HFSS simulated feed-through curves with advanced design system (ADS) simulation. As shown in Fig. 3, the extracted C_c of the cap without shielding is 3.252 fF, which will induce serious crosstalk. Fortunately, the C_c is greatly reduced to 0.058 fF for the coaxially shielded cap that is not susceptible to crosstalk, and is nearly unchanged for the larger via pitch. Considering the requirement of the miniaturization of MEMS devices, the via pitch of the shielding cap is designed to be 200 μm.

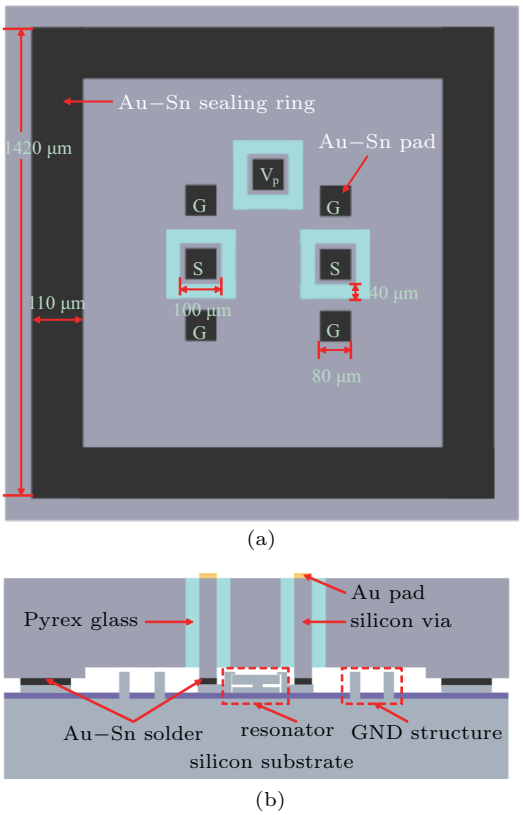


Fig. 1. (color online) (a) Top view of the proposed encapsulation cap. (b) Cross section of the packaged RF MEMS resonator.

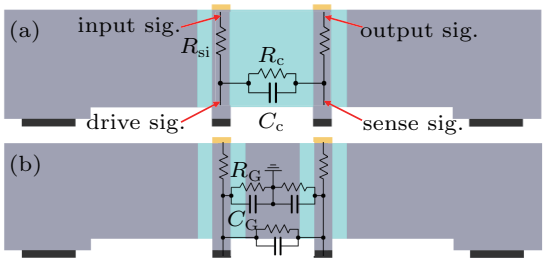


Fig. 2. (color online) Schematic view and via-to-via coupling models of proposed cap structures: (a) without shielding and (b) with coaxial shielding.

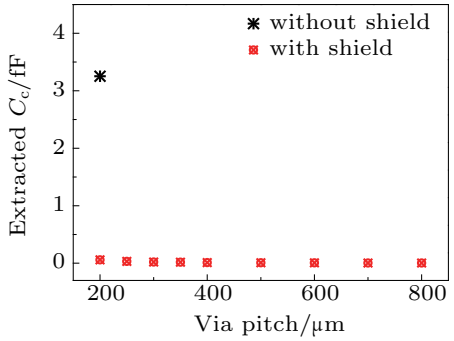


Fig. 3. (color online) Extracted C_c for different cap structures by fitting the HFSS simulated feed-through curves with ADS simulation.

3. Fabrication process

The encapsulation cap is micro-fabricated with a low resistive silicon wafer of 520 μm in thickness by GIS reflow process. The fabrication process flow of the 4-inch (1 inch = 2.54 cm) cap wafer is shown in Fig. 3. A layer of 350 μm is first etched away from the silicon substrate by using a deep reactive ion etch (DRIE) process to form reflow molds with silicon pillars (Fig. 4(a)). The substrate is anodically bonded to a Pyrex 7740 glass wafer in a vacuum, and then Pyrex glass is thermally reflowed into the molds under the assistance of high temperature and pressure load. Next, double-side chemical and mechanical polishing (CMP) processes are performed to form vertical silicon vias, and the thickness of the wafer is 300 μm after this process (Fig. 4(b)). Then, a shallow cavity is etched to 10 μm using a reactive ion etch (RIE) process to house the disk resonator (Fig. 4(c)). Finally, Ti (50 nm)/Au (150 nm)/Sn (2.1 μm)/Au (50 nm) stacked solder and Ti (50 nm)/Au (300 nm) contact pads are then produced by the lift-off process (Fig. 4(d)).

The bonding is carried out with SUSS SB6e vacuum bonder. Before bonding, the aligned device and cap wafers are held at 150 °C in vacuum pressure around 3×10^{-4} mbar (1 bar = 10^5 Pa) for 30 min to accomplish outgassing from their surfaces. Afterwards, a pressure of 7 MPa is applied, and bonding starts at 310 °C, lasting for 60 min. After the wafer-level dicing process, the packaged resonators each with a size of 1.5 mm×1.5 mm×0.8 mm are prepared for testing (Fig. 5(a)). Figure 5(b) presents the SEM cross-section of a packaged die, showing the details of the reflowed Pyrex glass, shielding layer, and the packaged cavity.

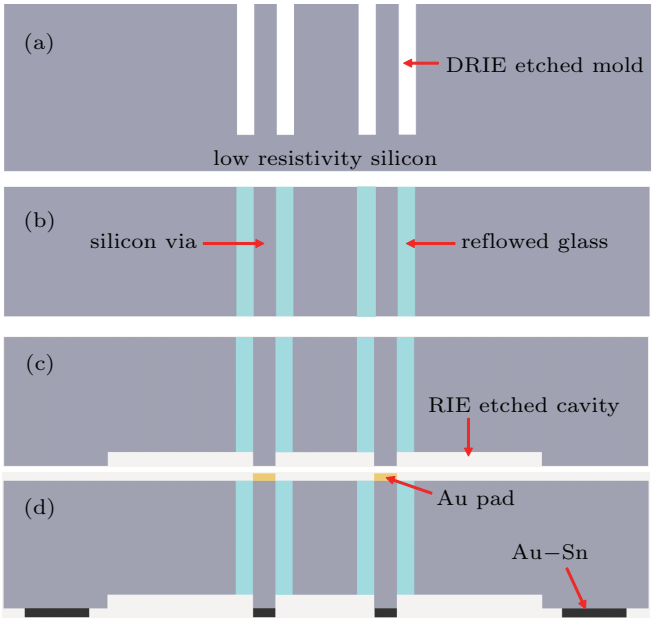


Fig. 4. (color online) Fabrication process flow of the encapsulation cap.

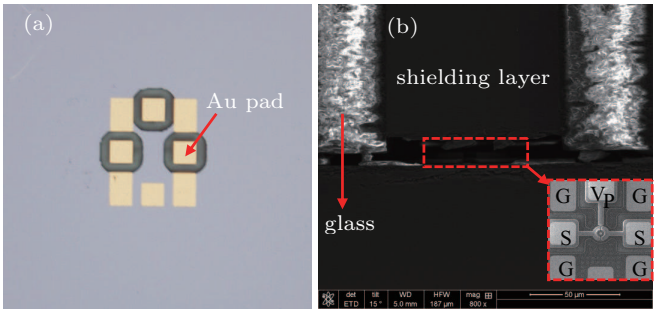


Fig. 5. (color online) (a) Photograph of the packaged resonator using a coaxially shielded encapsulation cap. (b) SEM cross-section photograph of the packaged resonator. In the lower right corner shown is the SEM photograph of the disk resonator.

4. Measurement and discussion

The frequency response of the resonator is characterized by a two-port measurement scheme. The frequency spectrum of the packaged resonator is measured by applying a DC-bias voltage of 8 V, and the results are compared with the measured value of the resonator before packaging.

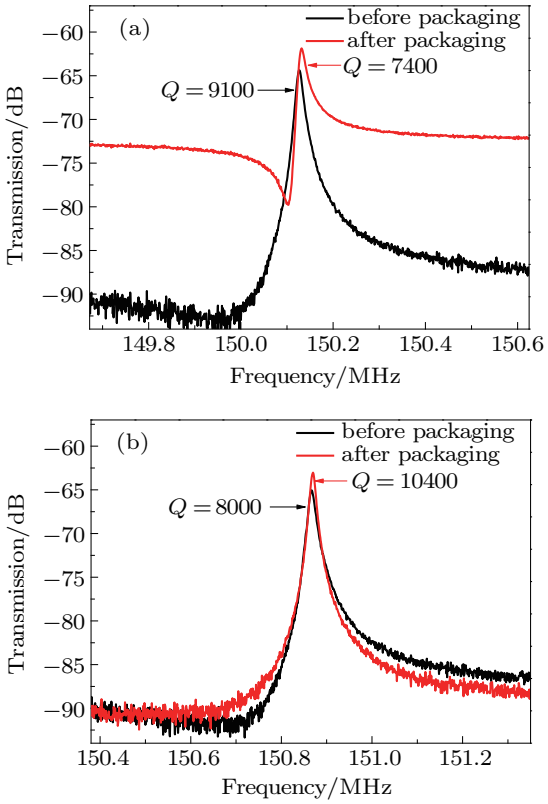


Fig. 6. (color online) Measured frequency spectra of packaged resonators: (a) without noise shielding and (b) with coaxial shielding.

Using the cap without noise shielding, the sense signal is seriously submerged by the coupling noise, the SBR is reduced from 22 dB to 9 dB as shown in Fig. 6(a), and its Q-factor also decreases from 9100 to 7400 due to spectrum distortion. However, using the cap with coaxial shielding, the frequency spectrum is not affected by the parasitic effect (Fig. 6(b)). The tested Q-factor for the optimized package increases from

8000 to 10400. This is due to a reduced pressure in the packaged cavity which minimizes the effect of air-damping loss. From the above results, the developed 3D encapsulation cap can provide low-noise vacuum packaging for the RF MEMS resonator.

The f–T characteristic of the resonator, packaged with the noise shielding encapsulation cap, is also investigated, which is one of the most important metrics for the frequency stability to evaluate residual stress caused by encapsulation. The resonant frequency is measured every 5 °C while temperature ramps up and down between 0 °C and 100 °C in the thermal chamber. The temperature coefficient of frequency (TC_F) of the resonator is −24.9 ppm/°C and also has a linear f–T characteristic (Fig. 7(a)), which is of benefit to the future temperature compensation. Further, the resonant frequencies can be calculated by the measured values of TC_F at different temperatures, and the deviations between the calculated and measured resonant frequencies are shown in Fig. 7(b). There is no variation trend with temperature, and the slight deviation stays within the measurement error due to the temperature accuracy of the thermal chamber. The measured results indicate that there is no significant residual stress caused by encapsulation.

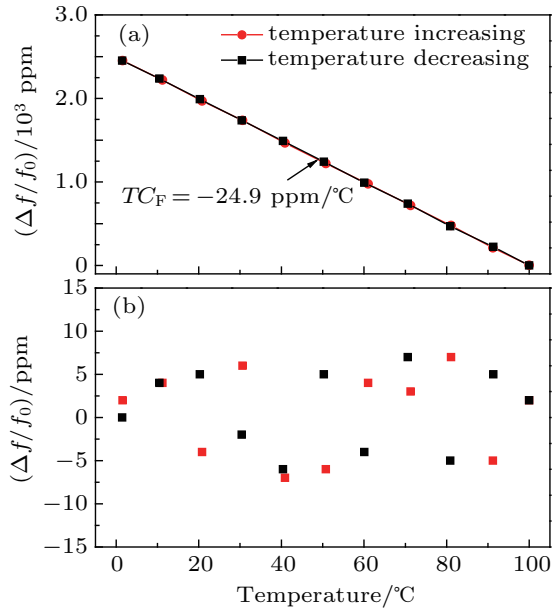


Fig. 7. (color online) (a) Temperature dependence of frequency for the packaged resonator between 0 °C and 100 °C. (b) Deviations of resonant frequencies from their interpolated values in a temperature range between 0 °C and 100 °C.

The hermeticity test is implemented using the Q-factor testing method, which is commonly used in the MEMS industry. In the hermeticity test, the packaged resonator serves as a pressure sensor to monitor the pressure in the packaged cavity. The packaged resonator is tested at a constant temperature (25 °C) for 200 days. The Q-factor of the resonator is monitored every 10 days using an Agilent E5071C network analyzer. The Q-factor drift with the operation time of 200 days is demonstrated in Fig. 8. As shown in this figure, the slight drop of the Q-factor is caused by outgassing in the first 20 days, and the Q-factor remains stable in the following 180 days. The favorable long-term stability of the Q-factor indicates that the packaged resonator has good hermeticity.

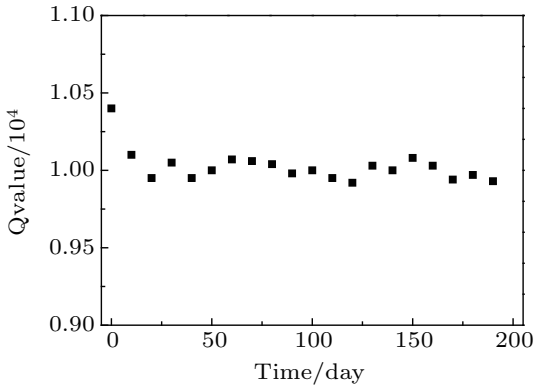


Fig. 8. Drift of Q-factor with an operation time of 200 days for the encapsulated resonator.

The shear strengths of the packaged samples are measured using a Royce 650 bond tester, and the results are shown in Fig. 9. The maximum shear strength, minimum shear strength and the average are 48.7, 38.5, and 43.58 MPa, respectively, which shows that the shear strengths of the packaged resonators are all much higher than the shear strength criterion benchmarked by MIL-STD-883F (the minimum shear strength which a die can withstand is 6.1 MPa).

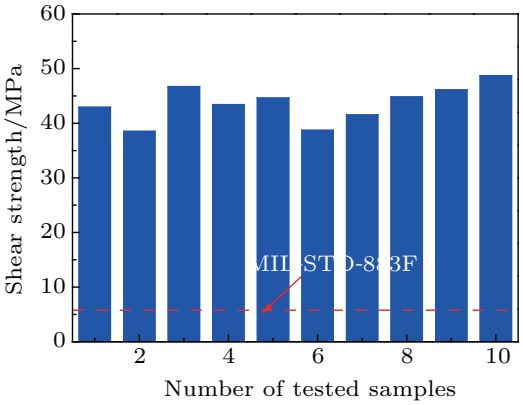


Fig. 9. (color online) Measured results of shear strength for 10 packaged samples.

5. Conclusions

A 3D vacuum packaging technique with silicon vias is developed for RF MEMS resonators. The analytical model for the GIS cap is established to evaluate the parasitic effect from the packaging, which provides an important guideline for RF MEMS encapsulation. The proposed packaging structure with coaxial shielding is effective for achieving excellent frequency responses of the packaged resonators. Au–Sn solder bonding provides a good vacuum condition, which results

in a higher Q-factor. Moreover, the f–T characteristic, long-term Q-factor, and shear strength are characterized, and the measured results show that the packages have favorable performances. It is therefore concluded that the proposed wafer-level 3D vacuum encapsulation technique is suitable for RF MEMS device applications.

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