Superjunction nanoscale partially narrow mesa IGBT towards superior performance*

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We present a detailed study of a superjunction (SJ) nanoscale partially narrow mesa (PNM) insulated gate bipolar transistor (IGBT) structure. This structure is created by combining the nanoscale PNM structure and the SJ structure together. It demonstrates an ultra-low saturation voltage ($V_{ce(sat)}$) and low turn-off loss (E_{off}) while maintaining other device parameters. Compared with the conventional 1.2 kV trench IGBT, our simulation result shows that the $V_{ce(sat)}$ of this structure decreases to 0.94 V, which is close to the theoretical limit of 1.2 kV IGBT. Meanwhile, the fall time decreases from 109.7 ns to 12 ns and the E_{off} is down to only 37% of that of the conventional structure. The superior tradeoff characteristic between $V_{ce(sat)}$ and E_{off} is presented owing to the nanometer level mesa width and SJ structure. Moreover, the short circuit degeneration phenomenon in the very narrow mesa structure due to the collector-induced barriers lowering (CIBL) effect is not observed in this structure. Thus, enough short circuit ability can be achieved by using wide, floating P-well technique. Based on these structure advantages, the SJ-PNM-IGBT with nanoscale mesa width indicates a potentially superior overall performance towards the IGBT parameter limit.

Keywords: insulated gate bipolar transistor (IGBT), partially narrow mesa (PNM), superjunction (SJ), turn-off loss

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1. Introduction

The insulated gate bipolar transistor (IGBT) is an important power semiconductor device, which is widely used in various power electronic systems. To achieve the best device performance, many technical solutions have been pursued to obtain low saturation voltage ($V_{ce(sat)}$) and small turn-off loss (E_{off}) without compromising other device parameters and reliability. From the physical mechanism point of view, the theoretical limit of $V_{ce(sat)}$ is that the holes only contribute to the conductivity modulation effect in the on-state.[1] Thus, the narrowed mesa width in trench IGBT can be an effective way to achieve this theoretical limit. Based on this concept, many structure variations have been presented, such as the advanced CSTBT structure,[2] the micro pattern trench IGBT,[3] the very shallow trench IGBT by the scaling rule theory,[4] the trench IGBT with P-ring structure and point injection effect,[5,6] the fin p-body IGBT,[7] the superjunction (SJ) trench IGBT with buried oxide,[8] and the partially narrow mesa IGBT (PNM-IGBT).[9,10] Among these structures, the $V_{ce(sat)}$ of PNM-IGBT can be very close to the theoretical limit by using a nanoscale mesa width as the hole barrier layer. Moreover, the fabrication process of PNM-IGBT is completely compatible with the trench IGBT structure, which has been experimentally demonstrated in the prior work.[9] However, when the mesa width decreases to the nanometer level, extensive holes are stored in the drift region in the on-state. The huge amount of minority carriers cannot sweep out quickly during the turn-off process and the turn-off loss becomes much higher inevitably. To improve the degenerated dynamic performance, Sumitomo *et al.* proposed a dynamic gate control technique to optimize the E_{off}.[10] But this improvement needs to adopt the double gate structure in chip layout and an additional gate control time during turn-off. Another proven way to optimize the dynamic performance of IGBT is by using the SJ structure.[11–15] Liu *et al.* reported that the PNM-IGBT with SJ structure (SJ-PNM-IGBT) can achieve good blocking ability and dynamic performance.[15] But they only studied the SJ-PNM-IGBT structure with 2 μm mesa width. The characteristics of SJ-PNM-IGBT with nanoscale mesa width were not studied in the previous work, especially the dynamic performance and reliability.

In this work, two-dimensional (2D) numerical simulation is performed to analyze the characteristic of the SJ-PNM-IGBT with nanoscale mesa width and the device parameters are compared with those of the conventional IGBT, the PNM-IGBT, and the SJ-IGBT. The influence of the structure variation on the device's static and dynamic performance is also studied in detail. In addition, the reverse bias SOA (RBSOA) ability and short circuit behavior for different structures are compared to verify the reliability of the structure.

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2. Device structure

Figure 1 shows the cross-sectional view of the conventional trench IGBT structure, the PNM-IGBT with 30 nm mesa width, the SJ-IGBT, and the SJ-PNM-IGBT with 30 nm mesa width. In order to achieve an accurate comparison, identical doping profiles and dimensional parameters are assumed in all devices, except for the SJ structure and trench nanoscale mesa region. The PNM structure (see Figs. 1(b) and 1(d)) is widened at 3 μm trench depth by expanding laterally to achieve the 30 nm mesa width. The IGBT structure with this mesa width is very close to the 1.2 kV theoretical limit, which has been demonstrated with simulation and experiment by Sumitomo *et al.*[9] Then, the N/P pillar is filled in the drift region to create the SJ structure, as shown in Fig. 1(d). Considering the charge balance requirement, 2 μm N/P pillar width is selected to keep the fully depleted condition at high pillar doping concentration.[11] The major structural parameters are shown in Table 1.

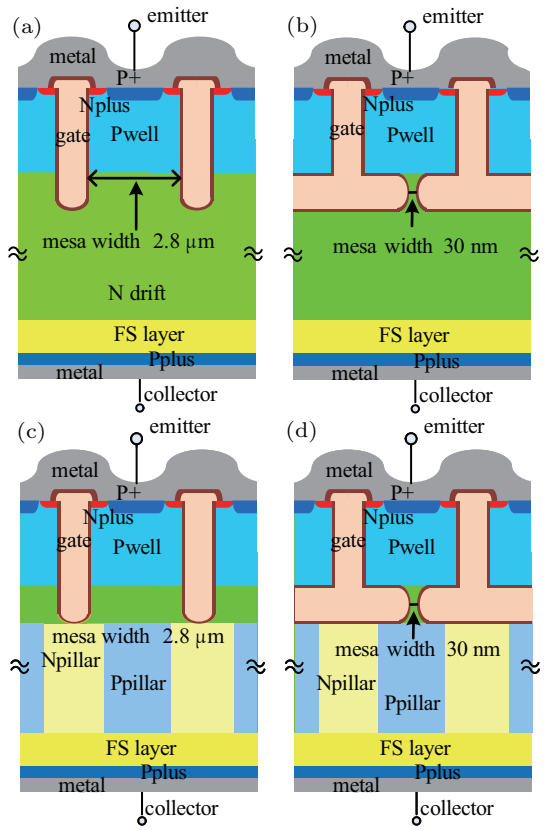


Fig. 1. (color online) Cross-sectional view of (a) the conventional IGBT, (b) the PNM-IGBT, (c) the SJ-IGBT, and (d) the SJ-PNM-IGBT. The mesa widths of the conventional trench structure and the PNM trench structure are 2.8 μm and 30 nm, respectively.

Table 1. Major structural parameters.

Structural parameters	30 nm SJ PNM IGBT	SJ IGBT	30 nm PNM IGBT	FS IGBT
Cell pitch/μm	4	4	4	4
N-drift thickness/μm	120	120	120	120
Gate oxide thickness/nm	100	100	100	100
Trench depth/μm	5	5	5	5
Trench width/μm	1.2	1.2	1.2	1.2
Main mesa width/μm	2.8	2.8	2.8	2.8
Mesa width at partially narrow area/nm	30	–	30	–
Pillar width/μm	2	2	–	–
Pillar doping/10^{16} cm^{-3}	1	1	–	–
N-drift doping/10^{13} cm^{-3}	6.8	6.8	6.8	6.8
FS doping/10^{16} cm^{-3}	9.0	9.0	9.0	9.0
P-well doping/10^{17} cm^{-3}	2.5	2.5	2.5	2.5
N$^+$ doping /10^{19} cm^{-3}	9.0	9.0	9.0	9.0
P$^+$ collector doping/10^{17} cm^{-3}	9	9	9	9
Lifetime τ_n/μs	10	10	10	10
Lifetime τ_p/μs	3	3	3	3

3. Device characteristics and structure variation comparison

3.1. Analysis of static and dynamic performance

Figure 2 shows the simulated breakdown voltage characteristic. The breakdown voltages of the conventional IGBT, 30 nm PNM-IGBT, SJ-IGBT, and 30 nm SJ-PNM-IGBT at 100 μA/cm^2 are 1.51 kV, 1.54 kV, 1.76 kV, and 1.76 kV, respectively. Obviously, the breakdown voltages of the IGBTs with SJ structure are higher than those of the other structures owing to the SJ advantage.

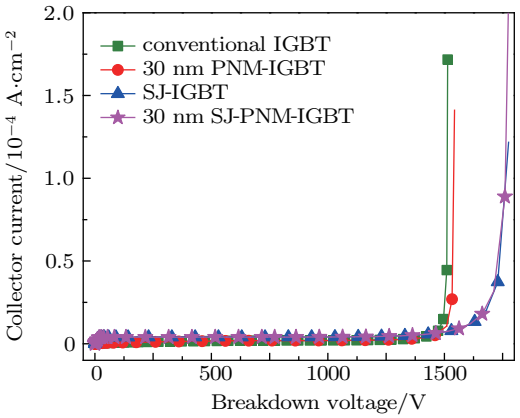


Fig. 2. (color online) Simulated breakdown characteristics of different structures at gate voltage of 0 V.

Figure 3 shows the forward *I*–*V* characteristics of all structures. At a current density of 100 A/cm^2 and gate bias $V_{ge} = 15$ V, the $V_{ce(sat)}$ of the conventional IGBT, 30 nm PNM-IGBT, SJ-IGBT, and 30 nm SJ-PNM-IGBT are 1.74 V, 0.92 V, 1.53 V, and 0.94 V, respectively. As we mentioned before, the nanoscale mesa can block the hole flowing effectively, which helps to approach the theoretical limit. The detailed theoretical computation equation was given in Ref. [1]. According to the theoretical result of ideal 1200 V IGBT,[1,2] the limit of $V_{ce(sat)}$ is about 0.9 V at current density 100 A/cm^2. Therefore, the $V_{ce(sat)}$ of IGBTs with 30 nm mesa width are very close the theoretical limit due to the superior conductivity modulation effect. It is worth noting that 30 nm SJ-PNM-IGBT has

slightly higher $V_{ce(sat)}$ than 30 nm PNM-IGBT. The reason is that part of the holes are used to compensate the high doping concentration of the SJ N pillar in the on-state not for the conductivity modulation effect. This phenomenon is more obvious in the high pillar doping concentration situation, as shown in Fig. 6. In addition, it can be seen that the saturation current densities of all structures are extremely higher due to the high MOS channel density. It will cause the poor short circuit performance and the optimized structure will be discussed in the later section.

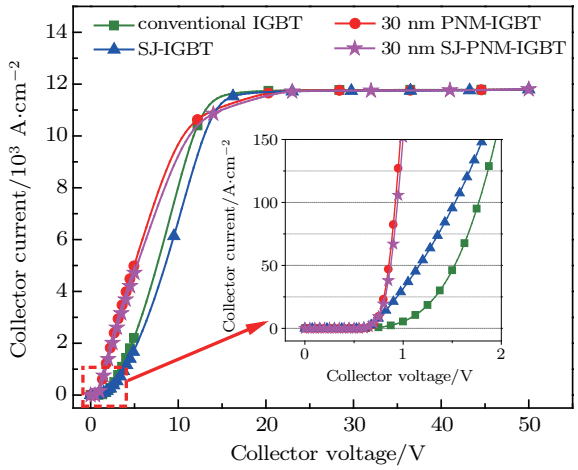


Fig. 3. (color online) Simulated forward *I*–*V* characteristics for different structures.

Figure 4 shows the inductive load turn-off waveforms. All structures are simulated with 600 V DC bus voltage, 5 Ω gate resistor, and 150 nH stray inductance. The load current density is set at 100 A/cm^2. The turn-off fall times for the conventional IGBT, 30 nm PNM-IGBT, SJ-IGBT, and 30 nm SJ-PNM-IGBT are 109.7 ns, 271.9 ns, 10.8 ns, and 12 ns, respectively. The turn-off losses of the conventional IGBT, 30 nm PNM-IGBT, SJ-IGBT, and 30 nm SJ-PNM-IGBT are 5.32 mJ, 18.32 mJ, 1.83 mJ, and 1.97 mJ, respectively. The E_{off} of 30 nm SJ-PNM-IGBT is down to only 37% of that of the conventional IGBT. As we mentioned before, the E_{off} of 30 nm PNM-IGBT is significantly higher than that of the other structures due to the influence of the excessive carriers storage effect.[9,10] However, the IGBTs with SJ structure present a superior dynamic characteristics owing to the fast carriers extraction.[11–14]

During the turn-off process, an oscillating peak voltage may appear due to the coupling effect of the di/dt, the gate collector capacitance, and the stray inductance.[16–18] It depends on the change rate of di/dt. For the conventional IGBT (green line), we can see that the change rate of di/dt is relatively moderate due to the slow minority carrier recombination process. Therefore, the collector peak voltage of the conventional IGBT is not very high and the dv/dt variation is also relatively smooth. This situation is more distinct for the 30 nm PNM-IGBT (red line) due to the slowest turn-off process in all structures. Conversely, the IGBT devices with SJ structure present a different situation owing to the faster turn-off speed. The fast di/dt with parasitic stray inductance, gate collector capacitance, and gate resistor can lead to a resonance condition.[16–18] When the oscillation occurs in the turn-off transient process, a high collector oscillating peak voltage and a negative drain current can be seen in the turn-off waveform, as shown in Fig. 4. Several methods can be used to suppress oscillation noise in the fast turn-off process, such as appropriate back concentration engineering, low parasitic inductance, and reduced gate collector capacitance.[13,16–18]

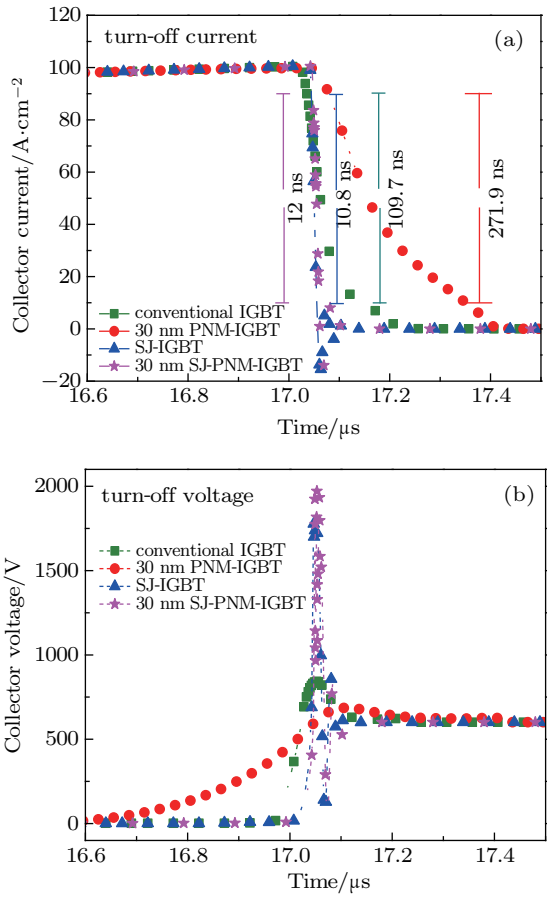


Fig. 4. (color online) Simulated turn-off (a) current and (b) voltage waveforms of the conventional IGBT, 30 nm PNM-IGBT, SJ-IGBT, and 30 nm SJ-PNM-IGBT. The pillar doping concentration of SJ-IGBT and SJ-PNM-IGBT is 1×10^{16} cm^{-3}.

3.2. Analysis of device characteristics with the structure variation

Figure 5 shows the tradeoff characteristic between $V_{ce(sat)}$ and E_{off} by varying the backside P^+ doping concentration. It can be seen that the tradeoff curve of 30 nm PNM-IGBT is near the left side of the coordinate axis and the SJ-IGBT is near the bottom of the coordinate axis. This means that the PNM-IGBT can effectively reduce $V_{ce(sat)}$ and the SJ-IGBT can contribute to reduce E_{off}. Note that the SJ-PNM-IGBT with nanoscale mesa width is even closer to the coordinate axis

with the mesa width reducing. Thus, the SJ-PNM-IGBT with nanoscale mesa width exhibits superior $V_{ce(sat)}$–E_{off} tradeoff performance due to inheriting the advantages of the PNM structure and the SJ structure simultaneously.

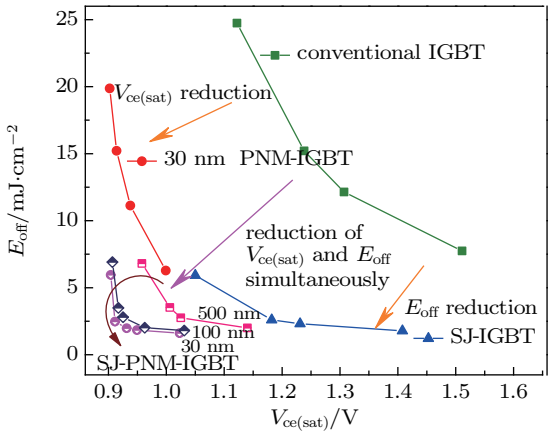


Fig. 5. (color online) Simulated tradeoff characteristics of E_{off} and $V_{ce(sat)}$ for different structures.

In the on-state, the huge carriers need to be stored at the drift region as much as possible. Therefore, the extremely narrow trench mesa width can impede the hole flowing effectively. In the off-state, the huge carriers need to be extracted as fast as possible. But the turn-off tail currents of the conventional and the PNM structures are inevitable due to the high plasma density in the undepleted drift region. It causes long turn-off fall time and high E_{off}. Fortunately, the switching speed of the SJ structure is faster than that of the other structures because the movement of the depletion layer in the SJ pillar is along vertical and lateral directions simultaneously. The excessive carriers in the plasma region are pushed to the device anode due to fast extension of the depletion layer. Therefore, the SJ-PNM-IGBT with nanoscale mesa width can achieve ultra-low $V_{ce(sat)}$ and low E_{off} simultaneously.

Figure 6 depicts the characteristics of the $V_{ce(sat)}$ and breakdown voltage with the variation of the pillar doping concentration from 1×10^{15} cm^{-3} to 3×10^{16} cm^{-3} and the mesa width from 20 nm to 1 μm. It can be seen that the breakdown voltage keeps almost constant when the pillar doping concentration is less than 1×10^{16} cm^{-3}. If the doping concentration is higher than 1×10^{16} cm^{-3}, the breakdown voltage begins to drop due to the incomplete depletion of the N/P pillar charge. The breakdown voltage degeneration situation due to the charge imbalance effect has been discussed in the prior work.[11] Thus, an optimized structure can be achieved by selecting the pillar doping concentration carefully. Moreover, it can be seen that the breakdown voltages with different mesa widths are almost the same and the curves nearly overlap (dashed line), as shown in Fig. 6. On one hand, we select the mesa width only in nanoscale scope for comparison. In these structures, the trench bottom shapes are similar and the influence of the mesa width on the blocking ability is small (only about 10 V). On the other hand, the breakdown voltage of this structure is mainly related to the pillar doping concentration of the SJ structure. Therefore, the difference of breakdown voltage with mesa width variation is not distinct in Fig. 6.

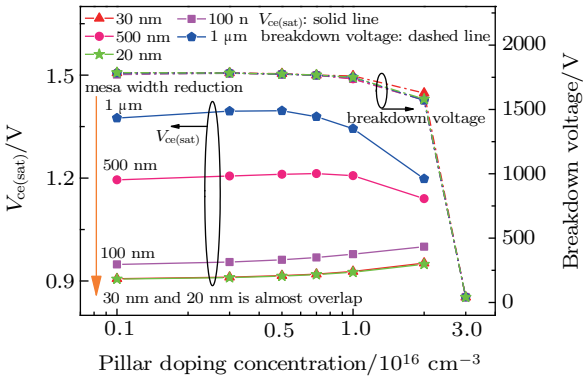


Fig. 6. (color online) Simulated $V_{ce(sat)}$ and breakdown voltage of the SJ-PNM-IGBT with different pillar doping concentrations and mesa widths.

In addition, a unique $V_{ce(sat)}$ characteristic is shown for the very narrow mesa width structure. It can be seen that the $V_{ce(sat)}$ of the 500 nm and 1 μm mesa widths keep relatively constant when the pillar doping concentration is below 7×10^{15} cm^{-3}. Then, the $V_{ce(sat)}$ becomes lower as the pillar doping concentration increases. The reason is that the conductivity modulation effect of relatively wide mesa width structures (1 μm and 500 nm) is not enough and the $V_{ce(sat)}$ can be further reduced at high pillar doping concentrations due to the unipolar effect.[11] But for the very narrow mesa width (below 100 nm), the conductivity modulation effect almost reaches the limit and the minority carrier concentration is high enough for bipolar conduction mode. In this situation, when the pillar doping concentration becomes higher, some holes are used to compensate the N pillar high doping concentration and the conductivity modulation effect is slightly weakened, as we mentioned before. This phenomenon is unique for the SJ IGBT with nanoscale mesa width.

Obviously, the $V_{ce(sat)}$ becomes smaller when the mesa width reduces from 1 μm to 30 nm and this is in good agreement with the theory analysis.[1] However, it can be seen that the $V_{ce(sat)}$ curve of 20 nm mesa width is almost overlapped with that of 30 nm mesa width. This means that the $V_{ce(sat)}$ hardly becomes lower if the trench mesa width shrinks less than 30 nm. Therefore, the 30 nm mesa width nearly reaches the bound width. The main reason is that the mobility decreases as the carrier density in the very narrow mesa width increases.[1]

4. Turn-off RBSOA performance

To analyze the turn-off RBSOA reliability, TCAD 2D mixed electro-thermal simulation with thermodynamics model is used. All devices are turned on to reach 5 times rated current (500 A/cm^2) with gate signal control and turned off at 1000 V DC bus voltage to compare the RBSOA ability. Considering the self-heating phenomenon is inevitable in high voltage and high current turn-off process, the thermal electrode is added at the bottom structure of each device in the simulation. Although the thermal boundary condition may not be in good agreement with the realistic turn-off situation due to the influence of parasitic component and practical environment factors, the internal physical behavior and turn-off reliability can still be given from the simulation results.

Figure 7 shows the turn-off characteristics of four structures. It can be seen that the 30 nm SJ-PNM-IGBT can turn off normally at 5 times rated current condition without latch-up phenomenon. This means that the 30 nm SJ-PNM-IGBT demonstrates a sufficient turn-off RBSOA ruggedness compared with the conventional IGBT.

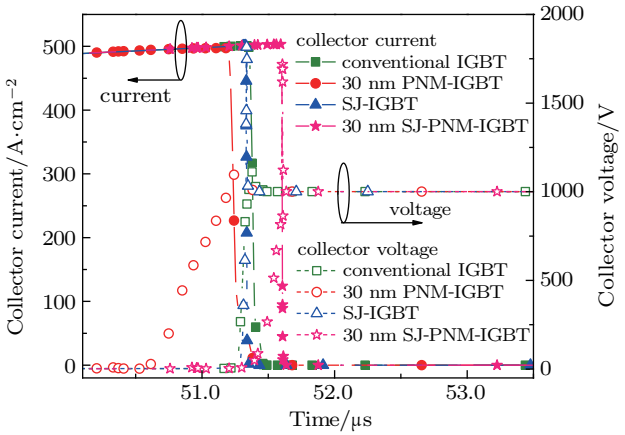


Fig. 7. (color online) Simulated turn-off waveforms for 4 structures at 5 times rated current condition (500 A/cm^2). The gate resistor is 5 Ω and the stray inductance is 20 nH. The thermal resistance is 0.5 k/kW·cm^2.

5. Design consideration of short circuit ability

For the very narrow mesa structure, a severe degeneration in the short circuit behavior is shown due to the collector bias induced barrier lowering effect (CIBL effect).[7,19] This phenomenon can cause the continual increase of the saturation current with the rising of the collector voltage. In other words, the collector current shows a non-saturated output characteristic in the on-state.[19] It is a negative factor in the IGBT design by using very narrow mesa structure. Fortunately, unlike other very narrow mesa structure, the SJ-PNM-IGBT with nanoscale mesa width is designed by combining the normal mesa width and the very narrow mesa width in one trench structure. The very narrow mesa structure is only at the trench bottom region and away from the top N$^+$/P-well junction. Thus, the CIBL effect is effectively avoided owing to the structure advantage. In Fig. 3, it can be seen that the saturation current curve of 30 nm SJ-PNM-IGBT keeps constant after 20 V collector voltage like other structures.

Another common situation in IGBT structure is the high current density due to the high MOS channel density. When the IGBT structure is designed with a high channel density, huge electrons are injected in the device in the on-state. Therefore, the saturation current density will become higher inevitably and it can cause a poor short circuit behavior. Note that the high saturation current density is shown in Fig. 3 and it needs to be optimized further. One proven effective method to reduce the saturation current while maintaining the same $V_{ce(sat)}$ is by using the wide floating P-well structure.[20] Based on this design concept, the PiN diode part is integrated in the device for conductivity modulation effect and the MOS transistor is reduced to suppress the saturation current density.

Figure 8 shows 2D cross-sectional view of the conventional IGBT and 30 nm SJ-PNM-IGBT with wide floating P-well structure. In this wide pitch structure, the cell pitch width consists of 1 active cell and 10 dummy cells of the floating P-well structure. The cell pitch of the wide structure is 11 times that of the original structure (44 μm), as shown in Fig. 8. For an accurate comparison between devices, all structures are designed with this cell structure and pitch dimension. Then, the short circuit ability is investigated by using the TCAD mixed electro-thermal simulation. The 300 K atmosphere temperature and thermal resistance 0.5 k/kW·cm^2 are used in simulation.

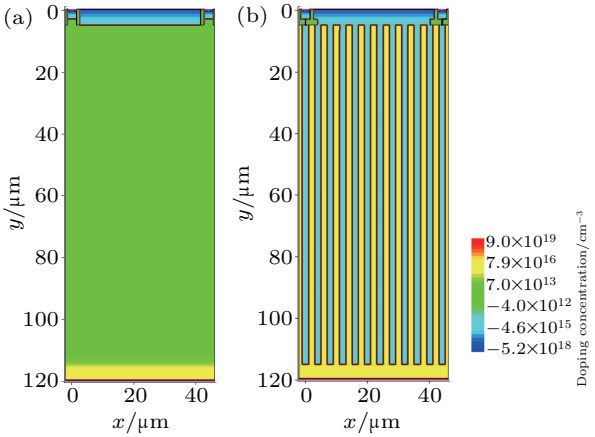


Fig. 8. (color online) Cross-sectional view of conventional IGBT and 30 nm SJ-PNM-IGBT with one active cell and 10 dummy cells.

Figure 9 shows the short circuit waveforms of all structures. It can be seen that the saturation current densities of all structures are roughly about 1500 A/cm^2 and the devices can turn off normally after 10 μs short current pulse. This saturation current is much smaller than the saturation current of the original high channel density structure. Therefore, the 30 nm SJ-PNM-IGBT demonstrates enough short circuit ability with the floating P-well technique. Considering the influence of the cell pitch width variation on the device's parameter, the major

static and dynamic performances of all structures with wide pitch structure are given in Table 2 for comparison. It can be seen that the performance of the 30 nm SJ-PNM-IGBT with floating P-well structure still presents great overall characteristics.

Table 2. Major parameter comparison for wide pitch structure. All structures are designed with the 44 μm cell pitch width and the floating P-well structure.

Structural parameters	30 nm SJ PNM IGBT	SJ IGBT	30 nm PNM IGBT	FS IGBT
Breakdown voltage/V	1536	1443	1439	1370
$V_{ce(sat)}$/V	1.17	1.42	1.14	1.42
T_f/ns	14	15.8	278.5	139.9
E_{off}/mJ	2.3	2.2	18.2	7.7

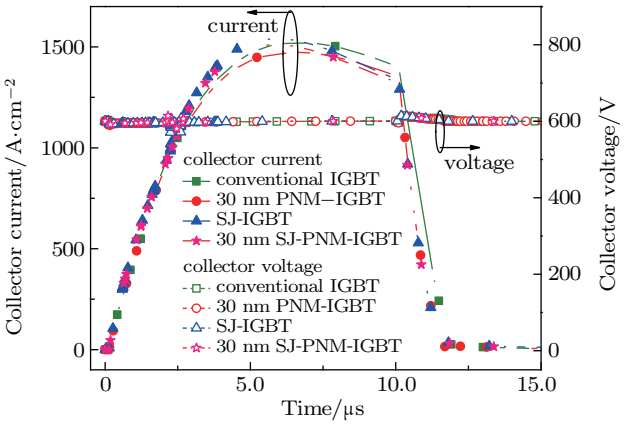


Fig. 9. (color online) Simulated short circuit waveforms of the conventional IGBT, 30 nm PNM-IGBT, SJ-PNM-IGBT, and 30 nm SJ-PNM-IGBT with wide floating P-well. The gate voltage and DC bus voltage are set to be 15 V and 600 V, respectively. The gate resistor of 5 Ω and stray inductance 20 nH are used. The thermal resistance is 0.5 k/kWcm^2.

6. Conclusion

An IGBT structure that inherits the advantages of the nanoscale PNM structure and the SJ structure is analyzed in detail by numerical simulation. The conductivity modulation of this proposed structure is effectively enhanced by using nanometer level mesa width. The high E_{off} in narrow mesa structure is optimized with SJ structure. The fall time of this structure decreases to 12 ns and the E_{off} is optimized to only 37% of that of the conventional structure. Great trade-off performance between $V_{ce(sat)}$ and E_{off} is also shown in this structure. In addition, enough turn-off RBSOA ruggedness is given by simulation comparison. For the device's short circuit ability, the CIBL effect is not observed in this nanoscale mesa structure. Thus, enough short circuit ability of this structure can be given by using appropriate floating P-well design, which is comparable with the conventional structure. Considering these structure advantages, the SJ-PNM-IGBT with nanoscale mesa width indicates a potentially superior overall performance.

References

[1] Nakagawa A 2006 *IEEE 18th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jun. 4–8, 2006, Naples, Italy, p. 1

[2] Kamibaba R, Konishi K, Fukada Y, Narazaki A and Tarutani M 2015 *IEEE 27th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 10–14, 2015, Hong Kong, China, p. 29

[3] Wolter F, Roesner W, Cotorogea M, Geinzer T, Seider-Schmidt M and Kae-Horng W 2015 *IEEE 27th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 10–14, 2015, Hong Kong, China, p. 105

[4] Tanaka M and Omura I 2012 *IEEE 24th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jun. 3–7, 2012, Bruges, Belgium, p. 177

[5] Antoniou M, Udrea F, Bauer F, Mihaila A and Nistor I 2012 *IEEE 24th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jun. 3–7, 2012, Bruges, Belgium, p. 21

[6] Antoniou M, Lophitis N, Bauer F, Nistor I, Bellini M, Rahimo M, Amaratunga G and Udrea F 2015 *IEEE Electron Device Lett.* **36** 823

[7] Feng H, Yang W, Onozawa Y, Yoshimura T, Tamenori A and Sin J K O 2016 *IEEE 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jun. 12–16, 2016, Prague, Czech Republic, p. 203

[8] Zhang J P, Li Z H, Zhang B and Li Z J 2014 *Chin. Phys. B* **23** 088504

[9] Sumitomo M, Asai J, Sakane H, Arakawa K, Higuchi Y and Matsui M 2012 *IEEE 24th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jun. 3–7, 2012, Bruges, Belgium, p. 17

[10] Sumitomo M, Sakane H, Arakawa K, Higuchi Y and Matsui M 2013 *IEEE 25th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 26–30 2013, Kanazawa, Japan, p. 33

[11] Antoniou M, Udrea F and Bauer F 2010 *IEEE Trans. Electron Dev.* **57** 594

[12] Bauer F, Nistor I, Mihaila A, Antoniou M and Udrea F 2012 *International Semiconductor Conference (CAS)*, Oct. 15–17 2012, Sinaia, p. 27

[13] Luther-King N, Sweet M and Madathil Sankara N E 2012 *IEEE Trans. Power Electron.* **27** 3072

[14] Hsieh A P S, Camuso G, Udrea F, Chiu N, Yi T, Vytla R K, Ranjan N and Charles A 2015 *IEEE 27th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 10–14, 2015, Hong Kong, China, p. 137

[15] Liu B, Lin X N, Jiang F X C and He J 2013 *Advanced Materials Research* **677** 334

[16] Wonsuk C, Dongkook S and Dongwook K 2014 *International Power Electronics Conference (IPEC)*, May 18–21, 2014, Hiroshima, Japan p. 2914

[17] Tan J, Zhu Y J, Lu S J, Tian X L, Teng Y, Yang F, Zhang G Y and Shen Q X 2016 *Acta Phys. Sin.* **65** 158501 (in Chinese)

[18] Zhu J, Yang Z, Sun W, Sun Y, Zhou J, Zhu Y, Ye P and Li Z 2016 *IEEE 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jun. 12–16, 2016, Prague, Czech Republic, p. 331

[19] Eikyu K, Sakai A, Matsuura H, Nakazawa Y, Akiyama Y, Yamaguchi Y and Inuishi M 2016 *IEEE 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Jun. 12–16, 2016, Prague, Czech Republic, p. 211

[20] Mori M, Oyama K, Kohno Y, Sakano J, Uruno J, Ishizaka K and Kawase D 2007 *IEEE Trans. Electron Devices* **54** 2011