TOPICAL REVIEW — 2D materials: physics and device applications

A review for compact model of graphene field-effect transistors*

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Graphene has attracted enormous interests due to its unique physical, mechanical, and electrical properties. Specially, graphene-based field-effect transistors (FETs) have evolved rapidly and are now considered as an option for conventional silicon devices. As a critical step in the design cycle of modern IC products, compact model refers to the development of models for integrated semiconductor devices for use in circuit simulations. The purpose of this review is to provide a theoretical description of current compact model of graphene field-effect transistors. Special attention is devoted to the charge sheet model, drift-diffusion model, Boltzmann equation, density of states (DOS), and surface-potential-based compact model. Finally, an outlook of this field is briefly discussed.

Keywords: two-dimensional material, graphene, field-effect transistor, compact model

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1. Introduction

As a two-dimensional material with honeycomb structure, graphene has attracted enormous interests because of its unique properties since its debut in 2004.[1–3] Its unique physical, mechanical, and electrical properties have drawn a lot of interests among scientists.[4–6] Graphene not only exhibits excellent optoelectronic and mechanical properties but also can provide good adhesion with several organic materials so as to produce high-performance organic field-effect transistors.[7–10] Compared with conventional semiconductors, such as silicon, graphene shows completely different properties, for example, it is a zero-overlap semiconductor with very high electrical conductivity, and its conduction and valence bands meet at the Dirac point. For semiconductors, the flow of electricity requires some kinds of activation (such as heat or light absorption) to get over the gap between the valence band and conduction band. If the semiconductor is activated by an external electric field to switch on and off, then it is called field-effect transistors (FETs).[11,12] A FET consists of a gate, a channel region connecting source and drain electrodes, and a barrier separating the gate from the channel, as shown in Fig. 1(a). The operation of a conventional FET relies on the control of the channel conductivity, and thus the drain current, by a voltage (V_{GS}) applied between the gate and the source. The corresponding transfer characteristics curve of FET is shown in Fig. 1(c). Generally speaking, the large-scale and bilayer graphene does not possess a band gap. However, constraining large-scale graphene in one dimension or applying an electric field perpendicularly on the bilayer graphene can induce a band gap.[13–15] Recently, both theoretical and experimental works have achieved the graphene FETs.[16–18] Figure 1(b) shows a structure of top-gated graphene FET (GFET). The corresponding transfer characteristics curve for two GFETs with large-area-graphene channel is shown in Fig. 1(d). One can see in Fig. 1 that, due to the structure different between conventional MOSFET and GFET, the transfer characteristics curve shows entirely different features. For example, the transfer characteristics curves of GFETs have two kinds of conductions, i.e., hole conduction and electron conduction, while MOSFET has a unique current–voltage transfer characteristic.

Semiconductor device model, being a connection bridge between semiconductor manufactures and circuit designers, plays a critical role in semiconductor industry.[19,20] With the development of CMOS technology, which brings plenty of new physical effects, semiconductor device model has rapidly developed. Currently, integrated circuit (IC) designers use various kinds of software (such as SPICE, SLIC, PHILIPAC) in circuit design.[21–23] The core of the corresponding software is the model of each unit device. Because an integrated circuit includes plenty of transistors, if all unit devices use the complicated model of transistor, the system level simulation will beyond computer ability and hence results in non-convergence in calculation. On the other hand, the transistor model can accurately describe its physical properties in order to ensure the reliability of the calculated result.

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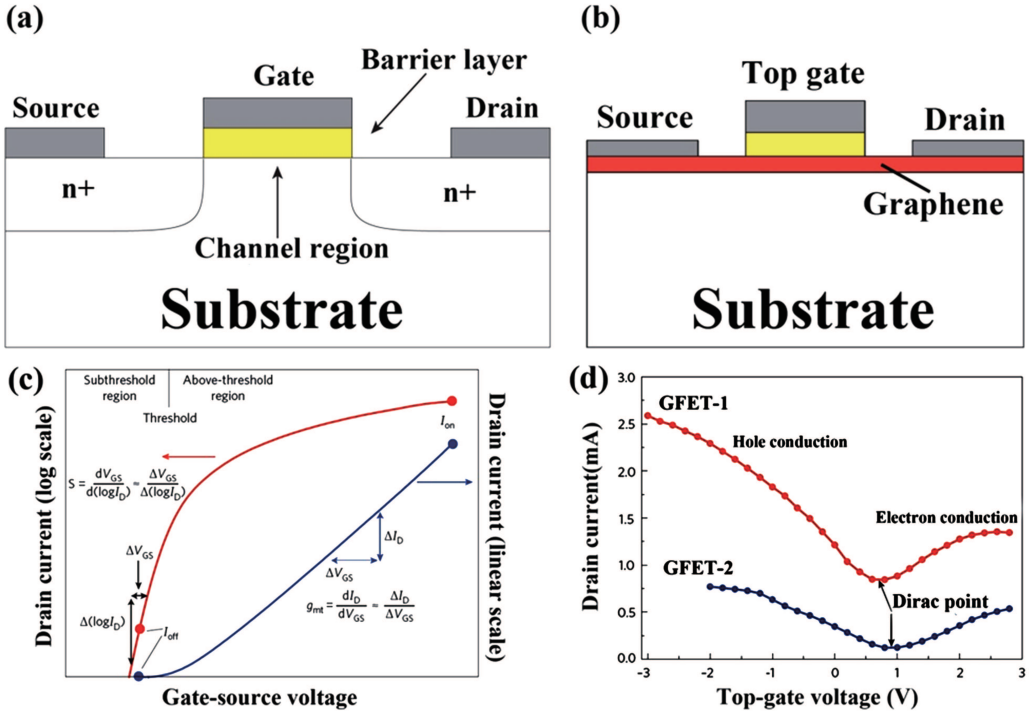


Fig. 1. (color online) Cross-section of (a) a n-channel MOSFET and (b) a top-gated graphene FET, (c) MOSFET transfer characteristics showing I_D (on a logarithmic scale on the left and a linear scale on the right) versus the gate-source voltage (V_{GS}), and (d) transfer characteristics curves for two GFETs with large-area-graphene channel.[11]

It is reasonable to state what a compact model is, since one may see differences in interpretations in the past. The following requirements for an excellent compact model have been considered in Refs. [24] and [25].

(i) Must represent consistently the behavior of FET device.

(ii) Must be symmetrical to reflect the symmetry of FET structure.

(iii) Has to be analytical, without differentials or integrals. Could be in a matrix format but must not be a finite element model.

(iv) Has to be simple and easily derivable. No compromises with the overall FET behavior but some freedom for simplifications should be allowed, neglecting details that deviate from experimental trends, are insignificant in magnitude, or are not reproducible in identical devices and measurements. In other words, one should have a generic model.

(v) Has to have parameters that can be characterized relatively easy, or even guessed.

(vi) Has to be upgradable and reducible. Consequently, different portions and dependences (e.g., on temperature) in the model can be replaced with different models. Thus, the different portions in the model are extensions of each other, and the portions communicate between each other only by the values of the parameters or the quantities but the relations in the different portions must remain separated.

(vii) Has to have relations that can be physically justified.

(viii) Should have similar form and correspondence to compact models for other FETs.

(ix) Should be tunable to inaccurate (or uncertain) experimental data. Consequently, scaling rules can be left external, since these rules can be obscured by individual devices and different measurements.

Compact model is a critical step in the design cycle of modern IC products.[26] It refers to the development of models for integrated semiconductor devices for use in circuit simulations. The models are used to reproduce device terminal behaviors with accuracy, computational efficiency, ease of parameter extraction, and relative model simplicity for a circuit or system-level simulation, for future technology nodes.[27] Physics-based models are often preferred, particularly when concerned with statistical or predictive simulation. The industry's dependence on accurate and time-efficient compact models continues to grow as circuit operating frequencies increase and device tolerances scale down with concomitant increases in chip device count, and analog content in mixed-signal circuits. Accurate and physics-based compact models are useful for the design and development of FETs for digital and analog circuits. These models are highly desirable because they offer better computational efficiency than their numerical alternatives without loss of physical insights. Since Kacprzak *et al.* reported firstly the compact DC model of GaAs-FETs in 1983,[28] the compact model for FETs has received much attention.[29–33] Figure 2 shows the Thomson Reuters Web of Science publication report for the topic "Compact Model for Field-Effect Transistors" in the last 20 years and "Compact

Model for Graphene FET". Research interest in the compact model has been growing remarkably over the last 10 years. The earliest compact model for graphene FET was reported by Meric *et al.* in 2008,[34,35] which is based on the charge sheet model of MOSFET. Following Meric's model, several evolving compact models have been established,[36–39] such as, virtual-source current–voltage model, SPICE-compatible compact model, and electrical compact model, etc. With the decrease of channel lengths to below 50 nm, traditional compact models lose validity. To satisfy the scale-down requests, the quasi ballistic FET model has been developed for nano scale FETs.[40] However, due to the difference of structure and transport feature between MOSFET and GFETs, the model of MOSFET maybe not entirely practicable to GFETs. Some new compact models, for example, based on a drift-diffusion model[41–45] and Boltzman equation,[46] have also been developed. Further, some new physical-based compact models, such as surface-potential-based[47,48] and based on density of states (DOS),[49–51] have been developed to achieve high accuracy and more physical.

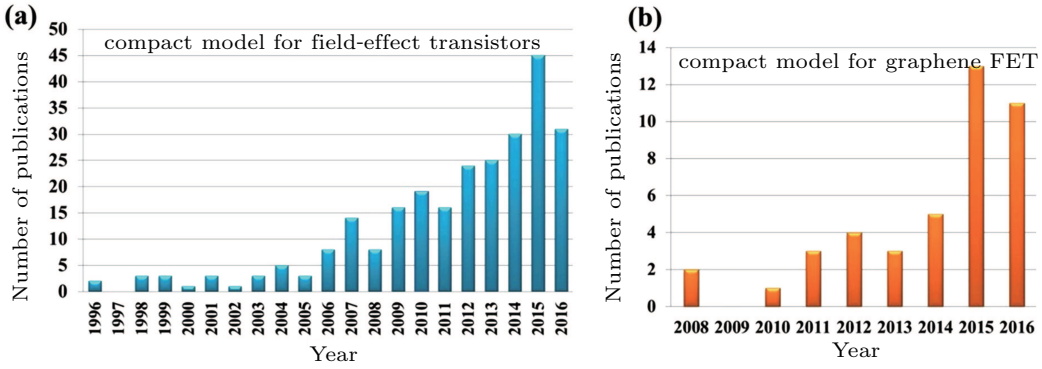


Fig. 2. (color online) Thomson Reuters Web of Science publication report for the topic, (a) "Compact Model for Field-Effect Transistors" in the last 20 years, and (b) "Compact Model for Graphene FET".

There have been some excellent reviews published recently with emphasis on the basic science of graphene and graphene FETs.[7,11,52–57] Given the growing interest in graphene in the electron-device community, and ongoing discussions of the potential of graphene transistors, a review article focusing on compact model of graphene FETs is timely. In this review, we mainly focus on the compact model of graphene FETs based on different methods, including not only based on conventional MOSFET model but also new physical-based model. In Section 2, the theoretical basis of compact model is discussed. In Sections 3–7, the charge sheet model, drift-diffusion model, Boltzmann equation, surface-potential-based compact model and the model based on density of states (DOS) are summarized. Finally, the future outlook for this field is briefly discussed in Section 8.

2. Theoretical basis of compact model

As mentioned above, the first compact model for FETs was proposed by Kacprzak *et al.* in 1983.[28] After more than 30 years, several researchers have developed various compact models for FETs. All these proposed compact models can be divided into two categories, one is charge-based and the other is surface-potential-based. Next, we will describe the theoretical basis of compact models developed from charge-based and surface-potential-based, respectively.

2.1. Charge sheet model

The charge sheet model is applied to long-channel devices. As compared with other models, such as Pao-Sah model,[58] the charge sheet model leads to a very simple algebraic formula for the current of long-channel devices, which can be used in all regimes from subthreshold to saturation. The charge sheet model firstly assumes a quasi-Fermi level formulation for carrier densities and the coordinate system. The source-to-drain current I can be related to the average quasi-Fermi level gradient $\mathrm{d}\bar{\Phi}_{\mathrm{f}}/\mathrm{d}y$ and the carrier density per unit area $N(y)$[59]

$$I = Zq\mu N(y)\mathrm{d}\bar{\Phi}_{\mathrm{f}}/\mathrm{d}y, \tag{1}$$

where Z is the channel width, μ is the effective mobility, q is the elementary charge, and y is the measured distance along the channel from the source toward the drain, $N(y) = \int_0^{\infty} \mathrm{d}x[n(x,y) - n_{\mathrm{f}}(x,y)]$. $n - n_{\mathrm{f}}$ is the minority carrier density per unit volume in excess of the zero band-banding density n_{f}. $\mathrm{d}\bar{\Phi}_{\mathrm{f}}/\mathrm{d}y$ can be simply approximated by

$$\frac{\mathrm{d}\bar{\Phi}_{\mathrm{f}}}{\mathrm{d}y} = \frac{\mathrm{d}\Phi_{\mathrm{s}}}{\mathrm{d}y} - \frac{1}{\beta}\frac{\mathrm{d}\ln N}{\mathrm{d}y}, \tag{2}$$

where $\Phi_{\mathrm{s}}(y)$ is the potential along the oxide–silicon interface and $\beta = q/(k_{\mathrm{B}}T)$. By integrating Eq. (2), one can obtain

$$N(y) = N(0)\exp\left\{\beta\left[\Phi_{\mathrm{s}}(y) - \Phi_{\mathrm{s}}(0)\right] - \beta\left[\bar{\Phi}_{\mathrm{f}}(y) - \bar{\Phi}_{\mathrm{f}}(0)\right]\right\}. \tag{3}$$

That is, equation (2) is equivalent to the assumption that the carrier density along the channel varies only because the inversion layer moves rigidly with respect to the quasi-Fermi level as the potential varies. All shape dependence of the inversion layer upon carrier density or normal field is contained in $N(0)$ and remains unaltered from source to drain.

By substituting Eq. (2) into Eq. (1), one can solve Eq. (1) for $N(y)$ to obtain

$$N(y) = N(0)\exp\{\beta[\Phi_s(y)-\Phi_s(0)]\} - \frac{I}{k_B T\mu Z}\exp(\beta\Phi_s(y))\int_0^y \mathrm{d}y_0 \exp(-\beta\Phi_s(y_0)). \quad (4)$$

The model is then addressed by using Poisson's equation for the potential

$$\begin{cases} \nabla^2\Phi = 0, & \text{in gate oxide,} \\ \nabla^2\Phi = -\dfrac{q(p-N_A)}{\kappa\varepsilon_0}, & \text{in silicon,} \end{cases} \quad (5)$$

where one can assume p-type material. Equation (5) is joined across the oxide–silicon interface by the discontinuity condition

$$\kappa_{ox}\varepsilon_0 \left.\frac{\partial\Phi}{\partial x}\right|_{o^-} - \kappa_{sc}\varepsilon_0 \left.\frac{\partial\Phi}{\partial x}\right|_{o^+} = -qN(y), \quad (6)$$

where (o^-) refers to evaluation on the oxide side of the interface, o^+ on the silicon side. The x-coordinate measures the normal distance from the interface to the silicon. Equation (6) implies that $N(y)$ is contained in a charge sheet of zero thickness. This in turn means that (i) the current is constrained to flow along the oxide–silicon interface, and (ii) there is no voltage drop across the inversion layer. Using some arbitrary $\Phi_s(y) \equiv \Phi(x=0,y)$, one can solve Eq. (5) for Φ in both oxide and semiconductor. This determines the normal derivatives in Eq. (6). Using Eq. (4), one can obtain an integral equation for $\Phi_s(y)$. This equation now will be set up and solved for long channel devices.

2.2. Boltzmann equation

In order to model the transport characteristics of the GFET, one can split carrier distribution function into its even and odd parts, that is, $f(\boldsymbol{k}) = f_{even}(\boldsymbol{k}) + f_{odd}(\boldsymbol{k})$. Then, it is well known that in the presence of randomizing collisions, and even in high fields, the Boltzmann transport equation can be written as[46,60]

$$\frac{qF}{\hbar}\frac{\partial}{\partial k_x} f_{even}(\boldsymbol{k}) = -\frac{1}{\tau_{tot}(k)} f_{odd}(\boldsymbol{k}), \quad (7)$$

with $\frac{1}{\tau_{tot}(k)} = \sum_i \frac{1}{\tau_i(k)}$ and the i-index indicates a particular scattering mechanism. In the presence of strong inter-carrier scattering for high carrier concentration, the even part of the distribution is thermalized at an electronic temperature T_e, and reads as

$$f_{even}(\boldsymbol{k}) = \frac{1}{1+\exp[(\hbar v_F)(k-k_F)/(k_B T_e)]}, \quad (8)$$

where $k_F = k_F(x)$ defines the carrier concentration along the channel. In p-channel, the current can be calculated as

$$\boldsymbol{I} = \frac{4q}{L}\sum_{\boldsymbol{k}} \boldsymbol{v}(\boldsymbol{k}) f_{odd}(\boldsymbol{k}), \quad (9)$$

where L is the channel length, and the factor 4 accounts for the spin and the two-fold degeneracy of the Dirac point. Here, $v(\boldsymbol{k}) = vF(\cos\theta, \sin\theta)$ and θ is the angle between the electric field and the vector $\boldsymbol{k}$. Then for $\hbar v_F k_F \gg k_B T_e$, one can approximate $(\partial/\partial k_x) f_{even}(\boldsymbol{k})$ by a delta function centered around k_F. After integrating and setting $k_F = \sqrt{\pi p}$,[61] the hole current in a 2D graphene layer reads

$$I = W\frac{2q^2}{h} F v_f \tau(p)\sqrt{\pi p}, \quad (10)$$

where W is the graphene layer width, p is the hole concentration, F is the electric field, and $\tau(p)$ is the relaxation time (inverse scattering rate) for a particular carrier concentration p. In the high field regime, one can assume $\tau(p) = \tau_{lf}/(1+F/F_c)$, where F_c is the critical electric field for the onset of high energy collisions such as remote phonons,[62] for instance, $\tau_{lf}(p) = \tau_0\sqrt{p/N_i}$ is the low-field relaxation time dominated by scattering with charged impurities with density N_i, and τ_0 is a time constant. By setting $\mu_0 = (q/\hbar)v_F\tau_0\sqrt{p/N_i}$, one recovers the conventional current expression

$$I = WqpV(F), \quad (11)$$

with $v(F) = \mu_0 F/(1+F/F_c)$, where the low-field conductance $\sigma_{lf} \propto p$, as observed experimentally.[61]

2.3. Drift-diffusion carrier transport

In semiconductor physics, the drift-diffusion equation is related to drift current and drift velocity. The equation at the steady state for electrons and holes, respectively, is normally written as[20,63]

$$\begin{cases} \dfrac{J_n}{-q} = -D_n\nabla_n - n\mu_n E, \\ \dfrac{J_p}{q} = -D_p\nabla_p + p\mu_p E, \end{cases} \quad (12)$$

$$\begin{cases} \dfrac{\partial n}{\partial t} = -\nabla\dfrac{J_n}{-q} + R, \\ \dfrac{\partial p}{\partial t} = -\nabla\dfrac{J_p}{-q} + R, \end{cases} \quad (13)$$

where n and p are the concentrations (densities) of electrons and holes, respectively, J_n and J_p are the electric currents due to electrons and holes, respectively, $\frac{J_n}{-q}$ and $\frac{J_p}{-q}$ are the corresponding "particle currents" of electrons and holes, respectively, R represents carrier generation and recombination, E is

the electric field vector, and μ_n and μ_p are electron and hole mobilities, respectively.

The diffusion coefficient and mobility are related by the Einstein relation[64]

$$\begin{cases} D_n = \dfrac{\mu_n k_{\rm B} T}{q}, \\ D_p = \dfrac{\mu_p k_{\rm B} T}{q}. \end{cases} \tag{14}$$

The drift and diffusion currents refer separately to the two terms in the expressions for J

$$\begin{cases} \dfrac{J_{\rm drift}}{-q} = -n\mu E, \\ \dfrac{J_{\rm diffusion}}{-q} = -n\mu E, \end{cases} \tag{15}$$

where μ is the mobility (μ_n (μ_p)) of electrons (holes)

2.4. Density of states (DOS)

The density of states for monolayer graphene is expressed as[65]

$$\mathrm{DOS}(E) = 2|E|/\pi(\hbar v_{\rm F})^2, \tag{16}$$

And the Fermi level varies linearly with the voltage drop (i.e. $V_{\rm CH}$) across the quantum capacitance $C_{\rm q}$, which implies that $E_{\rm F} = qV_{\rm CH}$.

The DOS for bilayer graphene can be written as[66]

$$\mathrm{DOS}(E) = \frac{2m_{\rm eff}}{\pi\hbar^2}\left[H\left(E - \frac{E_{\rm g}}{2}\right) + H\left(-E - \frac{E_{\rm g}}{2}\right)\right], \tag{17}$$

where $m_{\rm eff} = A$ is the effective mass, $E_{\rm g}$ is the bilayer energy bandgap, $\hbar$ is the reduced Planck constant, H is the Heaviside step function, and A is a fitting parameter.

2.5. Surface potential

Surface potential $\varphi_{\rm s}$, i.e., the potential at the interface is an implicit function of the terminal voltages that is usually obtained by solving the surface potential equation (SPE) occasionally known also as the input voltage equation.[67] It is derived under several simplifying assumptions essential in the compact model formulation. The first simplification is the Shockley's gradual channel approximation (GCA) that assumes

$$\left|\frac{\partial^2\varphi}{\partial y^2}\right| \ll \left|\frac{\partial^2\varphi}{\partial x^2}\right|, \tag{18}$$

where φ denotes the electrostatic potential. With this simplification, the Poisson equation becomes

$$\frac{\partial^2\varphi}{\partial x^2} = -\frac{\rho}{\varepsilon_{\rm s}}, \tag{19}$$

where ρ denotes the charge density and $\varepsilon_{\rm s}$ is the dielectric permittivity. By denoting the electron and hole concentrations as n and p respectively,

$$\rho = q(p - n - N_{\rm a}^-), \tag{20}$$

where $N_{\rm a}^-$ is the concentration of ionized acceptors and one can consider an n-channel MOS device. Since the hole current component is negligible, it is the gradient of the hole imref F_p and the hole concentration is given by the Boltzmann relation $p = p_{\rm b}\exp(-\beta\varphi)$ where $\beta = 1/\phi_{\rm t}$ and $\phi_{\rm t}$ denotes the thermal potential. This form assumes that the reference point for the potential is in the neutral bulk region, where the majority and minority carrier concentrations are $p_{\rm b}$ and $n_{\rm b}$ respectively. For electrons, it is necessary to take into account the imref gradient so that

$$n = n_{\rm b}\exp[\beta(\varphi - \phi_n)], \tag{21}$$

where the normalized imref splitting (a.k.a."channel voltage")

$$\phi_n = (1/q)(F_p - F_n). \tag{22}$$

For most applications, it is sufficient to assume the complete ionization of the channel dopants. Then $N_{\rm a}^-$ coincides with the total acceptor concentration $N_{\rm a} = p_{\rm b} - n_{\rm b}$ (for the uniformly doped channel). Hence

$$\rho = q\left[p_{\rm b}(\exp(-\beta\varphi) - 1) - n_{\rm b}(k\exp(-\beta\varphi) - 1)\right], \tag{23}$$

where $k = \exp(-\beta\phi_n)$.

From Eq. (19) and the boundary condition $\partial\varphi/\partial x = 0$ for $\varphi = 0$, it follows that

$$E_{\rm s}^2 = -\frac{2}{\varepsilon_{\rm s}}\int_0^{\varphi_{\rm s}} \rho\,{\rm d}\varphi, \tag{24}$$

where the surface electric field $E_{\rm s} = -({\rm d}\varphi/{\rm d}x)_{x=0}$. Continuity of the normal component of the displacement vector at the Si/SiO_2 interface provides SPE in the form

$$(V_{\rm gb} - V_{\rm fb} - \varphi_{\rm s})^2 = \gamma^2\phi_{\rm t}h, \tag{25}$$

where $V_{\rm fb}$ is the flat-band voltage, $\gamma = \sqrt{2q\varepsilon_{\rm s}p_{\rm b}}/C_{\rm ox}$ denotes the body factor, unit area oxide capacitance $C_{\rm ox} = \varepsilon_{\rm ox}/t_{\rm ox}$, $t_{\rm ox}$ is the oxide thickness, and $\varepsilon_{\rm ox}$ is the oxide permittivity. The dimensionless variable h represents the normalized square of the surface electric field

$$h = \frac{\varepsilon_{\rm s}E_{\rm s}^2}{2q\phi_{\rm t}p_{\rm b}} = -\frac{1}{q\phi_{\rm t}p_{\rm b}}\int_0^{\varphi_{\rm s}} \rho\,{\rm d}\varphi. \tag{26}$$

3. Charge sheet compact model

The first compact model for GFET was proposed by Meric *et al.* based on charge sheet model.[34,35] In Meric's model, it is assumed that a top-gated graphene FET is based on a high-k gate dielectric without bandgap engineering. And the GFETs have source and drain regions that are electrostatically doped by the back gate, which enables control over the

contact resistance and threshold voltage of the top-gated channel. Then, the sheet carrier concentrations (electrons or holes) in the source and drain regions are given as

$$n \cong \sqrt{n_0^2 + \left(C_{\text{back}}\left(V_{\text{gs-back}} - V^0_{\text{gs-back}}\right)/q\right)^2}, \quad (27)$$

where $V^0_{\text{gs-back}}$ and $V_{\text{gs-back}}$ are the back-gate-to-source voltage and back gate voltage at the Dirac point in these regions, respectively, and n is the minimum sheet carrier concentration as determined by disorder and thermal excitation. C_{back} is the back-gate capacitance Under the top gate, the carrier concentrations are determined by both the front and back gates

$$n = \sqrt{n_0^2 + \left(C_{\text{top}}\left(V_{\text{gs-top}} - V_0\right)\right)^2}, \quad (28)$$

where V_0, which has the character of a threshold voltage, is given by

$$V_0 \cong V^0_{\text{gs-top}} + \frac{C_{\text{back}}}{C_{\text{top}}}\left(V^0_{\text{gs-back}} - V_{\text{gs-back}}\right).$$

$V^0_{\text{gs-top}}$ is the top-gate-to-source voltage, C_{top} is the top-gate capacitance and given by the parallel combination of the electrostatic capacitance of the gate and the quantum capacitance of graphene.

Then, the carrier concentration dependence of the distance in the channel, shown schematically in Fig. 3 for different points in the I–V trace, is calculated using a field-effect model

$$n(x) = \sqrt{n_0^2 + \left(C_{\text{top}}\left(V_{\text{gs-top}} - V(x) - V_0\right)/q\right)^2}. \quad (29)$$

With this consideration, the current in the channel is express by[68]

$$I_{\text{d}} = \frac{W}{L}\int_0^L qn(x)\, v_{\text{drift}}(x)\, \text{d}x, \quad (30)$$

where L is the channel length and W is the channel width. Current continuity forces a self-consistent solution for the potential $V(x)$ along the channel. Here the carrier drift velocity (v_{drift}) is approximated by a velocity saturation model[69]

$$v_{\text{drift}}(x) = \frac{\mu E}{1 + \mu E / v_{\text{sat}}}, \quad (31)$$

where v_{sat} is the saturation velocity of the carriers.

By combining Eqs. (29)–(31), the final current in the channel can be obtained as

$$I_{\text{d}} = \frac{\frac{W}{L} q\mu \int_0^{V_{\text{sd}}} \sqrt{n_0^2 + \left(C_{\text{top}}\left(V_{\text{gs-top}} - V(x) - V_0\right)/q\right)^2}}{1 + \frac{\mu V_{\text{sd}}}{L v_{\text{sat}}}}. \quad (32)$$

Figure 4 shows the results of simple field-effect modeling of the devices, compared with the measured I–V characteristics of GFET. This field-effect model is also implemented in Verilog-A with the equations. Here, R_{s} is approximately 100 Ω (700 Ω) for two kinds of GFET devices, i.e., GFET A and GFET B. GFET A has a low-field mobility $\mu = 10^5$ cm^2/V·s and $n = 5 \times 10^{12}$ cm^{-2}, compared with $\mu = 1200$ cm^2/V·s and $n = 0.5 \times 10^{12}$ cm^{-2} for GFET B.

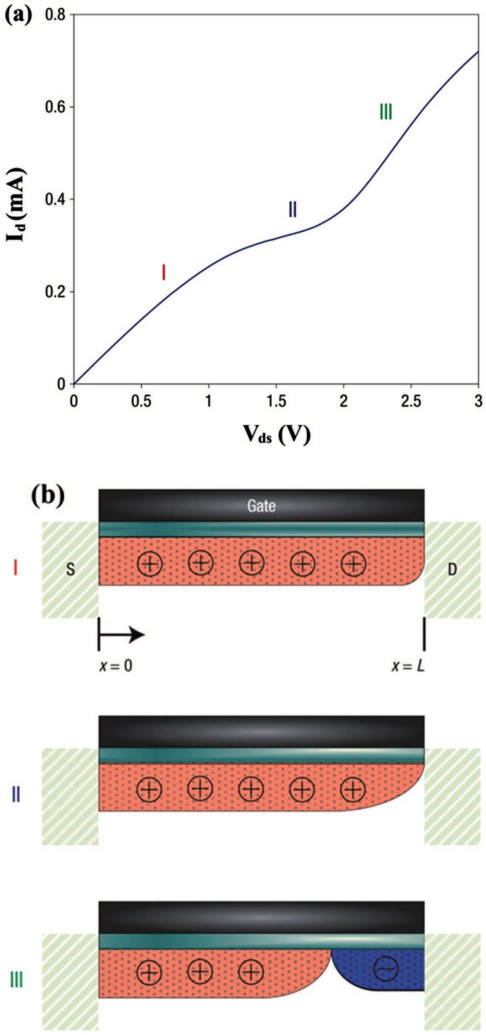


Fig. 3. (color online) (a) Measured I–V characteristic at $V_{\text{gs-back}} = 40$ V and $V_{\text{gs-top}} = 0.3$ V in GFET devices. Three points (I, II, and III) are indentified in the I–V curve. (b) Schematic demonstration of the carrier concentration under the top-gated region. At point I (V_{sd} , $V_{\text{sd-kink}}$, here $V_{\text{sd-kink}}$ means the V_{sd} of "kink" between I and II, or II and III in panel (a)), the channel charge at the drain end begins to decrease as the minimal density point enters the channel. At point II ($V_{\text{sd}} < V_{\text{sd-kink}}$), the minimal density point forms at the drain. For $V_{\text{sd}} > V_{\text{sd-kink}}$ (point III), an electron channel forms at the drain.[35]

Based on the Meric's model, Lee *et al.* have developed a compact model of extremely scaled graphene FETs.[38] In Lee's model, an electron–hole puddle existing near the charge-neutral region (Dirac point) is considered at a low carrier density while the velocity saturation effect due to surface polar phonon scattering is included at a high carrier density. Frégonèse *et al.* also proposed an electrical compact model for graphene FET device[39] at which, a trap model is introduced and the equivalent circuit is improved. And traps have an effect on the transconductance and influence consequently most figures of merit in circuit design. The electrical compact mode has been verified by comparison to DC and AC mea-

surements versus bias and frequency on an advanced GFET having a transit frequency of about 10 GHz.

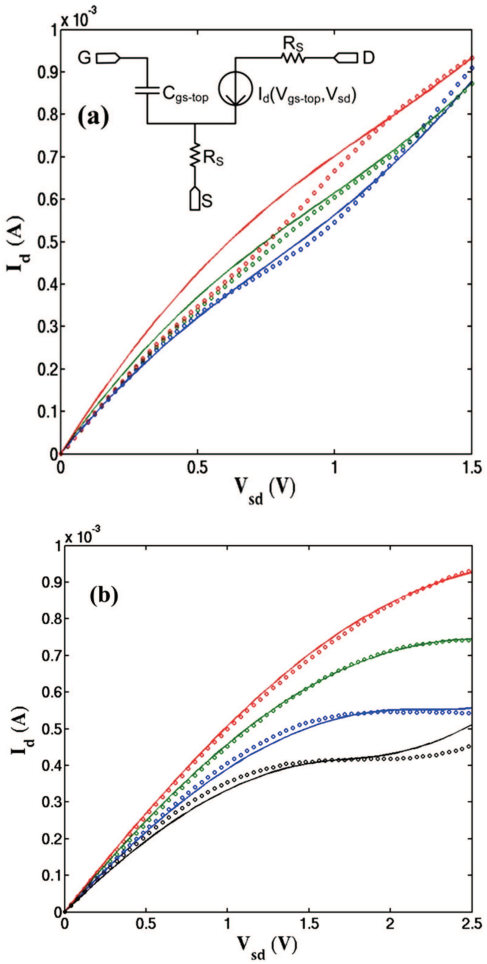


Fig. 4. (color online) Current–voltage characteristics of GFET device. Drain current I_d as a function of source-to-drain voltage V_{sd} (a) for GFET A at $V_{gs-top} = -0.1$ V, -0.3 V, -0.5 V and (b) for GFET B at $V_{gs-top} = 0$ V, -0.5 V, -1.5 V, -2.5 V (from bottom to top), respectively. Both measured (solid curves) and simulated (dashed curves) results are shown. Inset is the equivalent circuit for the corresponding compact model of GFET.[34]

Although Meric's model has firstly been developed and shown good agreement between experimental data and simulated results of drain current, due to the difference between MOSFET and GFETs, it maybe not entirely practicable to GFETs.

4. Compact model based on Boltzmann equation

To build a compact model accurately reflecting the characteristics of GFETs, researchers have presented the model based on Boltzmann equation.[46] Here, the graphene monolayer is assumed to sit on a thick SiO_2 layer with capacitance C_{back} on top of a back gate that controls the source and drain resistance R_s, at the same time, as the channel threshold voltage with bias V_{gback}. A top gate of length L, separated from the graphene monolayer by a thinner oxide with capacitance C_{top}, controls the carriers in the channel with V_{gtop}. According to Boltzmann equation, by integrating the current of Eq. (11) from source to drain as in conventional MOS devices, and by taking into account the series resistance R_s at the source and drain,[35] Scott *et al.* have obtained the drain current[46]

$$I_d = \frac{W\mu_0 V_c}{2LC_{top}(|V_{ds}| - 2|I_d|R_s + V_c)}\left[Q(L)^2 - Q(0)^2\right], \quad (33)$$

where

$$Q(L) = -C_{top}(V_{g0} - V_{ds} - |I_d|R_s),$$
$$Q(0) = -C_{top}(V_{g0} + |I_d|R_s),$$

V_{g0} is the threshold voltage, here $V_{g0} = V_{gtop} - V_0$ and $V_0 = V_{top}^0 \dfrac{C_{back}}{C_{top}}(V_{gback}^0 - V_{gback})$, R_s is the resistance. By solving for I_d, a closed expression for the drain current is expressed as

$$I_d = \frac{1}{4R_s}\left[V_{ds} - V_c + I_0R_s + \sqrt{(V_{ds} - V_c + I_0R_s)^2 - 4I_0R_sV_{ds}}\right], \quad (34)$$

where V_{ds} is the drain-source voltage,

$$I_0 = 2(W/L)\mu_0 V_c C_{top}(V_0 - V_{ds}/2),$$

and $V_c = F_cL$, F_c is the critical field.

Here, the low drain-source bias conductance is readily calculated by taking the derivative of the current expression (Eq. (34)) with respect to V_{ds} as V_{ds} goes to zero. One obtains

$$g_{ds}(V_{ds} \to 0) = \frac{-V_{g0}}{|2R_sV_{g0} - R_cV_c|}, \quad (35)$$

where $1/R_c = (W/L)\mu_0 C_{top}V_c$, so that R_cV_c is independent of V_c, as is the conductance at low drain bias. The low drain-source bias resistance reads

$$R_{ds} = \frac{1}{g_{ds}} = 2R_s - \frac{R_cV_c}{V_{g0}}, \quad (36)$$

which establishes a linear relation between $1/g_{ds}$ and $1/V_{g0}$ with a slope given by R_cV_c (inversely proportional to the mobility) and an asymptotic conductance value for large V_{g0} reaching $2R_s$.

In the same context, one obtains the expression for the drain-source saturation voltage as a function of the top gate voltage V_{g0} by solving for V_{ds} after setting the derivative of the current from Eq. (34) with respect to V_{ds} equal to zero that yields

$$V_{ds(sat)} = \frac{2\gamma V_{g0}}{1+\gamma} + \frac{1-\gamma}{(1+\gamma)^2}\left[V_c - \sqrt{V_c^2 - 2(1+\gamma)V_cV_{g0}}\right], \quad (37)$$

with $\gamma = R_s/R_c$. Substituting Eq. (37) into Eq. (34), one can obtain the expression of the saturation drain current as a function of the top gate voltage, which reads

$$I_{d(sat)} = \frac{\gamma}{R_s(1+\gamma)^2}\left[-V_c + (1+\gamma)V_{g0}\right.$$

$$+\sqrt{V_c^2-2(1+\gamma)V_cV_{g0}}\Big]. \tag{38}$$

By taking the derivative of the saturation current with respect to the top gate voltage, one derives the expression for the transconductance at saturation

$$g_m^{sat}=\frac{1}{R_s+R_c}\left[1-\frac{1}{\sqrt{1-2(1+\gamma)V_{g0}/V_c}}\right]. \tag{39}$$

Figure 5 shows the plots of both the low-bias conductance g_{ds} as a function of the top gate voltage and the low-bias resistance R_{ds} as a function of the inverse of the top gate voltage in the device configuration investigated in Ref. [35]. In Fig. 5(a), the solid curve is calculated from Eq. (35), which shows good agreement with the experimental data close to the minimum conductance, but underestimates the former by about 20% at high top gate bias. In Fig. 5(b), the experimental resistance displays a linear relation with $1/V_{g0}$ in agreement with Eq. (36).

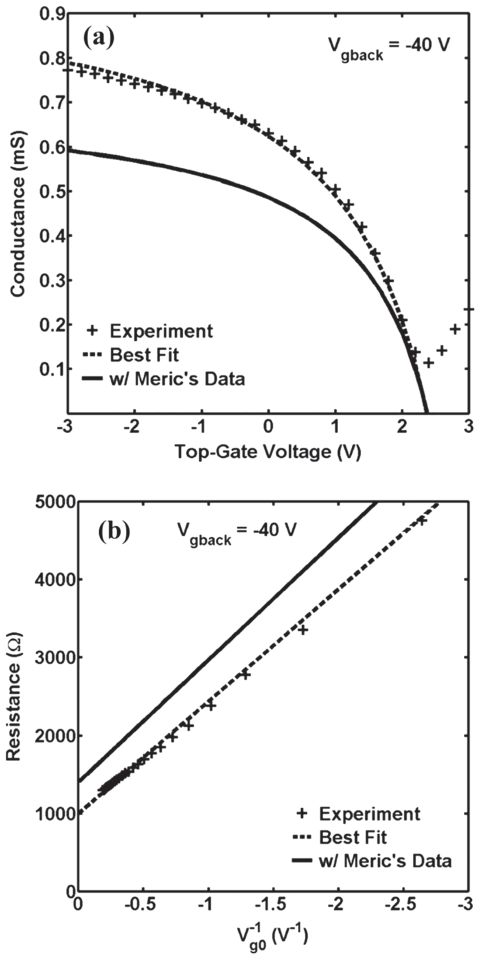


Fig. 5. (a) Small-signal source-drain conductance g_{ds} as a function of the top gate voltage minus the threshold voltage V_{g0}, and (b) small-signal source-drain resistance R_{ds} as a function of the inverse of the top gate voltage minus the threshold voltage $1/V_{g0}$.[46]

Figure 6(a) displays the I–V characteristics of the GFET. An excellent agreement between the experiment and simulated results from Eq. (34) is obtained. However, the mobility is 25% higher than Meric's fitted values.[35] Figure 6(b) shows the comparison between theoretical and experimental results for the p-channel conductance. The better fits are shown as compared with Meric's results.[35] Besides the simulated drain current, Scott *et al.* in their compact model have predicted a linear dependence of the low-field resistance versus the inverse gate voltage, and suggested that nonlinearity in the energy dispersion should be included, as well as carrier multiplication by impact ionization.

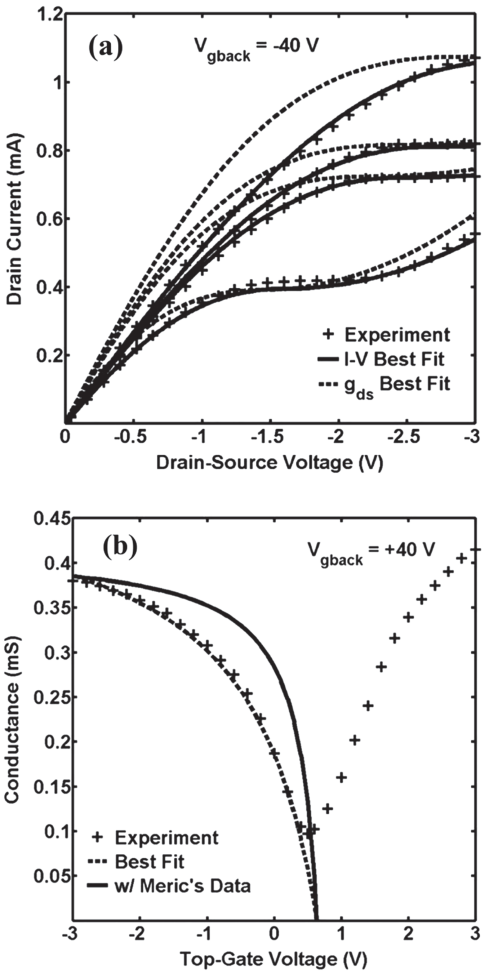


Fig. 6. (a) Small-signal source-drain current I_d as a function of drain-source voltage V_{ds}, and (b) small-signal source-drain conductance g_{ds} as a function of the top gate voltage minus the threshold voltage V_{g0}.[46]

5. Compact model based on drift-diffusion carrier transport

Based on drift-diffusion carrier transport, Jiménez *et al.* have presented a physics-based compact model of the current–voltage characteristics of GFET, of especial interest for analog and RF applications where band-gap engineering of graphene could not be needed.[41,42] They assumed that the electrostatics of this device is the equivalent capacitive circuit, in which the equivalent capacitive circuit C_t and C_b are the top and bottom oxide capacitances, and C_q represents the quantum capac-

itance of the graphene. Potential V_c represents the voltage drop across C_q, where $C_q = k|V_c|$ under condition $qV_c \gg k_B T$, with $k = (2q^2/\pi)\left(q/(\hbar v_F)^2\right)$, and $v_F\,(=10^6\ \mathrm{m/s})$ is the Fermi velocity. Potential $V(x)$ is the voltage drop in the graphene channel, which is zero at the source end at $x = 0$ and equal to drain-source voltage V_{ds} at the drain end at $x = L$. Then, to model the drain current, a drift-diffusion carrier transport is assumed under form

$$I_{ds} = -qW\rho_c(x)\,v(x), \tag{40}$$

where W is the gate width, $\rho_c(x) = |Q_c|/q$ is the free carrier sheet density in the channel at position x, and $v(x)$ is the carrier drift velocity. By using a soft-saturation model, consistent with Monte Carlo simulations,[70] $v(x)$ can be expressed as

$$v = \mu E/(1+\mu|E|/v_{sat}), \tag{41}$$

where E is the electric field, μ is the carrier low field mobility, and v_{sat} is the saturation velocity. The latter is concentration dependent and given by $v_{sat} = \Omega/\sqrt{\pi\rho_c}$. By applying $E = -\mathrm{d}V(x)/\mathrm{d}x$, combining the above expressions for v and v_{sat}, and integrating the resulting equation over the device length, the drain current becomes

$$I_{ds} = \frac{q\mu W\int_0^{V_{ds}}\rho_c\,\mathrm{d}V}{L+\mu\left|\int_0^{V_{ds}}\frac{1}{v_{sat}}\mathrm{d}V\right|}. \tag{42}$$

The denominator represents an effective length (L_{eff}) to take into account the saturation velocity effect. In order to get an explicit expression for I_{ds}, the integral in Eq. (42) is solved by using V_c as the integration variable and consistently expressing ρ_c and v_{sat} as a function of V_c,

$$I_{ds} = \frac{q\mu W\int_{V_{cs}}^{V_{ds}}\rho_c(V_c)\frac{\mathrm{d}V}{\mathrm{d}V_c}\mathrm{d}V_c}{L+\mu\left|\int_{V_{cs}}^{V_{ds}}\frac{1}{v_{sat}(V_c)}\frac{\mathrm{d}V}{\mathrm{d}V_c}\mathrm{d}V_c\right|}, \tag{43}$$

where V_c can be written as

$$V_c = \frac{-(C_t+C_b)+\sqrt{(C_t+C_b)^2 \pm 2k\left[(V_{gs}-V_{gs0}-V)C_t+(V_{bs}-V_{bs0}-V)C_b\right]}}{\pm k}. \tag{44}$$

The positive (negative) sign applies whenever $(V_{gs}-V_{gs0}-V)C_t+(V_{bs}-V_{bs0}-V)C_b > 0$. The channel potential at source V_{cs} is determined by $V_c(V=0)$. Similarly, the channel potential at drain V_{cd} is determined by $V_c(V=V_{ds})$. On the other hand, the charge sheet density can be written as $\rho_c(V_c) = kV_c^2/2q$. Extra term ρ_0 added to ρ_c accounts for the carrier density induced by impurities.[71] By inserting these expressions into Eq. (42), the following explicit drain current expression can be finally obtained:

$$I_{ds} = \frac{\mu W}{L_{eff}}\left\{q\rho_0 V_{ds} - \frac{k}{6}\left(V_{cd}^3 - V_{cs}^3\right) - \frac{k^2}{8(C_t+C_b)}\left(\mathrm{sgn}(V_{cd})V_{cd}^4 - \mathrm{sgn}(V_{cs})V_{cs}^4\right)\right\}. \tag{45}$$

To test the model, Jiménez *et al.* have benchmarked the resulting *I–V* characteristics with experimental results extracted from devices in Refs. [35] and [72], as shown in Fig. 7. The first device under test has $L = 1$ μm and $W = 2.1$ μm, top dielectric is HfO_2 of 15 nm, and permittivity is ~ 16, and the bottom dielectric is silicon oxide of 285 nm. The back-gate voltage was -40 V. The flat-band voltages V_{gs0} and V_{bs0} were tuned to 1.45 V and 2.7 V, respectively. These values were selected to locate the Dirac point according to the experiment. Figure 8 shows the resulting *I–V* characteristics. Here the authors have extended the simulated voltage range beyond the experiment range to show the predictive behavior of the model. The transfer characteristics exhibit an ambipolar behavior dominated by holes (electrons) for $V_{gs}-V_{gs0} < V_{gs,D}\,(>V_{gs,D})$ where $V_{gs,D}$ (Dirac gate voltage) is given by $V_{gs,D} = V_{gs0}+V_{ds}/2$. The output characteristics are similar to those of the first examined device. Once again, the comparison between the model and experiment further demonstrates the accuracy of the model.

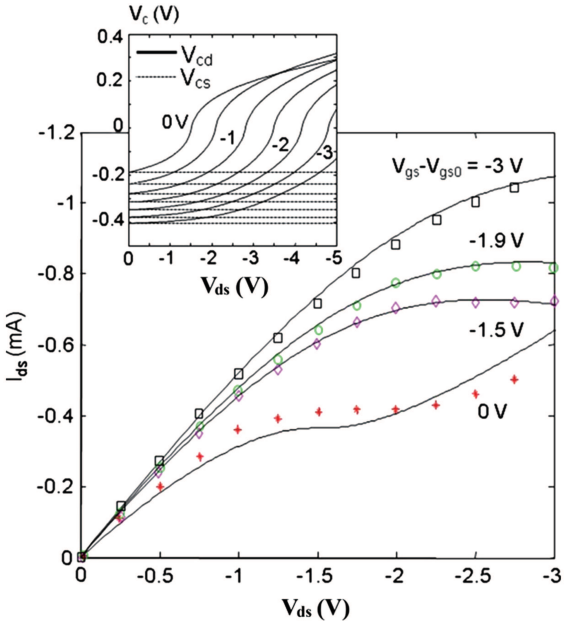


Fig. 7. (color online) Output characteristics obtained from the analytical model (solid lines) compared with experimental results (symbols) from Ref. [35]. Inset: quantum capacitance voltage drop as a function of the source-drain voltage for different gate voltage overdrive.[42]

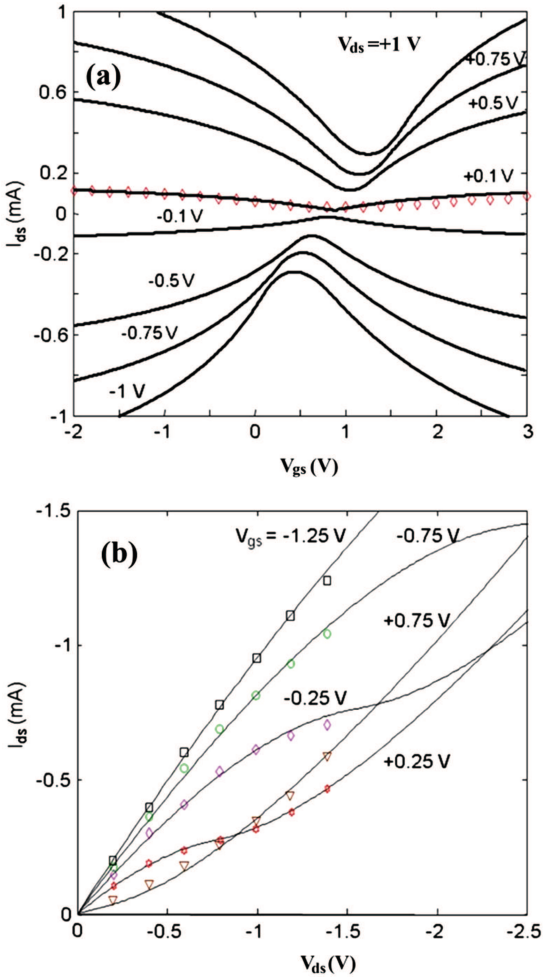


Fig. 8. (color online) (a) Transfer and (b) output characteristics obtained from the compact model (solid lines) compared with experimental results (symbols) from Refs. [42] and [72].

Based on drift-diffusion carrier transport, Jiménez *et al.* have presented a physics-based compact model of current–voltage characteristics of GFETs, which can capture the physics of all operation regions within a single expression for the drain current and each terminal charge and capacitance. At the same time, it is of special interest as a tool for the design of analog and RF applications. Additional physical effects, for example, short-channel effects, nonquasi-static effects, extrinsic capacitances, and mobility model, need to be incorporated into the long-channel core presented here to build a complete GFET compact model.

6. Compact model based on density of states

To evaluate the capabilities of electronic devices based on graphene as a channel material, accurate models are desired. Some new compact models based on physics-based DOS have also been developed. For example, Aguirre–Morales *et al.* have developed a new compact model for monolayer graphene FETs and dual-gate bilayer GFET by using a physics-based DOS to simulate the current and the charge, respectively.[32,49–51]

6.1. Monolayer graphene FETs

For the monolayer graphene FETs, the model considering the 2D DOS of monolayer graphene is used as Eq. (16). The corresponding device and equivalent capacitive circuit of monolayer GFET are shown in Fig. 9.[49] As shown in Fig. 9(a), the graphene film is located between the top and the back-gate dielectrics. The source and drain ohmic contacts as well as the top-gate stack are located on the top of the graphene channel. The back-gate stack is comprised of a dielectric and a substrate acting as the back-gate. In this structure, the access region resistances are modeled as a function of the applied back-gate bias. The model is based on the 2D DOS of monolayer graphene being proportional to the Fermi level energy E_{F}.

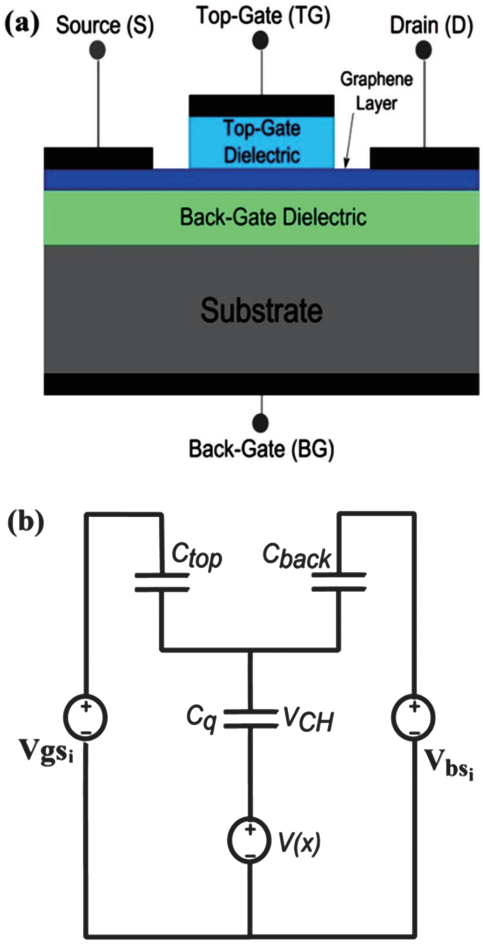


Fig. 9. (color online) (a) Cross section view and (b) equivalent capacitive circuit of monolayer GFET structure.[50]

For the monolayer GFETs, the drain current has also been derived from the general drift-diffusion equation and considered the velocity saturation of carriers[73] which reads

$$I_{\mathrm{ds}} = \mu W \frac{\int_0^{V_{\mathrm{ds_i}}} (|Q_{\mathrm{net}}| + q \cdot n_{\mathrm{puddle}})}{L + \mu \left| \int_0^{V_{\mathrm{ds_i}}} \frac{1}{v_{\mathrm{sat}}} \mathrm{d}V \right|} \tag{46}$$

where $Q_{\rm net}$ is the stored charge density in the channel and $n_{\rm puddle} = \Delta^2/\pi(\hbar v_{\rm F})^2$ accounts for the formation of hole and electron puddles in the graphene sheet[66] Δ represents the spatial inhomogeneity of the electrostatic potential and $v_{\rm F}$ is the Fermi velocity. To account for this asymmetric conduction behavior, a separation of electron and hole branch contributions is necessary for the total drain current implementation, the total drain current can be written as the sum of the hole and electron contributions ($I_{\rm ds} = I_{\rm ds_n} + I_{\rm ds_p}$) as

$$I_{\rm ds} = \mu_n W \frac{\int_0^{V_{\rm ds_i}} \left(|Q_n| + \frac{q \cdot n_{\rm puddle}}{2} \right)}{L + \mu_n \left| \int_0^{V_{\rm ds_i}} \frac{1}{v_{{\rm sat}_n}} {\rm d}V \right|} + \mu_p W \frac{\int_0^{V_{\rm ds_i}} \left(|Q_p| + \frac{q \cdot n_{\rm puddle}}{2} \right)}{L + \mu_p \left| \int_0^{V_{\rm ds_i}} \frac{1}{v_{{\rm sat}_p}} {\rm d}V \right|}, \quad (47)$$

where (Q_n, $v_{{\rm sat}_n}$, μ_n), and (Q_p, $v_{{\rm sat}_p}$, μ_p) are the charge sheet density, saturation velocity, and mobility for electrons and holes respectively. The net stored charge density in the channel can be written as

$$Q_{\rm net}(x) = Q_p - Q_n = -\frac{1^3}{\pi(\hbar v_{\rm F})^2} V_{\rm CH}(x) |V_{\rm CH}(x)|. \quad (48)$$

Under the applied bias voltages ($V_{\rm gs}$, $V_{\rm ds}$, $V_{\rm bs}$), one can write a second degree equation of the channel potential $V_{\rm CH}$ by solving the charge equations from the equivalent capacitive circuit shown in Fig. 9(b)

$$V_{\rm CH}(x) = {\rm sign}(Q_{\rm tot} - C_{\rm eq} V(x)) \times \frac{-C_{\rm eq} + \sqrt{C_{\rm eq}^2 + 4\alpha |Q_{\rm tot} - C_{\rm eq} V|}}{2\alpha}, \quad (49)$$

with $C_{\rm eq} = C_{\rm top} + C_{\rm back}$, $Q_{\rm tot} = C_{\rm top} V_{\rm gsi} + C_{\rm back} V_{\rm bsi} + qN_{\rm F}$, and $\alpha = q^2/\pi(\hbar v_{\rm F})^2$, where $C_{\rm top}$ and $C_{\rm back}$ are the top and back gate capacitances, respectively. $N_{\rm F}$ is the net doping in the graphene channel. $V_{\rm gsi}$ and $V_{\rm bsi}$ are the intrinsic voltages within the structure $V(x)$ is the voltage drop across the graphene channel. $V_{\rm CH}(x)$ along the channel depends on the bias conditions of the graphene layer. Then, based on Eq. (49), the net charge due to electron and hole conductions leads to the following equations

$$Q_{\rm net} \approx \begin{cases} -Q_n \to -Q_n \approx \alpha V_{\rm CH} |V_{\rm CH}| = \alpha V_{\rm CH}^2, \\ -Q_p \to -Q_p \approx \alpha V_{\rm CH} |V_{\rm CH}| = \alpha V_{\rm CH}^2. \end{cases} \quad (50)$$

Finally, the gate-source and gate-drain capacitances are calculated using the following equations:

$$\begin{cases} C_{\rm gs} = \left(\frac{{\rm d}Q_{\rm channel}}{{\rm d}V_{\rm gs}} \right)_{V_{\rm ds}={\rm cst}} + \left(\frac{{\rm d}Q_{\rm channel}}{{\rm d}V_{\rm ds}} \right)_{V_{\rm ds}={\rm cst}}, \\ C_{\rm gd} = \left(\frac{{\rm d}Q_{\rm channel}}{{\rm d}V_{\rm gd}} \right)_{V_{\rm gs}={\rm cst}} = -\left(\frac{{\rm d}Q_{\rm channel}}{{\rm d}V_{\rm ds}} \right)_{V_{\rm gs}={\rm cst}}, \end{cases} \quad (51)$$

with $Q_{\rm channel} = W \int_0^L (Q_{\rm net} + q \cdot n_{\rm puddle}) {\rm d}x$.

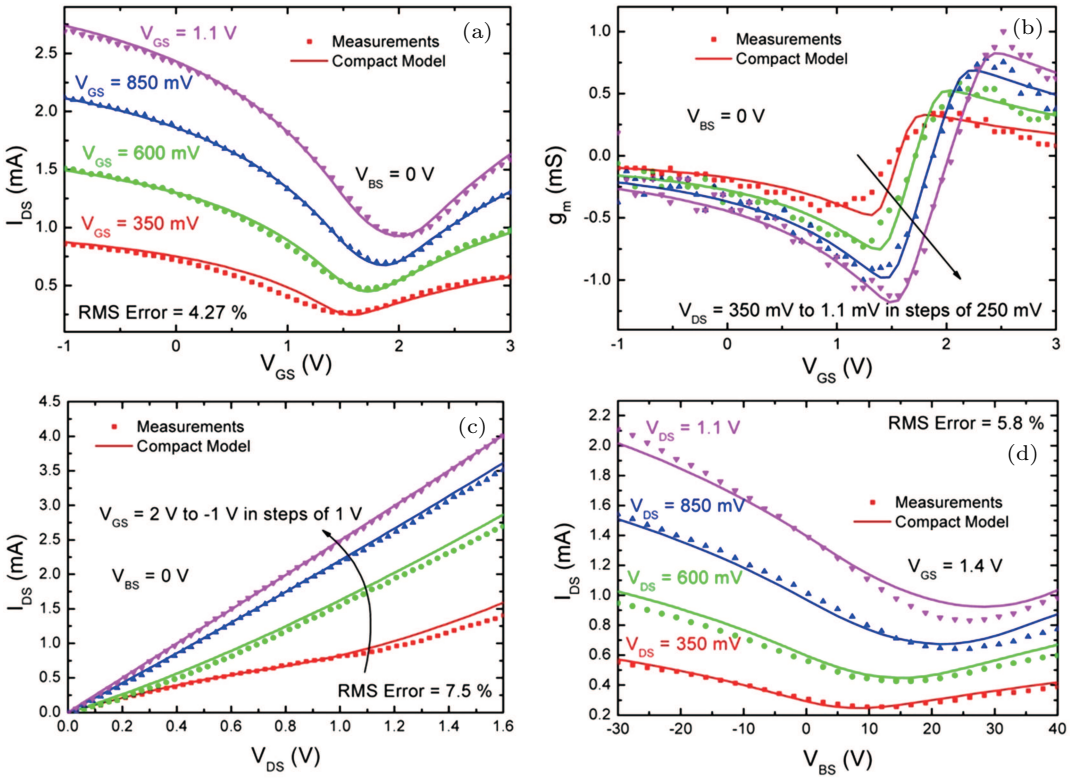


Fig. 10. (color online) Comparison of (a) $I_{\rm d}$–$V_{\rm gs}$, (b) $g_{\rm m}$–$V_{\rm gs}$, (c) $I_{\rm d}$–$V_{\rm ds}$, and (d) $I_{\rm d}$–$V_{\rm bs}$ measurements (symbols) with the compact model (solid lines).[50]

For verifying the model described above, measurement results from two different monolayer GFET technologies have been compared with the model simulations. Figure 10 shows the DC characteristics (I_d–V_{gs}, I_d–V_{bs}, I_d–V_{ds}) from a device having a gate length of 5 μm and width of 25 μm.[36] The simulation shows a good agreement with the measured results.

6.2. Bilayer graphene FETs

For the bilayer graphene FETs, the model considering DOS of bilayer graphene is used as Eq. (17). The corresponding device and equivalent capacitive circuit of bilayer GFET are shown in Fig. 11.[49] It is assumed that on top of the bilayer graphene channel, the source and drain ohmic contacts as well as the top-gate stack are located. The back-gate stack is composed of a dielectric and a substrate acting as the back-gate.

The drain current I_{ds} in the bilayer graphene FETs can also be expressed as the sum of the electron and hole contributions, $I_{ds} = I_{ds_n} + I_{ds_p}$, which is similar to that in the monolayer graphene FETs.

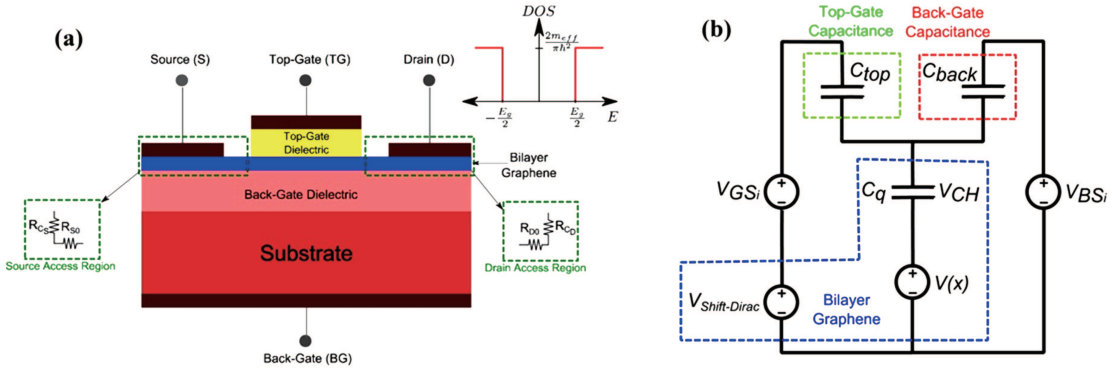


Fig. 11. (color online) (a) Cross-sectional view and the equivalent drain and source access resistances, and (b) equivalent capacitive circuit of bilayer GFET structure. Inset: DOS of bilayer graphene with a nonzero energy bandgap.[49]

The saturation velocity of carriers is given by

$$V_{\mathrm{sat}_{(n,p)}} = \frac{\hbar\Omega}{\sqrt{\pi\left(\dfrac{|Q_{(n,p)}|}{q} + \dfrac{n_{\mathrm{puddle}}}{2}\right)}}, \tag{52}$$

with $\hbar\Omega$ being the effective energy due to phonon scattering in the substrate. Here, an even distribution of the residual carrier density n_{puddle} in the electron and hole puddles is considered.

As the back-gate voltage V_{bs} becomes more negative, more positive charges are induced to close the back-gate, thereby inducing more negative charges close to the graphene channel on the top side of the back-gate dielectric. Thus, higher values of V_{gs} are required to obtain the channel charge inversion, resulting in a shift in the Dirac point $V_{\mathrm{Shift-Dirac}}$ toward the positive direction. Then, the shift in the Dirac voltage will also saturate eventually as described by the exponential model

$$V_{\mathrm{Shift-Dirac}} = V_1 + V_2 \cdot \exp\left(-\frac{|V_{\mathrm{bs}_i}|}{V_3}\right), \tag{53}$$

where V_1, V_2, and V_3 are constants.

Considering that the areas of hole and electron puddles are equal in size, the spatial electrostatic potential is simplified as a step function with a peak-to-peak value of $\pm\Delta$, as presented in Ref. [66], which includes the effect of the opening of an energy bandgap. The electron and hole puddles are written as

$$n_{\mathrm{puddle}} = \frac{2m_{\mathrm{eff}}}{\pi\hbar^2}k_{\mathrm{B}}T\left\{\ln\left[1+\exp\left(\frac{-E_{\mathrm{g}}/2+\Delta}{k_{\mathrm{B}}T}\right)\right] + \ln\left[1+\exp\left(\frac{-E_{\mathrm{g}}/2-\Delta}{k_{\mathrm{B}}T}\right)\right]\right\} \tag{54}$$

In order to validate the capability of the developed compact model for accurate modeling of the bilayer GFET devices, comparisons with measurements from the literature[74] have been performed and are presented. The comparison of the measurement data and the developed compact model is shown in Fig. 12, which shows the good agreement.

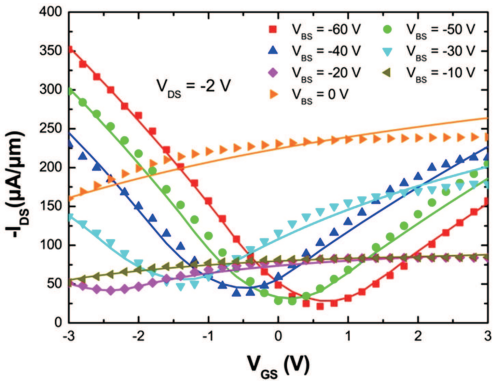


Fig. 12. (color online) Comparison of the I_{ds}–V_{gs} measurements[34] (symbols) with the compact model (solid lines) for $V_{ds} = -2$ V and $V_{bs} = 0$ V to -60 V.[49]

7. Surface-potential-based compact model

As described above, plenty of compact models for GFETs have been developed with the current characteristics and can be implemented in Verilog-A for simulations of DC, AC, or

transient properties. However, to achieve an accurate model qualified in EDA tool, the compact model with high accuracy and strong physical property should be further considered. For the real graphene device, the random distribution of carriers (electron or hole) caused by the impurities and spatial disorder will play a role in carrier transport. Thus, to obtain an accurate transport property, compact model in GFETs should include the real physical effect, such as disorder and temperature. The surface-potential-based compact model is believed to have high accuracy and strong physical property, and be easily simplified into the charge-based and threshold-voltage-based models.

Based on the surface-potential-based, Li *et al.* have developed a continuous physical compact model for GFET. Figure 13(a) shows the schematic diagram of a top-gated GFET for GEFT compact model.[47,48] In Li *et al.*'s work, it is assumed that on top of the graphene channel, the source and drain ohmic contacts as well as the top-gate stack are located. And DOS for graphene is Gaussian DOS with disorder parameter, and the analytical carrier density is based on the exponential distribution of potential fluctuations for the electron branch ($E_F > 0$) or the hole branch ($E_F < 0$).

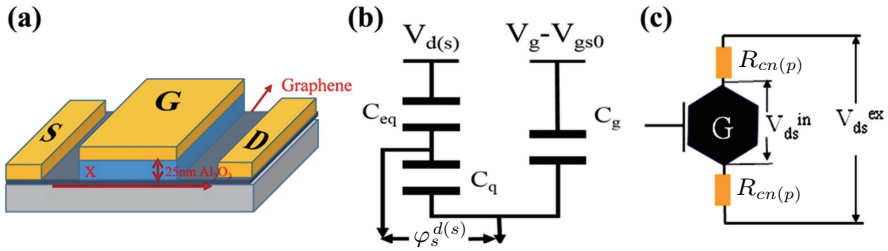


Fig. 13. (color online) (a) Geometric definition for compact model of GFET, (b) capacitance divider scheme extracted from a single gated GFET, and (c) extrinsic structure for GFET.[48]

7.1. Surface-potential- based model

Generally, the threshold voltage emphasizes the converting point, while the surface potential φ_s always generates a continuous transition behavior covering the whole region. For the zero band-gap graphene, carriers generally degenerate with Fermi level located in the conduction or valence energy band. In this situation, the surface potential is obtained by using capacitance divider scheme instead of Poisson equation as shown in Fig. 13(b). For a single gate GFET, φ_s is expressed as

$$\varphi_s = \mathrm{sgn}(V_x)\frac{-C_g+\sqrt{C_g^2+4kC_gV_{gx}}}{2k}, \tag{55}$$

where sgn is the sign function, $V_{gx} = \sqrt{\left(V_{gs}-V_{gs}^0-V(x)\right)^2}$, $V(x)$ is the voltage along the channel, $V(0)$ or $V(L)$ represents the source or drain voltage, V_{gs}^0 is the gate doping voltage which will cause the drift of Dirac point. Equation (55) is applicable for high gate voltage region arising from the simple quantum capacitance. However, at the low gate voltage, the disorder effect dominates the transport and hence demands the accurate C_q. With the Gaussian distribution of potential fluctuations,[75] although C_q can achieve the high accuracy, it also blocks the analytical solution of φ_s. Fortunately, this question has been addressed by Li *et al.* by using the exponential distribution instead of Gaussian form.[76]

Based on Ref. [76], the surface potential φ_s can be obtained by solving the following equation:

$$V_{gx} = q\left(n_e(\varphi_s)-n_h(\varphi_s)\right)\left(\frac{1}{C_g}+\frac{1}{C_{eq}}\right)+\varphi_s, \tag{56}$$

where C_{eq} is the effective capacitance of the metal and graphene contact, $C_{eq} = \varepsilon_0/d_{eq}$, and d_{eq} is the effective contact distance. By using the 3rd Taylor series, the final surface potential φ_s can be written as

$$\begin{cases} f_4 = \sqrt{\left(27f_1^2+9f_1f_2f_3-2f_2^3\right)^2+4\left(3f_1f_3-f_2^2\right)^3} \\ \qquad +27f_1^2+9f_1f_2f_3-2f_2^3, \\ \varphi_s = \dfrac{\sqrt[3]{f_4}}{3\sqrt[3]{2}f_1}-\dfrac{\sqrt[3]{2}\left(3f_1f_3-f_2^2\right)}{3f_1\sqrt[3]{f_4}}-\dfrac{f_2^2}{3f_1}. \end{cases} \tag{57}$$

7.2. Asymmetry behaviors

It is well known that ambipolar characteristic curves in GFET show an asymmetry for electron and hole, which mainly derives from contact metal doping. Thus, the corresponding model should be modified. Based on the contact resistances as shown in Fig. 13(c), Li *et al.* developed the intrinsic voltage as[47,48]

$$V_{ds}^{in} = V_{ds}^{ex}-2I_{ds}R_c, \tag{58}$$

where V_{ds}^{in} and V_{ds}^{ex} are the intrinsic and extrinsic drain-source voltages, respectively, and I_{ds} is the drain-source current related to V_{ds}^{in}. Equation (58) can only be solved numerically with contact resistance for hole (electron). Considering the

contribution of the contact doping to the surface potential, the asymmetry surface potential can be obtained by altering the effective contact capacitance C_{eq} in different operation regions. Then, the asymmetry surface potential is written as

$$\varphi_{sa} = \frac{1}{r_0}\log\left[\exp\left(r_0\mathrm{sgn}\left(V_{gx}\right)\varphi_{sh}\right) + \exp(r_0\mathrm{sgn}(V_{gx})\varphi_{se})\right], \tag{59}$$

where r_0 is a fitting parameter and its sign controls the type of metal doping, the detailed parameter is shown in Table 1.

Table 1. Different metal-graphene contact and channel related to fitting parameter r_0.

Metal	Contact form	Parameter
Ag (Ti, Au, Pd)	p–p–p	$r_0 < 0, V_{gs} < V_{dirac}$
	p–n–p	$r_0 < 0, V_{gs} > V_{dirac}$
Al	n–p–n	$r_0 > 0, V_{gs} > V_{dirac}$
	n–n–n	$r_0 > 0, V_{gs} > V_{dirac}$

Based on Eq. (59), one can calculate the surface potential with numerical and analytical solutions, as shown in Fig. 14. The corresponding small error is shown in the inset.

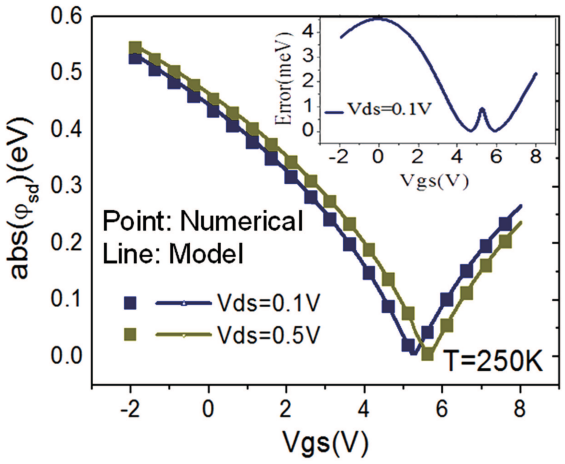


Fig. 14. (color online) Simulation results of surface potential with numerical and analytical solutions, respectively. Inset: the error between numerical and analytical solutions.[47,48]

7.3. Current modeling

Generally, the constant mobility instead of function of Fermi level in model was applied. To achieve a higher level, the functional current will be simplified and then accuracy is reduced. To obtain carrier transport property, Li *et al.* introduced thermal activated transport theory and Bolzmann transport theory into the surface-potential-based model.[48] Electron or hole will contribute to the thermal activated transport[77] in the low Fermi level region, while in the high Fermi level, the Boltzmann transport will be dominant and include two scattering mechanisms (long-range and short-range). Based on these theories, the current should include three components as

$$\begin{cases} I_{long} = \dfrac{W}{L}\dfrac{qk\hbar\pi}{I_0 n_i (2\pi q^2/k)^2}\left[\mathrm{sgn}(\varphi_s)\displaystyle\int(n_e(\varphi_s) + n_h(\varphi_s))\varphi_s\frac{dV(x)}{d\varphi_s}d\varphi_s\right]\frac{|\varphi_{sd}|}{|\varphi_{ss}|}, \\ I_d = \dfrac{W}{L}\left[\mathrm{sgn}(\varphi_s)\displaystyle\int\sigma_d\frac{dV(x)}{d\varphi_s}d\varphi_s\right]\frac{|\varphi_{sd}|}{|\varphi_{ss}|}, \\ I_{short} = \dfrac{W}{L}\dfrac{4kD_1\hbar(\hbar V_f)^2}{q^3 n_d V_0^2}\left[\mathrm{sgn}(\varphi_s)\left(\displaystyle\int\left(1-\exp\left(-\frac{\varphi_s}{\beta}\right)\right)\frac{dV(x)}{d\varphi_s}d\varphi_s\right)\right]\frac{|\varphi_{sd}|}{|\varphi_{ss}|}, \end{cases} \tag{60}$$

where the subscripts d, long, and short represent the thermal activated, long-range scattering, and short-range scattering mechanisms, respectively, φ_{sd} (φ_{ss}) represents the drain (source) surface potential obtained by Eq. (57). Due to the competence of the two scattering mechanisms and the geometric mean presenting the transition from the thermal activation to Boltzmann transport, the final current model is expressed as

$$I_{total} = \left[\left(I_{long}^{-r_1} + I_{short}^{-r_1}\right)^{-r_2/r_1} + I_d^{r_2}\right]^{1/r_2}, \tag{61}$$

where r_1 and r_2 are the fitting parameters.

In Figs. 15(a) and 15(b), the comparison of the calculated and experimental results for output and transfer current characteristics is presented.

For current models, the output current saturation is always considered, which arises from drift velocity saturation or Joule heating effects. Generally, model with drift velocity saturation is written as the effective length expression

$$L_{eff} = L + \int_{\varphi_{ss}}^{\varphi_{sd}}\frac{\mu}{v_{sat}(\varphi_s)}\frac{dV(x)}{d\varphi_s}d\varphi_s, \tag{62}$$

where v_{sat} is the saturation velocity. As well as typical models for v_{sat} and μ, various effective channel length expressions can be obtained. Actually equation (62) can be fully simplified with constant mobility and non-disorder carrier density ($n \propto \varphi_s^2$). Then, equation (62) will be transformed as

$$L_{eff} - L \propto \left(\varphi_s^2 + C\varphi_s^3\right)\left|\frac{\varphi_{sd}}{\varphi_{ss}}\right|. \tag{63}$$

According to Eq. (63), a model including residue carrier density (n_0) or disorder parameter (s) has been evolved. Remarkably, the effective length with the scattering mechanisms dependent mobility can be improved. L_{eff} embedded with two scattering mechanisms can be simply presented as

$$I_{eff} - L \propto \left(L_{long}^{-r_1} + L_{short}^{-r_1}\right)^{-1/r_1}. \tag{64}$$

Based on Eq. (64), the comparison of saturation output current for the calculated and experimental results under different channel lengths is presented in Figs. 15(c) and 15(d).

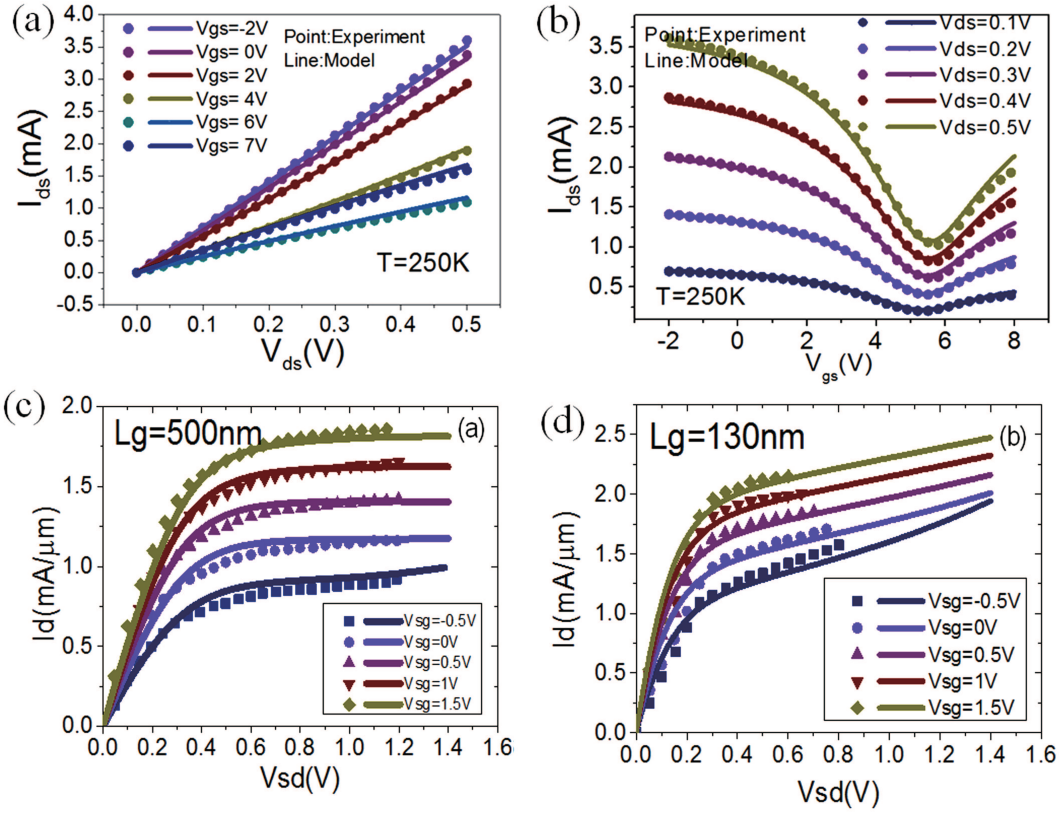


Fig. 15. (color online) (a) The output current under different gate voltages for the calculated and experimental results, and (b) transfer current under different drain voltages for the calculated and experimental results. Output current with simulated and experimental resutls under (c) $L_g = 500$ nm and (d) $L_g = 130$ nm.[47,48]

7.4. Capacitance model

The terminal charges Q_g, Q_d, and Q_s always relate with the gate, drain, and source electrodes. Q_g is the integration of the net mobile carrier concentration along the channel. Q_d and Q_s can be obtained by Ward–Dutton's linear charge partition scheme,[41,47] with the charge conservation relationship. The expressions for terminal charges are written as

$$\begin{cases} Q_g = -w\int_0^L Q_{net}\,dy, \\ Q_d = w\int_0^L Q_{net}\,dy, \\ Q_s = -\left(Q_g + Q_d\right). \end{cases} \tag{65}$$

Due to the current continuity equation, dy in Eq. (65) can be replaced by $-\mu W\,|Q_{net}|\,dV/I_d$ and y is equal to $L_{eff}I_d(\varphi_s)/I_d$. Generally, if one considers the simple current model with constant mobility, disorder induced carrier density can be introduced into Eq. (63). Then, the capacitance model can be deduced analytically by using the formula

$$C_{ij} = \begin{cases} -\dfrac{\partial Q_i}{\partial V_j}, & i \neq j, \\ \dfrac{\partial Q_i}{\partial V_j}, & i = j, \end{cases} \tag{66}$$

where i and j represent the terminals. As the gate oxide thickness is greatly decreased, the quantum capacitance needs to account for accurate intrinsic capacitance modeling during circuit simulation. Quantum capacitance induced by disorder is significant in discussing scaling down effect. The comparison of capacitance for the calculated and experimental results is shown in Fig. 16.

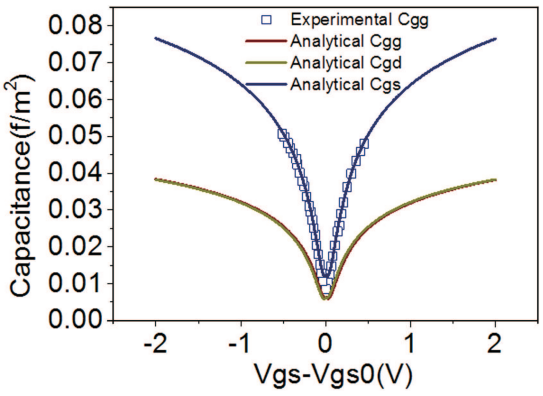


Fig. 16. (color online) Comparison of C_{gg}, C_{gs}, and C_{gd}. The lines represent the calculated results, and the points represent the experimental results.[47,48]

7.5. Parameter extraction

The computable effective and physics-based extraction method will benefit the compact model's accuracy. Generally, extraction aims at being physical and fitting parameters. To obtain higher level, the parameter sequence should introduce physical effect. However, considering the continuity and accuracy of compact model, the fitting parameters will be used for

smoothing the output curves and reducing the error. It is anticipated that the compact model of GFETs with the parameter sets will be suitable to circuit design and can provide accurate insight into the performance. The main criterion for a good set of parameters is the balance of error, efficiency, and continuity. Figure 17 shows the extraction flow of the key physical parameters of the surface-potential-based compact model.[47,48]

Based on the corresponding equations shown in Fig. 17, four key parameters which determine the transport mechanisms can be obtained. Generally speaking, the self-consistent physics-based model is easier to extract the physical parameters. But, it is incompatible to propose a unified method of parameter extraction due to quite complicated models.

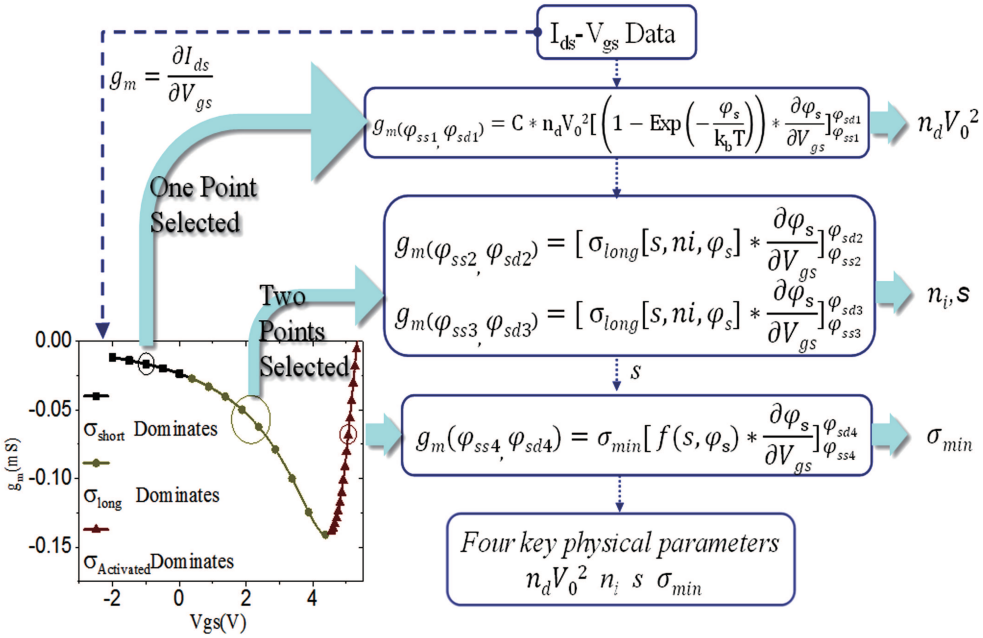


Fig. 17. (color online) Extraction flow of the key physical parameters of the model.[47]

7.6. Gummel symmetry test

For convergence in simulation and analysis for GFET based circuit, continuity and symmetry characteristics have to be kept. On the other hand, to simulate RF circuit, the corresponding parameters should satisfy the continuous and symmetry conditions. Compact model must fulfill one of the benchmark tests, that is, Gummel symmetry test (GST).[78,79] The traditional GST circuit is shown in Fig. 18. Generally, the higher-order derivatives in MOSFET compact models are obtained as a function of V_x, which is symmetry for $V_x = 0$. This symmetry roots in the symmetry device structure and channel.

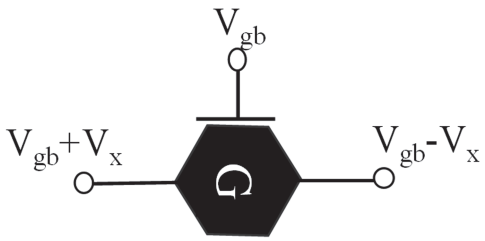


Fig. 18. Traditional GST circuit.

For GFETs, the symmetry is different from the transitional devices due to the drift of Dirac point. Depletion layer in the channel has disappeared in GFETs. In the capacitance divider scheme, this doping effect causes the asymmetry for plus and minus branches of drain voltage. Thus, to achieve GST, an applied gate-voltage will supplement the drift voltage. Otherwise, to control the continuity, the boundary conditions of the transition of different transport mechanisms cannot be ignored. To achieve it, the current components cover the whole region to avoid the sharp change at some typical points. For $V_x = 0$, the hole and electron branches will meet, where smoothing parameter in sgn function will be used for better continuity. If the model passes the GST, as shown in Fig. 19, one can claim that the model has a good continuity and symmetry.

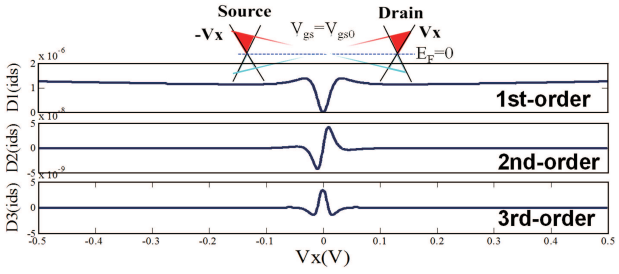


Fig. 19. (color online) GST for 1, 2, 3-order derivatives of I_{ds} under the condition $V_{gs} = V_{gs0}$.[47,48]

7.7. Simulation of GFET-based circuits

To embed the compact model into a vendor simulator, the Verilog-A hardware description language (HDL) language

is always used for constructing a circuit level model. VA HDL is used for designing analog and mixed-signal systems and integrated circuits defined modules which encapsulate high-level behavioral descriptions as well structural descriptions. Here the surface-potential-based compact model is coded by using Verilog-A language.[80] The parameter declaration, surface-potential calculation, output current, and capacitance are shown in Fig. 20.

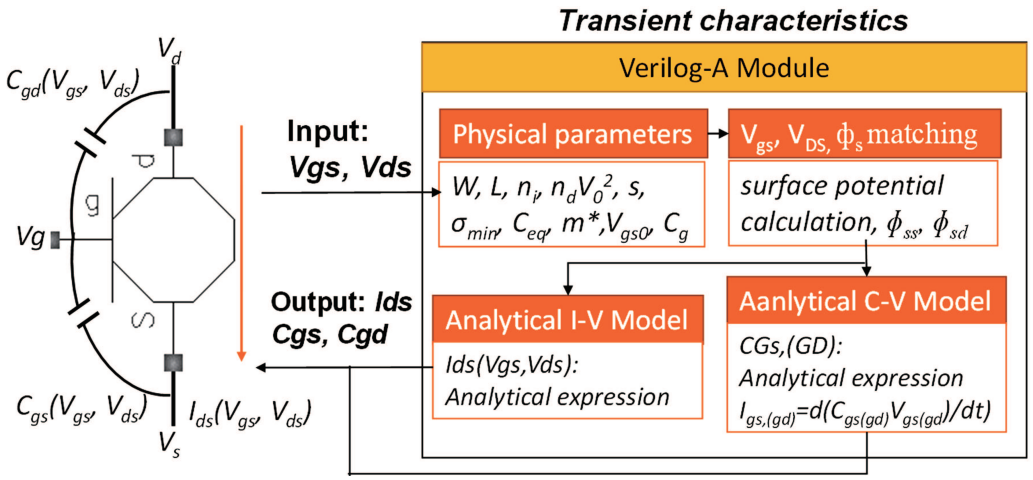


Fig. 20. (color online) Verilog-A module for compact model of GFET.

8. Conclusions and outlook

We have reviewed the concept, origin, development, and application of compact model within the scope of graphene field-effect transistors (GFETs). Although the compact model has a short history since it appeared, it seems that research interest in the compact model has been growing greatly. Based on the several current contributions, we have tried to describe plenty of methods on developing the GFET compact model. The merits and demerits for current compact model have also been discussed. To keep pace with the increase of circuit operating frequencies and device tolerances scale down with concomitant increases in chip device count, accurate and physics-based compact models are essential for the design and development of GFETs. Currently, the compact model is still open and evolvable. We hope that this review will be helpful to comprehensive understanding of GFETs compact model, and provide a motivation for promoting the application of GFETs in industry.

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