TOPICAL REVIEW — 2D materials: physics and device applications

Atomic crystals resistive switching memory*

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Facing the growing data storage and computing demands, a high accessing speed memory with low power and non-volatile character is urgently needed. Resistive access random memory with $4F^2$ cell size, switching in sub-nanosecond, cycling endurances of over 10^{12} cycles, and information retention exceeding 10 years, is considered as promising next-generation non-volatile memory. However, the energy per bit is still too high to compete against static random access memory and dynamic random access memory. The sneak leakage path and metal film sheet resistance issues hinder the further scaling down. The variation of resistance between different devices and even various cycles in the same device, hold resistive access random memory back from commercialization. The emerging of atomic crystals, possessing fine interface without dangling bonds in low dimension, can provide atomic level solutions for the obsessional issues. Moreover, the unique properties of atomic crystals also enable new type resistive switching memories, which provide a brand-new direction for the resistive access random memory.

Keywords: atomic crystals, two-dimensional materials, resistive switching memory

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1. Introduction

With the explosive growth of portable and wearable devices, a high density, low power dissipation and fast speed memory with non-volatile feature is needed to meet the demand for accessing enormous information. Solid-state non-volatile memory known as Flash memory has been introduced as a trade-off point of DRAM (dynamic random access memory) and HDD (hard disk drive), which has both non-volatile character and moderate accessing speed.[1] However, the limitations, such as, low endurance, high operation voltage supply, slow write speed and cumbersome erase procedure, have hindered the further development of Flash.[1,2] In the past few decades, research on a new architecture non-volatile memory, resistive random access memory (RRAM), has been accelerating. RRAM is a two terminals device, the memristor concept was firstly brought forward by Leon Chua in 1971,[3] whose electrical state depends on the history of applied voltage and current.[2,4] Utilizing a crossbar MIM (metal/insulator/metal, generally, the "metal" should indicate conductor) architecture, the RRAM can be a promising candidate for non-volatile memory with high density (crossbar area can be scaled down to 10×10 nm^2),[5] switching in sub-nanosecond,[6] extreme cycling endurances of over 10^{12} cycles,[7] and sufficient retention exceeding 10 years at 85 °C.[7,8] Because RRAM is not based on silicon, this will promote more extensive applications, such as flexible and transparent applications.[9,10] Except for storing information, RRAM behaves in some unique applications. Resistive switch cells can be used as synapses in neuromorphic circuits, which can satisfy both high connectivity and high density demands for efficient computing.[11–16] Resistive switches can even both store logic values and perform logic operations.[17] Although RRAM shows huge potential in the non-volatile memory application, there still remain some challenges, such as sneak leakage path,[2,11,18,19] the metal films sheet resistance problem in three-dimensional (3D) RRAM,[20–22] power dissipation[2] and reliability.[1] Atomic crystals may provide a series of solutions to these problems, as we will discuss in the next part.

Atomic crystals are low dimensional crystal materials, such as one dimensional (1D) materials, and two-dimensional (2D) materials. As a major part of atomic crystals, 2D materials are layered materials with strong in-plane chemical bonding and weak van der Waals force between adjacent layers, whose surface is free of dangling bonds.[23] As graphene was firstly exfoliated from bulk graphite by Geim and Novoselov,[24] graphene attracts lots of attention because of its rich physical properties. Graphene is a Dirac semimetal which has a linear energy dispersion in k-space near Dirac points (Fig. 1(a)).[25,26] Graphene is the strongest material ever measured[27] and can carry ultrahigh density current about 10^8 A/cm^2, which is 100 times higher than metal films, even in single layer (Fig. 1(b)).[28,29] Moreover, the electrical properties of graphene are easily tuned by a physical or chemical method.[30–35] Transition metal dichalcogenides (TMDCs) is another big family of 2D materials whose single layer is composed by three layered atoms and its effective Young's mod-

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ulus is comparable to that of steel (Figs. 1(c) and 1(d)).[36,37] Compared with graphene, TMDC families have much more abundant band structures. Some of them even have a transition from indirect band gap to direct band gap when the layer number decreases to monolayer.[38–40] Owing to the large band gap (1–2 eV), TMDCs are promising candidate materials for logic circuit applications.[36,41,42] Such as MoS_2, the monolayer ($\sim$0.65 nm, Fig. 1(d)) shows great electrical performance:[36] for $V_{ds} = 500$ mV, the I_{on}/I_{off} ratio is higher than 10^8. Graphene with outstanding carrier and heat conduction,[28,29,43,44] good flexibility and transparent,[25,27] can offer atomic level solutions for the integration,[45–47] power dissipation[48,49] and reliability[50] problems in RRAM. TMDCs with excellent electrical performance and easily tuned characters can inspire a stirring new type of RRAM.[51]

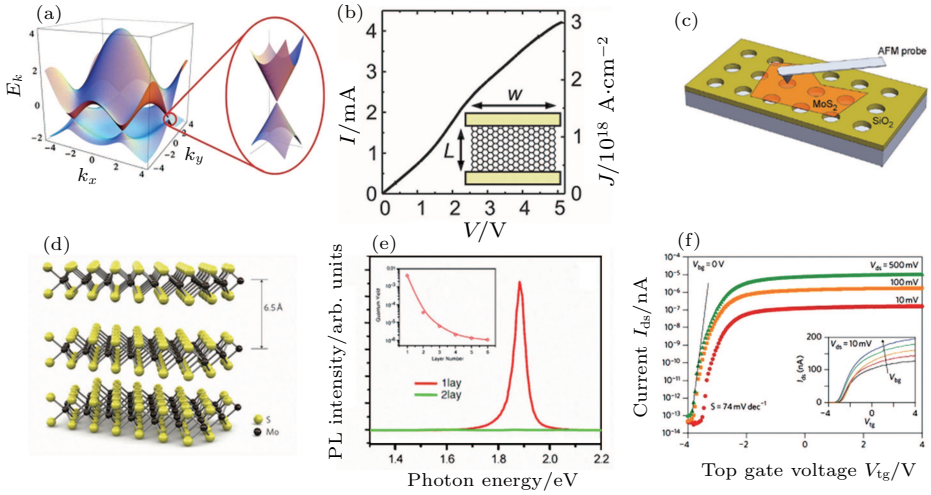


Fig. 1. (color online) Two-dimensional materials. (a) The band structure of graphene. Right: zoom in one of the band spectrum near the Dirac points.[52] (b) Output characteristics of graphene field effect transistor, which prove that graphene can carry ultrahigh density current (over 1 μA/nm^2).[28] (c) Schematic of the MoS_2 breaking strength measurement. The effective Young's modulus is comparable to that of steel.[37] (d) Schematic of two-dimensional materials MoS_2, which belongs to the transition metal dichalcogenide family. A single layer is around 0.65 nm.[36] (e) The photoluminescence spectra of monolayer and bilayer MoS_2 sample, which represents the MoS_2 band structure transition from indirect (corresponding to bilayer) to direct (corresponding to monolayer).[38] (f) Transfer characteristics of single layer MoS_2 field effect transistor,[36] which shows excellent electrical performance: for $V_{ds} = 500$ mV, the I_{on}/I_{off} ratio is greater than 10^8.

This review focuses on the issues that hinder the RRAM further developments and the atomic level solutions that atomic crystal provided. In Section 2, the detailed issues about the RRAM in integration, power dissipation and reliability will be discussed. In Sections 3 and 4, this review will focus on the solutions for integration, power and reliability problems provided by atomic crystals. In Section 5, some inspired new type RRAM will be discussed in detail. Finally, Section 6 will summarize the works and discuss the blueprint for future development.

2. The issues hindering the development of RRAM

Generally, RRAM use an MIM crossbar architecture where the "M" represents metal or any good conductor and "I" denotes an insulator. The mechanisms are quite different and could be dominated by thermal, chemical, or electronic/electrostatic effects, which depend on the material systems of "M" and "I".[53] However, the switching characteristics can be roughly classified into two basic operation modes: unipolar and bipolar (Fig. 2(a)).[54] For unipolar switching characteristics, the set voltage is higher than the reset voltage, and the reset current is higher than the compliance current (CC) during set operation. While the bipolar switching characteristics, set and reset voltages have the opposite polarity. There are also so-called nonpolar devices, which is the coexistence of unipolar and bipolar characteristics.[54–56]

Although taking advantage of the crossbar architecture can hugely elevate the integration density,[5,19,57] the sneak leakage path issue[2,11,18,19] (Fig. 2(b)) that comes along is obsessional. When we try to read the state of an addressed element, there will be a leakage current flowing along the adjacent low resistance state elements. Such a leakage current could lead to an inadequate read voltage at the addressed element which may cause read error (left side of Fig. 2(c)). While the write operation has a similar situation, the extra voltage drops along half-selected elements, which are also caused by leakage current flowing along adjacent low resistance state elements, would lead to insufficient write voltage at the selected element (right side of Fig. 2(c)). In order to solve the read/write errors resulted by the sneak leakage path, one selected transistor is added to the memory cell, which is so called the 1T1R memory cell (left side of Fig. 2(d)). With the help of selected transistors, the read/write operation can only be accessing the selected single row at one time. Another feasible solution is to adopt a complementary structure (right side of Fig. 2(d)), in which the overall small voltage resistance is always high.[18]

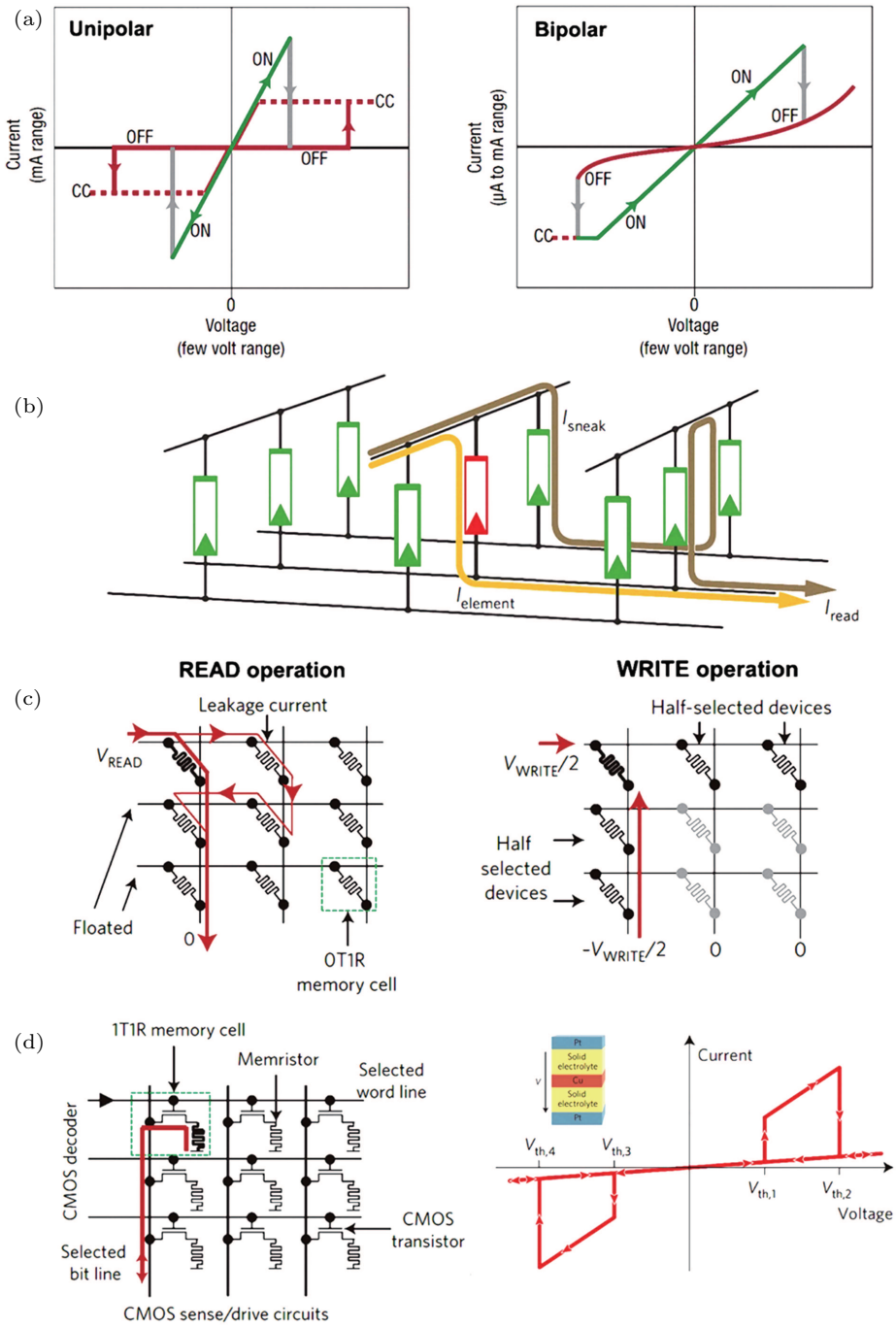


Fig. 2. (color online) (a) Classification of the switching characteristics based on the set/reset voltage polar.[54] Left: unipolar switching. The set voltage is higher than the reset voltage, and the reset current is higher than the compliance current (CC) during set operation. Right: bipolar switching. The set voltage and reset voltage have the opposite polarity. (b) Crossbar array and the sneak leakage path issue.[18] When we try to read/write the selected element, the sneak leakage current will affect the operations. (c) Schematic shows the effect of sneak leakage path to read/write operations.[2] Left: read operation. When trying to read the state of the addressed element, the leakage current from adjacent elements in the low resistance state will degrade the output signal. Right: write operation. During the write operation, the extra voltage drop along half-selected elements will lead to an insufficient voltage at the selected element. (d) The solutions for sneak leakage path problem.[2,18] Left: 1-transistor/1-resistor (1T1R) cell architecture which only enables read/write to a particular row. Right: using complementary structure to produce a complementary switching characteristics.

However, both of the two ways will increase the processing steps and limit the integration density. If the switching characteristic has an intrinsic rectifying character, it will be more favorable to increased density and realize low power dissipation. From another practical angle, researchers are also focusing on 3D integration to achieve a higher density.[20–22] In this situation, the metal films have encountered its physical bottleneck: the sheet resistance will exponentially grow when the film thickness is below 5 nm, which will significantly degrade the memory performance.[20–22] With continuous scaling down, the interface will be more important and harder to control quality, which will cause power and reliability problems. Furthermore, because of the hardly controlled conductive filament, there is large resistance variation between different devices and even the same device with different cycles, which leads to a reliability problem.[1] Using atomic crystals

is an attractive option to solve these problems, since they possess many excellent properties even in atomic thickness.

3. Seeking higher integration density

Atomic crystal like graphene, has an atomic level flat surface and holds good conductance even in a single layer, which make it a promising electrode material for solving the interface and metal films sheet resistance problems. Moreover, the easily tuned character makes it possible for emerging new features. The character that oxygen can be largely trapped and quickly moved in graphene is also favorable for oxygen vacancy based RRAM.[58,59] In addition, 1D atomic crystals material carbon nanotube (CNT) owns nanometer level diameter, which can be expected to scale the crossbar area to a nanometer × nanometer level.

3.1. Sneak leakage path: atomic thickness selected diode

As we have discussed, using a selected diode can technically solve the sneak leakage path problem. Here is an example that using poly-Si diode makes the set/reset operation of crossbar $4F^2$ cell possible.[19] However, the stacked poly-Si diode (around 200 nm) makes the further scaling down hard to advance. If a diode whose thickness is in nanometers and with the stable rectifying character it will be much more favorable for achieving high integration density RRAM. Fortunately, the excellent 2D properties of 2D materials graphene make such an amazing conception possible.

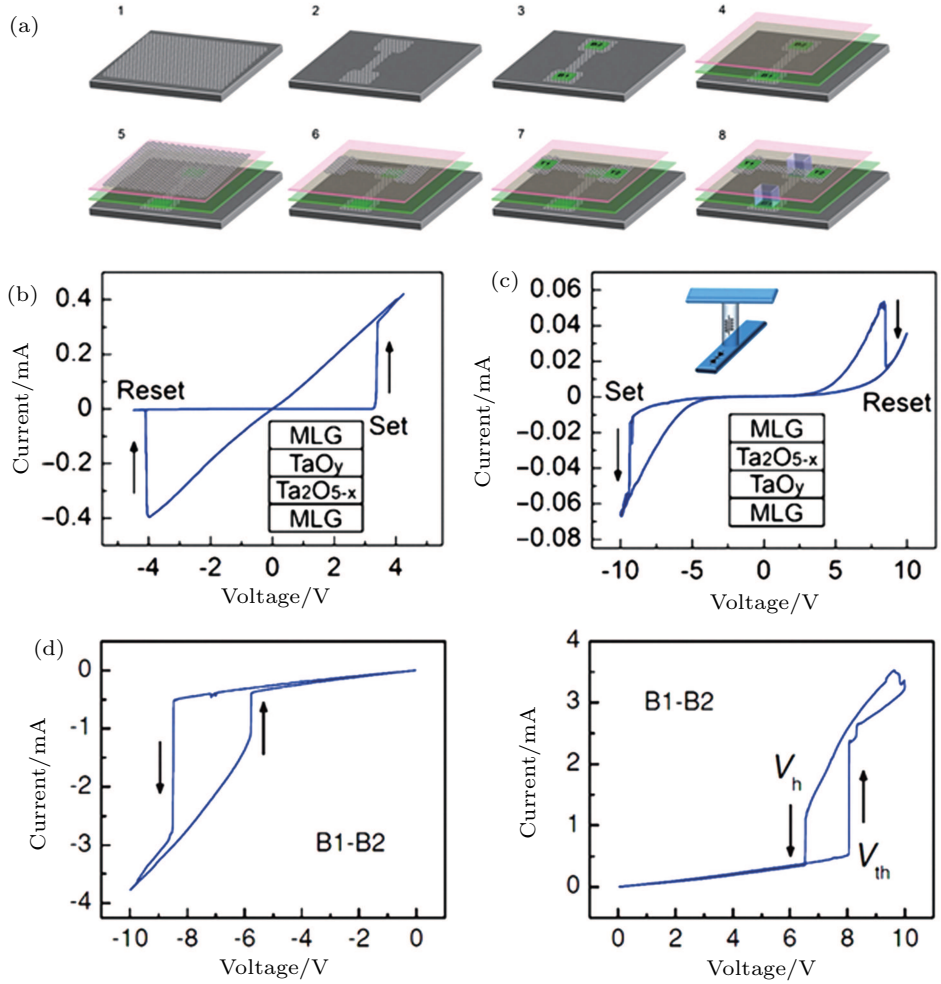


Fig. 3. (color online) Graphene as built-in selector element to solve sneak leakage path problem.[19,47] (a) The fabrication process of graphene resistive switching: the green film is TaO_y, the red film is Ta_2O_{5-x}. (b) The switching characteristics of MLG/TaO_y/Ta_2O_{5-x}/MLG, which shows linearity. (c) The switching characteristics of MLG/Ta_2O_{5-x}/TaO_y/MLG, which shows significant nonlinearity. (d) The switching characteristics of bottom electrodes: B1 and B2.

Yang *et al.* achieved such conception by utilizing multilayer graphene (MLG) as an electrode with structure: MLG/Ta_2O_{5-x}/TaO_y/MLG (Ta_2O_{5-x}: oxygen rich layer; TaO_y: oxygen deficient layer).[47] The device was fabricated on a glass substrate and the process was schematically represented by Fig. 3(a). The monolayer graphene was repeatedly transferred to form a stack of graphene on the substrate, which functioned as the bottom electrode. Then the MLG was defined into bottom electrodes and Au/Ti were deposited as metal contacts: B1, B2. Subsequently, switching mediums Ta_2O_{5-x} (oxygen rich layer) and TaO_y (oxygen deficient layer) were deposited by radio-frequency (RF) sputtering and reac-

tive sputtering (400 °C, O_2/Ar = 3%), respectively. The MLG top electrodes (T1, T2) were defined through the same process as bottom electrodes. As the Ta_2O_{5-x}/TaO_y device is based on oxygen vacancy distribution, the switching medium stacking sequence would only affect the set/rest polarity of the device, which already has been proved by researches on such devices with inert metal electrodes. However, the different stacking sequences in MLG devices show totally different switching characteristics (see Figs. 3(b) and 3(c)). Device with TaO_y/Ta_2O_{5-x} as the switching medium shows only normal linear switching characteristics, while the inversely sequence stack Ta_2O_{5-x}/TaO_y represents a high nonlinearity switching characteristic that is a favorable feature to suppress the sneak leakage path problem in crossbar architecture RRAM.

Since the nonlinearity does not come from the switching medium, MLG electrodes are the only possible factors to make such a nonlinearity. Seen from the fabrication process angle, the reversal of the switching medium has an effect on the bottom MLG electrode. The stacking sequence decides if the environment of the bottom MLG will be exposed: inert Ar environment if Ta_2O_{5-x} film is deposited first and oxygen plasma environment if TaO_y film is deposited first. Yang *et al.* thought the bottom MLG could be partly oxidized when it was exposed in the oxygen plasma environment and heated in 400 °C. In order to check the hypothesis, they measured the switching characteristics of bottom MLG electrodes: B1 and B2. Being different from the graphene field effect transistor, the bottom MLG device shows significant volatile threshold switching behavior without voltage polarity (Fig. 3(d)). When the applied voltage exceeds a particular value, the state of the device will change from high resistance state (HRS) to low resistance state (LRS) and a similar phenomenon can be observed on the opposite polarity. Once the voltage is removed, the device will return to HRS. Such an analogue of threshold switches can be utilized as an intrinsic series selector element in crossbar architecture RRAM. The non-linearity ratio $I(V_{\rm read})/I(V_{\rm read}/2)$ is about 280, which means the sneak leakage current can be debased around 2 orders.

In summary, Yang *et al.* demonstrated that MLG as electrode materials can integrate atomic thickness intrinsic selector in crossbar architecture RRAM which could benefit the scaling down (such as: stackable 3D RRAM) and flexible electronic application.

3.2. 3D integration: atomic thickness film with low sheet resistance

Pursuing higher integration density, the 3D stackable RRAM is needed, which hopefully goes beyond its competitor: 3D NAND Flash. Compared with conventional RRAM 2D crossbar architecture stacked layer by layer, 3D vertical RRAM crossbar architecture shows an excellent switching characteristics and demonstrates a cost-effective fabrication process. When more layers are needed to stack, the 3D crossbar architecture encounters its physical bottleneck: the limit of metal film sheet resistance.[20–22] The vertical 3D RRAM integration density can greatly increase for both the metal film sheet resistance improvement (using good conductor Cu film to replace TiN film as metal film material) and thickness scaling down.[20] Further sheet resistance and metal film thickness improvement is necessary, while the growing current density aggravates the Cu electromigration phenomenon which could significantly degrade the device performance: decay of write and read window, increased wire latency, and substantial interconnect energy.[22] When the metal film thickness scales below 5 nm, the resistance will increase exponentially.[22]

As atomic crystal, graphene intrinsically owning an ultrathin thickness represents the plane thickness minimum scaling down limit. With a strong in-plane chemical bond between carbon atoms, graphene without the electromigration problem like bulk metal film is used. The ability of carrying ultrahigh density current[28,29] (about 10^8 A/cm^2, 100 times of metal film) even in one atom thick makes graphene promising electrode materials in 3D RRAM. Moreover, the graphene, sheet resistance as low as 125 Ω/sq, can be roll to roll produced (Fig. 4).[60]

Compared with Pt film based 3D RRAM, the research of Lee *et al.* indicated 3D RRAM based on atomically thin graphene has lower accessing voltage, lower current, and higher storage potential.[46] Figure 5(a) shows the schematic of two-layers graphene based RRAM, the thickness of graphene electrode is only 0.3 nm. Because of the unique characters, the graphene electrode serves as the set electrode in the graphene based RRAM (GS-RRAM), while

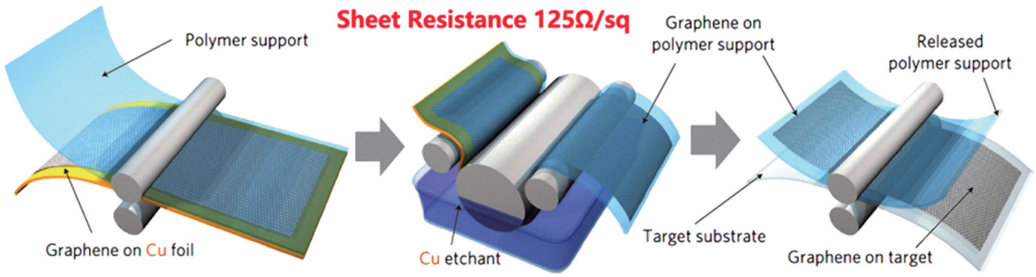


Fig. 4. (color online) The sheet resistance of graphene produced by a roll-to-roll method.[60]. The sheet resistance can be as low as ~ 125 Ω/sq.

the Pt electrode serves as the reset electrode in the Pt-based RRAM (Pt-RRAM). After 50 cycles of switching operations, the set/reset voltages and reset power distributions data are represented in Figs. 5(b) and 5(c), respectively. The lower accessing voltage and reset power dissipation demonstrate that using graphene as an electrode not only improves the scalability but also shows some kinds of power dissipation advantage. Further analysis was needed to figure out the mechanism.

Figures 5(d) and 5(e) are the mechanism schematic of Pt-RRAM and GS-RRAM respectively. By applying positive voltage to the TiN electrode in Pt-RRAM, the oxygen vacancies form a filament to connect TiN and Pt electrodes which makes the device state change from HRS to LRS (set process is achieved). Negative voltage ruptures the filament and the device is reset to HRS. Unlike the Pt-RRAM, when a negative voltage is applied to TiN, the oxygen ions quickly move into graphene since oxygen ions can migrate in graphene without barrier (set process is achieved). When positive voltage is

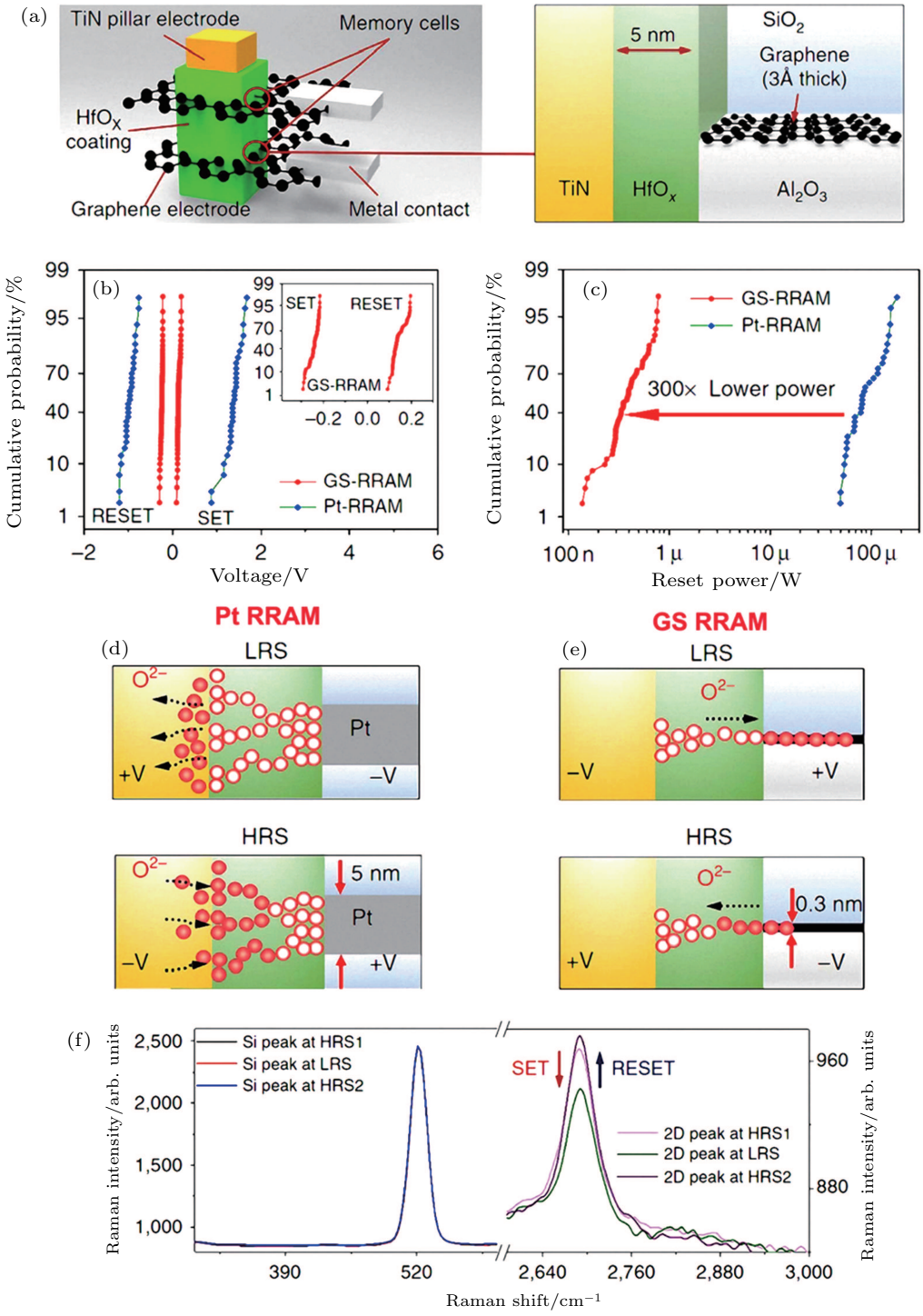


Fig. 5. (color online) Graphene-based 3D RRAM.[46] (a) The schematic of graphene-based 3D RRAM in vertical crossbar architecture. (b) The set/reset voltage distribution of Pt-RRAM and GS-RRAM after 50 cycles of switching. (d) Schematic of Pt-RRAM mechanism. (e) Schematic of GS-RRAM mechanism. (f) Changes of 2D peaks intensity of the graphene electrode during the switching process.

applied to TiN, the trapped oxygen ions in graphene are discharged, which ruptures the conductive filament and resets the device into HRS. Since the doping in graphene will reduce the 2D peak intensity in Raman spectra, Raman spectra can be used as a monitor to the oxygen migration in graphene.[58,59] Figure 5(f) shows the changes of 2D peak intensity as the oxygen is trapped (set process) and discharged (reset process). As we can see, when the device is set to LRS the 2D peak has a significant reduction which indicates the oxygen doping in graphene. Therefore, the key factor that results in the lower set/reset voltage is the good mobility of oxygen in graphene. The activation egergy of oxygen in graphene is only 0.15–0.18 eV,[61,62] which is much lower than that in TiN (0.95–2.1 eV).[63]

In summary, Lee *et al*. have demonstrated that graphene as the electrode in 3D vertical RRAM can be a promising candidate to solve the metal film sheet resistance limit and the good oxygen storage ability can also decrease the power dissipation in some kind of degree.

3.3. Ultrahigh density: crossbar area scaling down to 1.2×1.2 nm^2

With the impressive scaling race, NAND Flash memory, the dominative non-volatile memory, encounters multiple difficulties in scaling below 20 nm. RRAM using a two terminal structure owns greater potential in high integration density,[5] which has successively achieved a HfO_2-based memory cell with an area of less than 10×10 nm^2. However, to seek an even smaller crossbar structure, such as nanometer × nanometer, bulk materials are physically impossible up to providing a favorable interface in such an ultimate size. Unlike the bulk materials, atomic crystal can still hold perfect interface characters in low dimension which could be a promising candidate for realizing ultrahigh integration density of RRAM.

In order to explore the ultrahigh density memory, Chai *et al*. used CNT as electrodes to achieve the resistive switching function.[45] Firstly, the metal/a-C/CNT (a-C: amorphous carbon) cell was fabricated, the fabricate process is represented in Fig. 6(a). CNTs were transferred forward substrate as bottom electrodes and 30-nm-thick a-C layer was deposited in the region defined by lithography. Subsequently, Au metal film was deposited on a-C and CNTs which functioned as top electrode and bottom electrode measurement pads, respectively. The metal/a-C/CNT device shows a bipolar switching characteristics with ohmic-like behavior in LRS (Fig. 6(b)). However, in the metal/a-C/CNT structure, the conduction filament is composed by active metal Au which leads to the linearity of the switching characteristics. Further improvement is realized by composing a complementary structure: metal/a-C/CNT/a-C/metal (Fig. 6(c)), which is the anti-series of two bipolar memory cells. The four different threshold values, shown in the switching characteristics (Fig. 6(d)), allow information to be stored in two distinct high resistance states: "0" (LRS/HRS), "1" (HRS/LRS), which makes the cell always hold a high resistance when storing information.[18] Such a character can enable the crossbar cell without selected diode, which means a higher integration density. As a demonstration of ultrahigh density RRAM, the CNT/a-C/CNT device was fabricated and is shown in Fig. 6(e). The top CNTs were transferred orthogonal to the bottom CNTs and each crossbar area is 1.2×1.2 nm^2. The corresponding switching characteristics are shown in Fig. 6(f). However, the result only shows rectifying characteristics and is quite unstable.

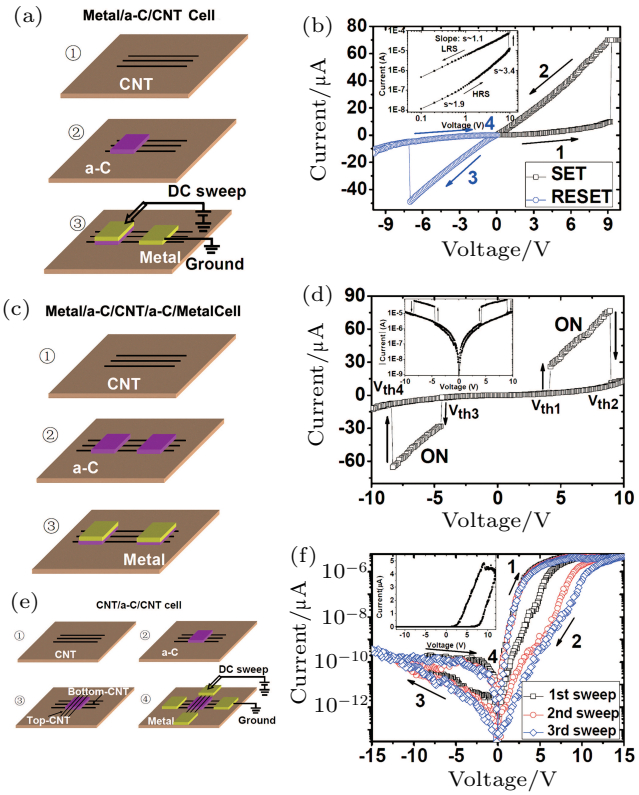


Fig. 6. (color online) CNT-based ultrahigh density RRAM.[5,45] (a), (b) Fabrication process of CNT-based RRAM with a metal/a-C/CNT structure (a-C: amorphous carbon) and the corresponding switching characteristics. (c), (d) Fabrication process of CNT-based RRAM with a metal/a-C/CNT/a-C/metal structure and the corresponding switching characteristics. (e), (f) Fabrication process of CNT-based RRAM with a CNT/a-C/CNT structure and the corresponding switching characteristics.

Although CNT with nanometer diameter is a promising candidate material to achieve ultrahigh density RRAM, the current technological level is still limited. During the device fabrication process, the ordered arrangement of CNTs, making CNTs parallel to each other, is hard to control and the alignment of top and bottom electrodes is also full of difficulties. The quality of CNTs is also not good enough for the electrode application. As the data of already measured devices showed, the CNTs devices are not robust: the metal/a-C/CNT device only successfully switched 27 cycles. Moreover, the switching medium material a-C is bulk material whose surface is quite rough, which would lead to a contact problem. In order to overcome the contact problem resulted by a rough surface,

it is necessary to explore the possibility of 2D materials serving as switching medium materials (such as hexagonal boron nitride[64] and graphene oxide[65–70]). In general, ultrahigh density RRAM based on CNT still has a long way to go and exploring the low-cost way to produce high-quality CNTs, developing reliable alignment technology, and seeking 2D materials as switching medium are three key points to achieve such a fantastic conception.

4. Power dissipation and device reliability

To achieve an optimal trade-off between cost and performance, nowadays the computing systems use a hierarchy of volatile and non-volatile architecture to store information.[1] The closest part to the microprocessor is using the fastest accessing memories: static random access memory (SRAM) and dynamic random access memory (DRAM), which are volatile memories. The main memory for non-volatile storage is using Flash memory, which has high density and non-volatile character, and is usually located in a separate chip because the fabrication technology is different from that of the microprocessor. The rise of RRAM has combined the advantages of both the fast accessing speed and non-volatile character, which could be a promising candidate to the next generation memory. However, compared with SRAM and DRAM, the energy per bit is still yet not low enough up to the cache application.[2] Furthermore, RRAM has a reliability problem, that are the difficulties of reproducing its electrical states and the resistance variations of different cells. 2D materials with atomic level flatness and unique characters can assist RRAM with low power dissipation and promote reliability.[48,49,59]

4.1. Power dissipation

When Chang *et al*. designed a resistive switching memory device based on active-layer:Zr:SiO_x, they discovered that a double-active-layer: Zr:SiO_x/C:SiO_x has a smaller power dissipation.[49] The device fabrication process is shown below. For the single-active-layer device: Pt/Zr:SiO_x/TiN, the active layer film (20 nm) was deposited on patterned bottom TiN electrodes by cosputtering with pure SiO_2 and Zr targets. For the double-active-layer device Pt/Zr:SiO_x/C:SiO_x/TiN, the active layer films C:SiO_x (6 nm) and Zr:SiO_x (14 nm) were deposited one after another with the same parameters as the single-active-layer device. The following electrical measurement shows that the double-active-layer device has a smaller forming voltage and lower current for both HRS and LRS (Fig. 7(a)). Further mechanism analysis was aided by Raman spectra, the result of the C:SiO_x insulator layer shows a typical graphene oxide (GO) Raman spectra (Fig. 7(b)).

Obviously, the existence of GO should be the reason for the low power, Chang *et al*. proposed a carbocycle model (Fig. 7(c)) to explain the power difference between two distinct devices. When the TiN electrode is applied with a negative voltage, the oxygen atoms inject into the C:SiO_x layer and the GO traps these oxygen atoms, which makes the carbon–carbon bonds stretched. In contrast, when the positive

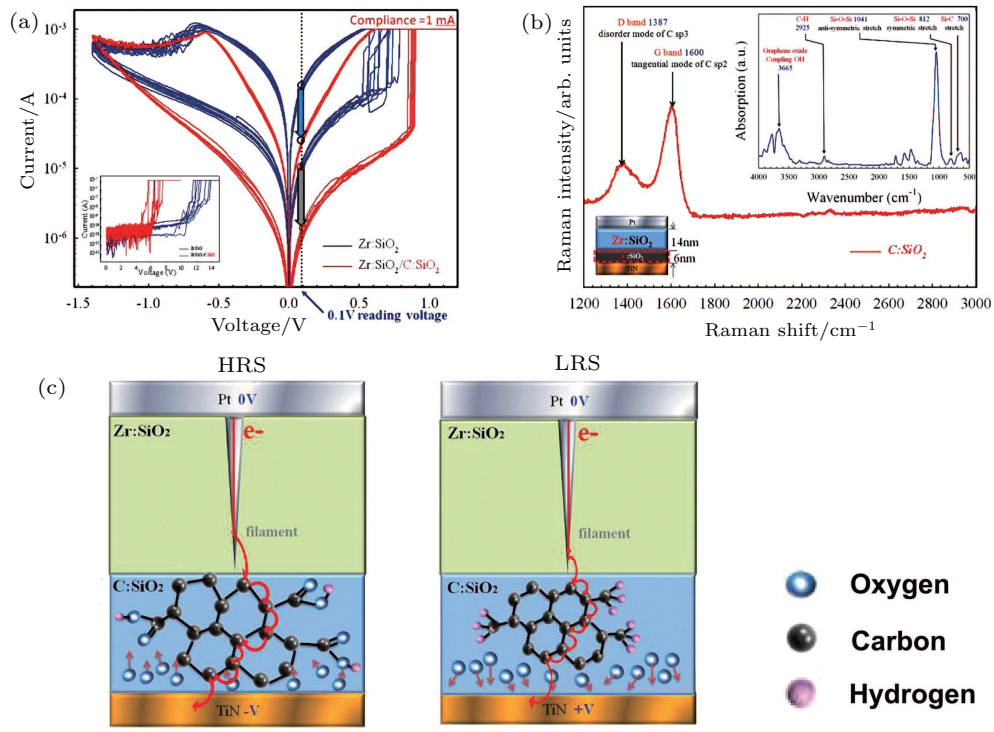


Fig. 7. (color online) Graphene-oxide-doped RRAM.[49] (a) The switching characteristics of Zr:SiO_x film (blue curve) and Zr:SiO_x/C:SiO_x film (red curve), respectively. (b) Raman spectra of C sp2 and C sp3 in C:SiO_x film, which confirms the existence of graphene oxide. (c) Schematic of graphene-oxide-doped RRAM mechanism.

voltage is applied, the trapped oxygen atoms are discharged and the carbon-carbon bonds recover. The electrons hop through the carbocycle and the corresponding hopping distance can be extracted from the current–voltage characteristics in different temperatures (the HRS hopping distance: 0.468 nm, the LRS hopping distance: 0.324 nm). Owing to the existence of GO in the active layer, the electrons hopping through the carbocycle in G, result in the favorable lower power dissipation.

As we have discussed in Section 3, using the graphene (treated by oxygen plasma) as an electrode can lead to a nonlinearity switching characteristics and some kinds of power saving. Here, further investigation has been made, by Qian *et al*., to analyze the potential of graphene as an electrode to the improvement of power dissipation.[48] Qian *et al*. combined large-area chemical vapor deposition (CVD) grown graphene and TiO_x based resistive switching memory to achieve low switching power and nonlinear switching characteristics. The interface between graphene and TiO_x has a critical effect on the memory performance.

There are three kinds of samples in this research of the graphene memory devices (GMDs): Pt/Ti/TiO_x/high-quality-graphene, Pt/Ti/TiO_x/low-quality-graphene and the Pt memory devices (PtMDs): Pt/Ti/TiO_x/Pt (Fig. 8(a)). For all kinds of devices, the conductive filament initial forming voltage is 8–10 V, which indicates that the forming process is electrical field driven.[2] Although all these types are based on the same switching medium TiO_x, the switching characteristics show large difference (Fig. 8(b)). The GMDs have lower working current than that of PtMDs, which leads to a significant lower power, and represent strong nonlinear characteristics, which indicates a barrier at the graphene/TiO_x interface. Figures 8(c) and 8(d) show the power and resistance distributions of the three types devices. There are many possible mechanisms in the graphene/TiO_x interface, such as Schottky barrier thermionic emission, direct tunneling, and Fowler–Nordheim tunneling. Since the *I*–*V* characteristics are symmetric and there is a low operation voltage, which means the electric field is not high enough to form a triangular barrier, the more likely the electron transport path should be direct tunneling. Subsequent theory calculation shows that the barrier widths are 0.35 nm and 0.94 nm for LRS and HRS, respectively. The barrier width difference is the reason for the resistance difference between LRS and HRS. Since graphene has a low density of states near the Dirac points,[71,72] the GMDs have lower tunneling probability than PtMDs which reasonably accounts for the higher resistance and lower power dissipation. Moreover, the GMDs based on low-quality graphene have a larger barrier width than devices based on high quality graphene. In general, the power saving of GMDs comes from the low density of state near Dirac points and the reduction of power is tunable by barrier width and the quality of graphene bottom electrode.

4.2. Device reliability

RRAM has reliability issues of large resistance variations and reproducibility of electrical characteristics, which hinder RRAM back from commercialization despite its other superior performance.[1] Here, Yang *et al*. have demonstrated that

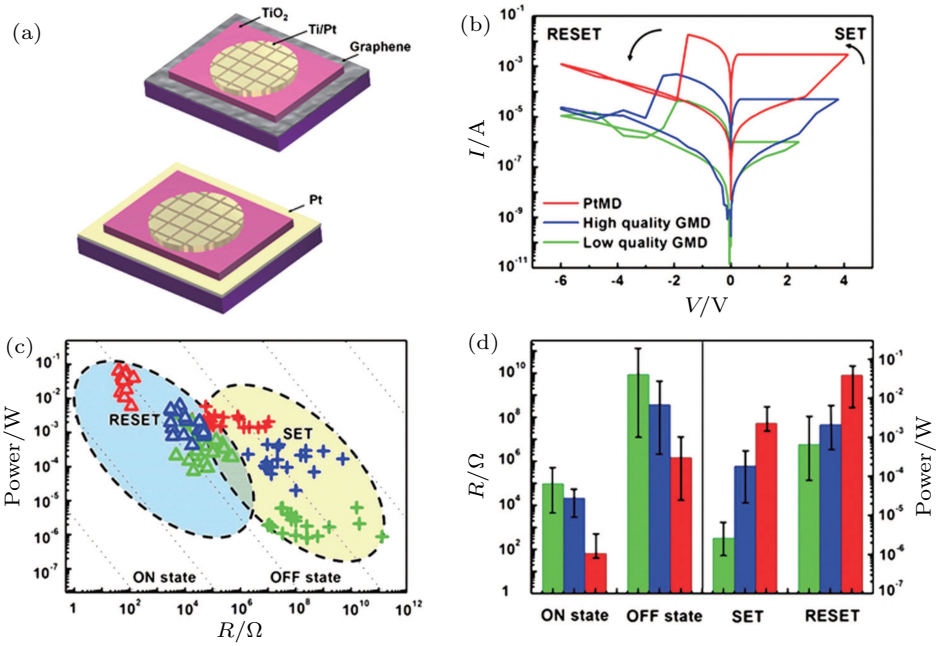


Fig. 8. (color online) Ultralow-power graphene RRAM.[48] (a) Schematics of GMDs (graphene memory devices) and PtMDs (Pt memory devices). (b) Switching characteristics of PtMD (red), high-quality GMD (blue), and low quality GMD (green), respectively. (c) The resistance and power distribution of PtMDs and GMDs with graphene of different quality. Red: PtMDs; blue: GMDs with high quality graphene; green: GMDs with low quality graphene. (d) The resistance and power distribution of PtMDs and GMDs with graphene of different quality. The error bars represent the minimum and maximum measured values. Red: PtMDs; blue: GMDs with high quality graphene; green: GMDs with low quality graphene.

ZnO-based RRAM employs atomic layered graphene showing significant reliability advantage. Graphene greatly suppresses the surface effect, which leads to a switching yield increasing and insensitivity to the environmental atmosphere.[50]

The devices use ITO (indium tin oxide) as top and bottom electrodes and employ 50-nm radio-frequency-sputtering ZnO as the switching medium, whose structure is ITO/ZnO/ITO. As a demonstration of the improvement of graphene to the device reliability, half of the devices are inserted with atomic layered graphene between top electrode and switching medium. The graphene film has sheet resistance as low as $\sim 30\ \Omega$/sq and $\sim 90\%$ optical transmittance, which prove the transparency of the devices. The switching characteristics of ZnO RRAM with/without graphene have the similar characters (Fig. 9(a)).

As we know, the defect in the interface can absorb O_2 molecules which makes the RRAM based on oxygen vacancies susceptible with the ambient oxygen partial pressure. When the oxygen partial pressure increases, the augmented oxygen in the interface will lead to reliability issues, such as switching yield falling and resistance variation. The use of atomic layered graphene will significantly improve such an undesirable phenomenon. Figure 9(b) shows the switching yield percentage of ZnO devices with/without graphene in four different oxygen partial pressure environments: a vacuum, N_2 ambience, air, and O_2 ambience. The switching yield percentage is defined as the ratio of the number of cells switching successively over 20 cycles to the total number of the cells. As we can see, compared with the N_2 ambience and air, the ZnO devices have much lower yield in the vacuum and O_2 ambience. Surprisingly, ZnO with graphene devices shows similar switching yield in different ambiences. The HRS of ZnO devices also show apparent resistance variation in the four different ambiences, the resistance arising with the oxygen partial pressure increases (Fig. 9(c)). Again, the ZnO with graphene devices have both stable HRS and LRS (Fig. 9(d)). Obviously, the graphene insert layer has played a key role in the switching yield improvement and resistance stability.

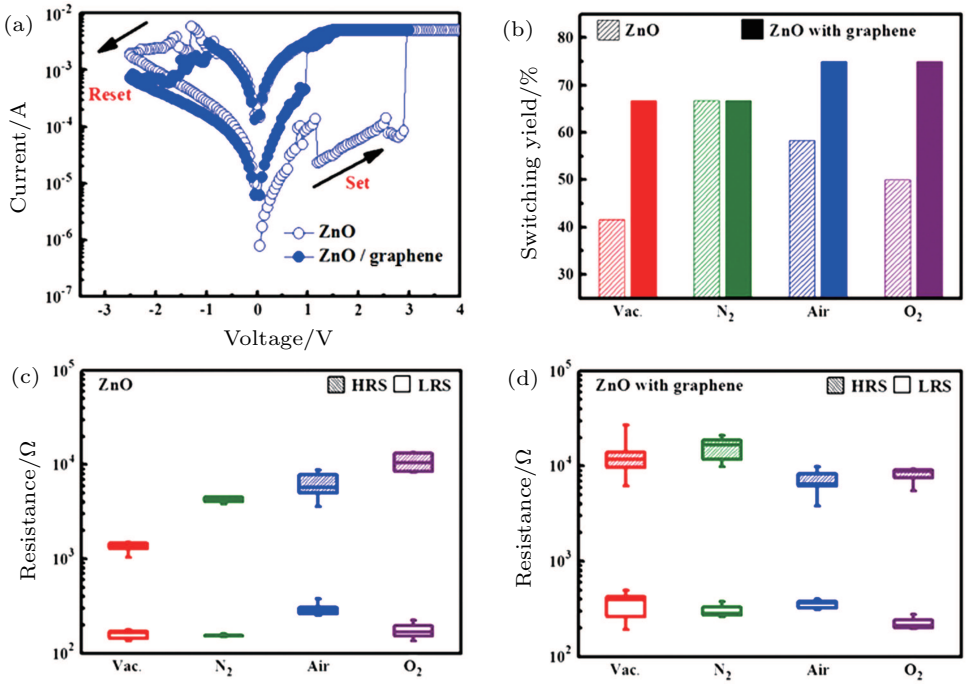


Fig. 9. (color online) Reliability improvement of RRAM induced by graphene.[50] (a) Switching characteristics of the ZnO-based RRAM with/without graphene layer. (b) The switching yield of ZnO and ZnO/graphene devices in different atmospheres. (c), (d) Box and whisker plots for the atmosphere-dependent resistance of ZnO and ZnO/graphene devices.

Several kinds of surface effect could have remarkable effects on the device performance, such as surface band bending,[73,74] chemisorption/photodesorption at the surfaces,[75] and surface roughness.[76] According to the previous researches, the trapped oxygen in the interface will affect the formation/rupture of conductive filaments, which leads to a fall of switching yield. The trapped oxygen can capture electrons which have a band bending effect in the interface. When the device is applied with a positive voltage, the interface will accumulate more oxygen ions that make the band bending effect more remarkable. Hence the devices have a higher resistance HRS when the oxygen partial pressure increases. While the LRS is based on a metallic conductive filament, the LRS is not affected by the oxygen partial pressure. When it comes to the role of graphene, according to the opinion of Yang *et al.*, graphene serves as a passivation layer because of weak chemisorption of O_2 molecules. While such a theory is controversial, many researches have reported the trapping oxygen ability of graphene.[58,59] Moreover, the HRS resistance values of ZnO with graphene devices are consistent with the HRS re-

sistance values of ZnO devices in high oxygen partial pressure. Consequently, the reliability improvement should be induced by the good oxygen storage ability of graphene, leading to a quite stable trapped oxygen density in the interface.

In the RRAM system based on active metal, the negative-SET behavior is also a reliability issue, especially for the programming failure. Liu *et al*. have demonstrated that such a harmful phenomenon is the reformation of the conductive filament with the active metal atoms in the counter electrode.[77] The transmission electron microscopy (TEM) and energy dispersive spectrometer (EDS) analysis were employed to further explore the negative-SET behavior. After inserting graphene between the resistive switching layer and inertia electrode, the active metal atoms filament only grows inside the resistive switching layer, which means the negative-SET phenomenon resulted by the filament overgrowth can be effectively suppressed by the graphene.

5. New type of devices

With the rapid expansion of atomic crystals researches, many fantastic phenomena and unique properties have been discovered. Taking advantage of these special features, there will appear the new possibility for memory devices. After the breakdown of graphene field effect transistors, there will be a nanogap existing in the middle of the channel and such breakdown devices have a resistive switching effect.[78] Although the resistive switching phenomenon is actually relied on the SiO_2 substrate,[79–82] graphene could provide a nanoscale gap,[83–86] which is favorable for device scaling down. The grain boundary (GB) in 2D materials is a harmful existence, which will lead to an accumulation of defects near the GB.[87–89] However, utilizing GB existence, MoS_2 field effect transistors could achieve the function of resistive switching memory[76] which is promising to scale the vertical height to 0.65 nm (the thickness of monolayer MoS_2). This section will discuss the two kinds of new type resistive switching memory. The graphene nanogap device is called a physical switch whose mechanism is based on a physical thermal effect and the GB MoS_2 device is called GB memory.

5.1. Physical switch: a new type RRAM based on graphene nanogap device

A graphene field effect transistor possessing resistive switching phenomenon after breakdown was firstly discovered by Standley *et al*. in 2008.[78] When they increased the applied voltage, the current abruptly increased after a slow augment for a while and then quickly fell off (Fig. 10(b)). Moreover, such a resistive switching effect is nonvolatile and the memory performance is considerable: the ratio of current between LRS and HRS I_{ON}/I_{OFF} is ~ 100, repeated set/reset over 10^5 without degradation, retention of both HRS and LRS are exceeding 24 hours at room temperature. The scanning electron microscope (SEM) image shows a nanogap at the middle of the channel after breakdown. In the theory of Standley *et al*. (Fig. 10(a)), after breakdown the channel has a nanogap in the middle which accounts for the HRS. Driven by electric field, there is a formation of linear chains of carbon atoms between the gap which leads to a state change from HRS to LRS. However, further researches demonstrate that the switching key of such a graphene nanogap device is more likely to be the formation of Si nanocrystal conductive filament in the SiO_2 substrate.[79–82]

In order to activate the resistive switching behavior of the two terminals graphene, liking the forming process of traditional RRAM, it is necessary to apply an adequate voltage to puncture the device. The forming process depends on the device pattern design and the breakdown voltage and current are linearly dependent on the channel length and width, respectively.[90] After the forming process there will be a nanogap, brought into being by the massive heat which is generated by large current density, in the channel. The gap usually occurs near the middle of the channel, which is the hottest place for a metallic graphene channel.[83–86] The depth of the gap has been demonstrated to have a larger value than the channel thickness, which indicates that the SiO_2 substrate must have some kind of crack.[90] Yao *et al*. taking advantage of in situ TEM has clearly illuminated the breakdown of SiO_2 substrate.[81] Figure 10(c) shows the schematic of the device structure and the cross-section TEM images before/after breakdown. Figure 10(d) is the high resolution TEM image, which represents the nanogap (width is ~ 15 nm) and the formation of Si nanocrystal which is different from the conventional diamond cubic structure. The switching characteristics of the physical switch are nonpolar, which means the set/rest operations can be achieved through positive–positive, positive–negative, negative–positive, and negative-negative voltage polarities (Fig. 10(f)).[90] Such nonpolar switching characteristics usually indicate a mechanism based on the thermal effect.[54,55] Further insight can be achieved by the temperature dependence of the switching characteristics (Fig. 10(f)).[90] With the decrease of temperature, the HRS current reduces significantly and the set operation is much more difficult to be executed. In the low temperature, higher set voltage is needed to provide enough heat to achieve the conversion: insulator SiO_2 to conductor Si nanocrystal.[79,80] In summary, the physical switch device is based on the thermal effect to form the conductive filament: Si nanocrystal and the graphene can provide a nanogap for further scaling down.

Utilizing a physical switch can realize multilevel and flexible storage. He *et al*. has explored the potential of a physical switch for multilevel switching (see Figs. 11(a)–11(c)).[90] In the reset process, different HRS can be achieved by using various reset voltage values. By sweeping the reset voltages to 5 V, 7 V, 9 V, 11 V, the device can be reset to four different HRSs (Fig. 11(a)). Different reset voltages can induce various

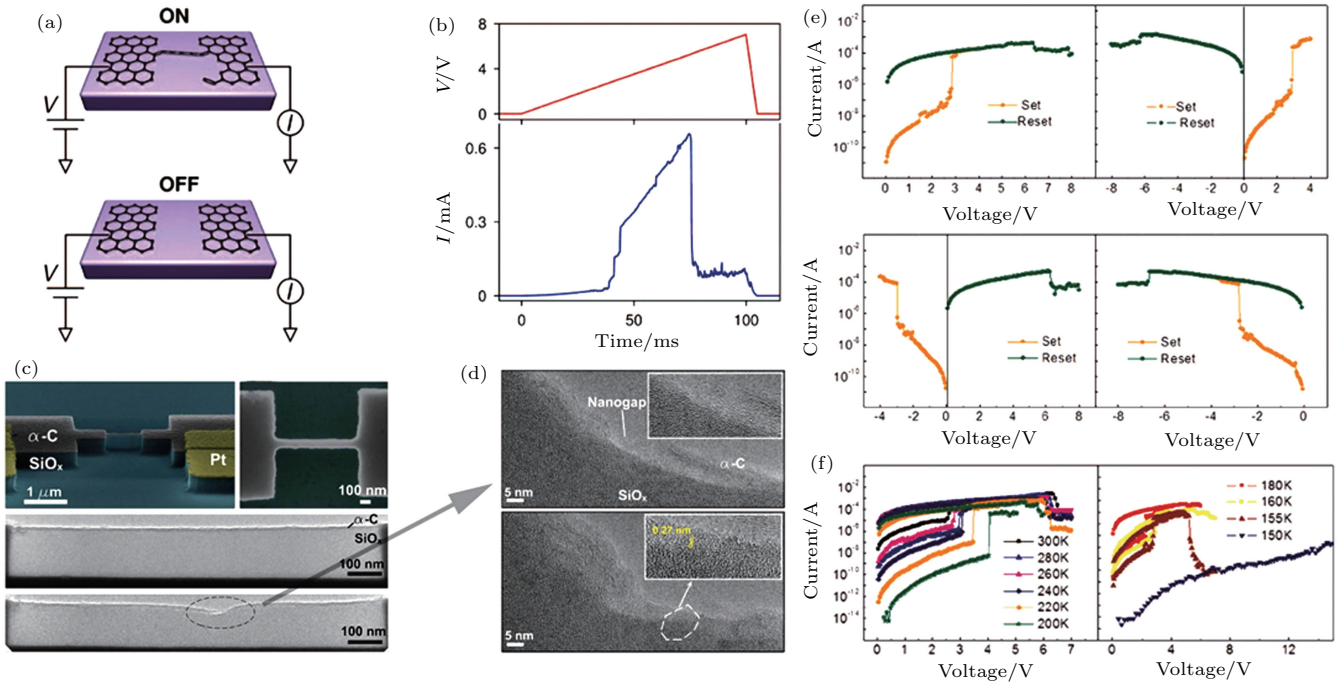


Fig. 10. (color online) The mechanism of new type RRAM: physical switching. (a), (b) Discovery of the resistive switching effect in the graphene field effect transistor.[78] (a) Schematic of mechanism and (b) demonstration of resistive switching effect. (c) Mechanism illustration of the physical switching.[81] The SEM images are the states before/after (up/down) breakdown. (d) The high magnification SEM images after breakdown.[81] The upper and bottom images show the nanogap and Si nanocrystal, respectively. (e) Nonpolar switching characteristics of the physical switching devices, which indicate that the device is based on the thermal effect.[90] (f) The relationship of set voltage value and temperature.[90]

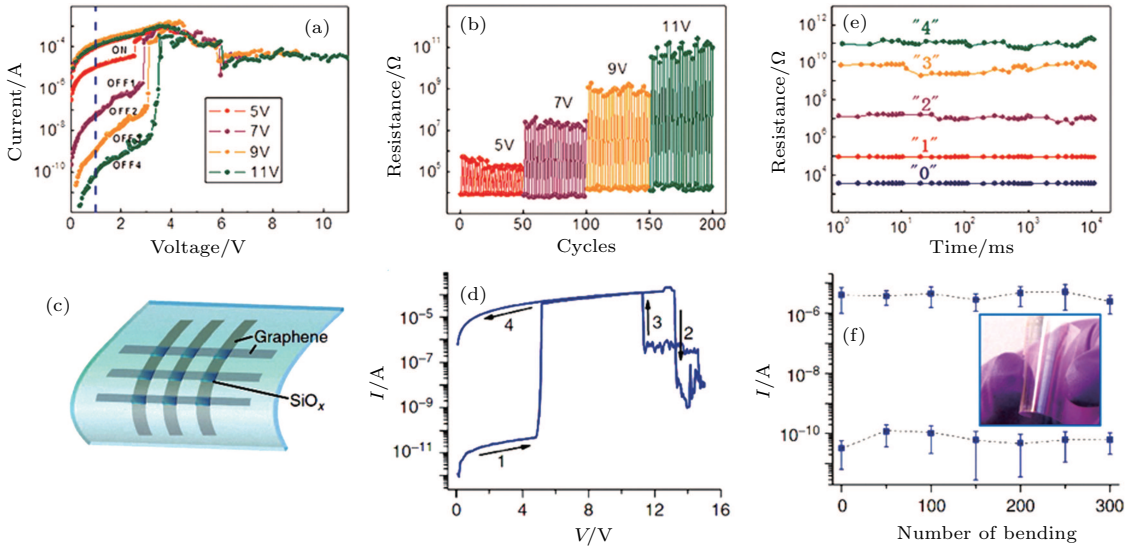


Fig. 11. (color online) The applications of new type RRAM: physical switching. (a)–(c) Multilevel storage ability demonstration of physical switching.[90] (a) Switching characteristics, (b) repeatable ability demonstration, and (c) each bit retention ability demonstration. (d)–(f) Flexible electronic storage demonstration.[91] (d) Schematic of graphene/SiO_x/graphene, (e) switching characteristics, and (f) demonstration of flexible storage.

oxidation degrees of Si nanocrystal filament and hence lead to distinct HRSs. Figure 11(b) shows the cycled switching of the device, reading pulse $\sim$ 1 V, and figure 11(c) demonstrates that the five distinct states are stable. By using a vertical structure: graphene/SiO_x/graphene (Fig. 11(d)), Yao *et al.* has successively fabricated flexible RRAM.[91] Figure 11(e) shows the switching characteristics of the devices. Repeated bending of the plastic substrate into a 1.2-cm-diameter curvature, the current ratio of LRS and HRS still holds a high value: $\sim 10^4$ (Fig. 11(f)) which reveals the potential for flexible memory.

5.2. Grain boundaries memory

Atomic crystals possessing numerous fantastic properties make them have broad applications in RRAM and provide promising solutions for the sneak leakage path, 3D integration, power dissipation, and reliability issues, as we have

discussed above. However, using 2D materials as the main switching medium is usually not suitable. The atomic level thickness and semiconductor characteristics (some of 2D materials) make the device based on 2D materials as switching medium usually have a power dissipation problem. There will be dislocations assembling near the GBs in 2D materials which could have some kinds of influence on the device's electrical and photoelectric performance.[87–89] However, Sangwan *et al.* has proved that a monolayer MoS_2 with GBs can serve as the switching medium and achieve the function of resistive switching memory.[51] With different kinds of GBs, the GBs MoS_2 devices represent favorable resistive switching characters, switching ratio up to $\sim 10^3$, and significant dynamic negative differential resistance (NDR). Moreover, with the modulation of back gate voltage, the GBs MoS_2 devices show tunable set voltage and resistance.

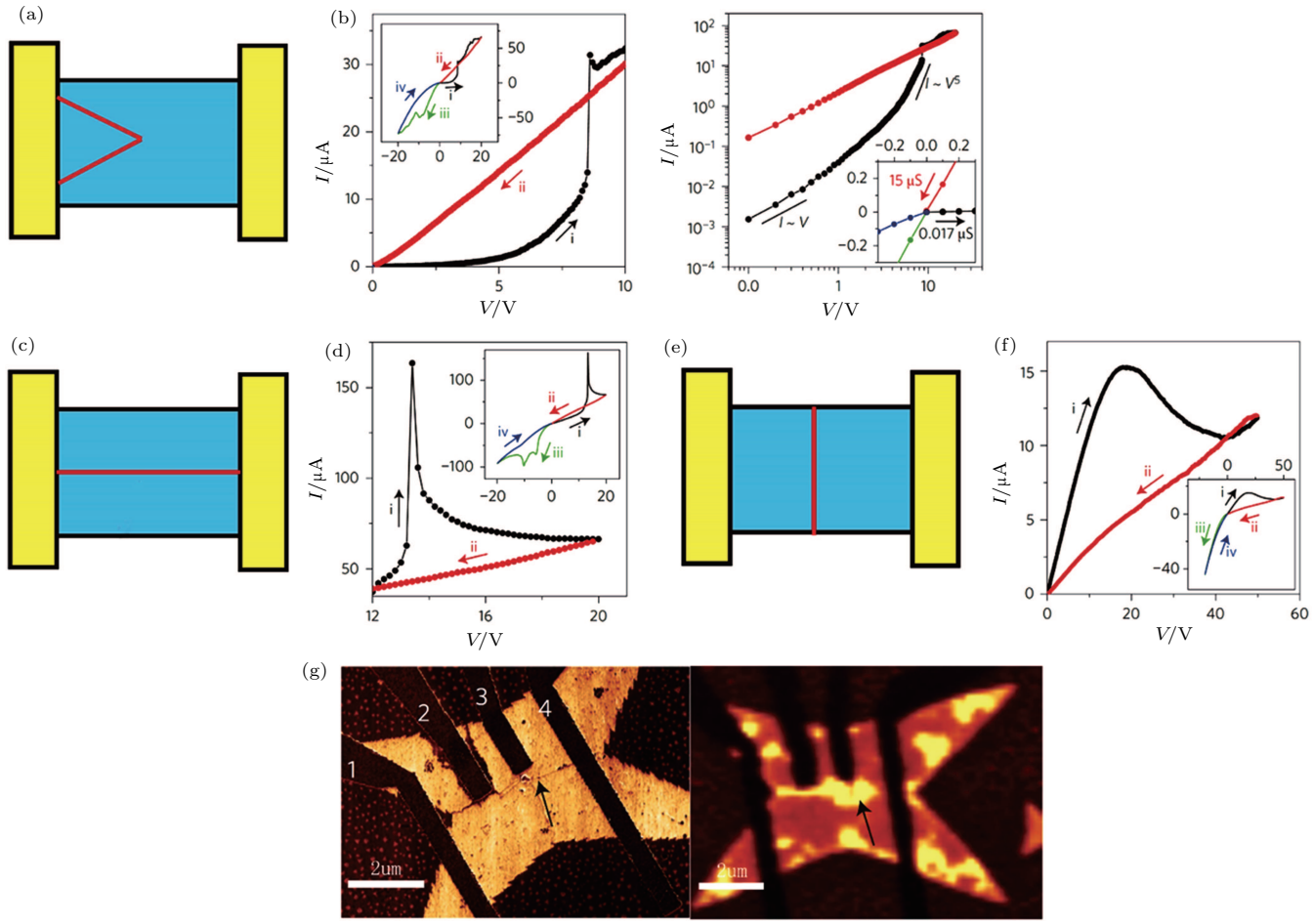


Fig. 12. (color online) New type of RRAM: resistive switching based on GB (grain boundaries) MoS_2.[51] (a), (b) Schematic structure and switching characteristics of an intersecting-GB device, respectively. (c), (d) Schematic structure and switching characteristics of a bridge-GB device, respectively. (e), (f) Schematic structure and switching characteristics of a bisecting-GB device, respectively. (g) AFM phase image and spatial mapping of the area under the PL excitonic peaks. Scale bars are 2 μm.

The channel material GBs monolayer MoS_2 is grown by CVD with a method to intentionally produce sulfur vacancies which lead to the GBs in the MoS_2. Two Au electrodes are used to define the channel and the highly doped Si substrate with 300 nm SiO_2 functioned as a control gate. Depending on the GBs types, the GBs MoS_2 devices are classed into three types: an intersecting-GB device: the GB is only connected to one of the two electrodes; a bridge-GB device: GB parallel to the channel and connecting the two electrodes; and a bisecting-GB device: GB perpendicular to the channel and does not connect to both of the electrodes (see Figs. 12(a), 12(c), and 12(e)). The intersecting-GB device has the best resistive switching memory character, with a resistance ratio, at zero bias, R_{HRS}/R_{LRS} up to 10^3 (Fig. 12(b)). At the beginning, the device is on a HRS. When applying a gradually increasing voltage to the device, there is an abrupt current increasing and the device converts into LRS. The LRS is holding until a large enough negative voltage is applied. Compared with the intersecting-GB device, the bridge-GB device always maintains a relatively low resistance without two stable distinct states (Fig. 12(d)), which indicates the existence of a conducting filament between two electrodes, and has the strongest NDR phenomenon. The bisecting-GB device possesses both resistive switching memory character and significant NDR phenomenon with broad current peak followed by a slow current decay (Fig. 12(f)). However, the resistive switch-

ing character is quite weak with a ratio of only $R_{HRS}/R_{LRS} \approx 4$ at zero bias.

Obviously, the resistive switching character depends on the existence of the GBs, which lead to the different resistive switching character in different GB devices. Because there will be defects accumulating near the GBs which are observed in other researches,[87–89] Sangwan *et al.* assigns the resistive switching phenomenon to the defects near the GBs. In order to achieve a visual image of the mechanism, the electrostatic force microscopy (EFM) and spatially resolved photoluminescence (PL) spectroscopy are employed to achieve insight of the operation mechanism. The EFM image of a bisecting-GB device shows a drastic potential drop, which is consistent with the relatively high resistance of the bisecting-GB device. On account of previous research indicating that sulfur vacancies will accumulate near GBs,[87–89] the electrons donated by dangling bonds should be the reason for the resistive switching character. Combining the atomic force microscope (AFM) phase image and PL spatial mapping, it can be noted that electroformed devices have higher concentrations of sulfur vacancies concentrations near the GBs (Fig. 12(g)). Therefore, the resistive switching mechanism of GBs devices should be based on sulfur vacancies. When the external voltage is applied, the sulfur vacancies migrate along the GBs and form a conductive filament, which lead to an LRS. Enough Joule heating will drive the sulfur vacancies to spread in all directions, which ruptures the filament and results in the HRS.

6. Conclusion

Undoubtedly, RRAM with $4F^2$ cell size,[19] switching in sub-nanosecond,[6] cycling endurances of over 10^{12} cycles,[7] and information retention exceeding 10 years,[7,8] is a promising candidate for next generation nonvolatile memory. However, additional construction is necessary to suppress the accessing error resulted by the sneak leakage path problem.[18,19] In 3D vertical RRAM, huge sheet resistance of metal film in nanoscale thickness degrades performance, which greatly hinders the development of RRAM in 3D.[20–22] Moreover, the variations of resistance between different devices and even different cycles of the same device holds RRAM back from commercialization.[1] Compared with volatile memory, such as DRAM and SRAM, the energy per bit of RRAM is still too high up to the application of cache.[2] These troublesome issues originate from the physical limits of bulk materials in low dimension. Atomic crystals with the interface in low dimension can provide atomic level solutions for such obsessional problems. The unique properties of atomic crystals also inspire a novel idea about new type of RRAM.

The relatively high current of LRS in small voltage leads to the sneak leakage path problem, which affects the accessing operation. Inducing few-layers graphene as the bottom electrode, successively lead to a nonlinearity in switching characteristics.[46] The functioned graphene serves as a 2D diode, inducing a nonlinearity ratio $I(V_{read})/I(V_{read}/2) \sim 280$, which debases sneak leakage current ~ 2 orders. Graphene, as atomic crystal, intrinsically possessing only one-layer atom represents the plane thickness minimum limit and can be a large area produced with sheet resistance as low as 125 Ω/sq.[60] Using graphene as an electrode can break through the metal film sheet resistance limit in 3D vertical RRAM.[46] Moreover, CNT with nanometer diameter can serve as a promising electrode material to achieve ultrahigh RRAM.[45] The low density of state near Dirac points in graphene[71,72] can be designed to realize power saving, because the low density of state can decrease the tunneling probability.[48] The reliability resulted by the interface state and the overgrowth of active atoms can be improved by the 2D materials intrinsic atomic level flatness and dangling free surface.[50,77] Except for solving the integration density, power dissipation and reliability issues, the unique properties of atomic crystals also inspired the novel idea about RRAM. Combining the nanogap generated by graphene breakdown and SiO_2 substrate can achieve a nonpolar physical switch.[78,81,90,91] Utilizing the sulfur vacancies accumulated near the grain boundaries in monolayer MoS_2 can achieve single layer thickness (0.65 nm) plane RRAM.[51]

Although atomic crystals provide various aspects of improvement and the novel idea for the RRAM, there are still some challenges among the atomic crystals application in RRAM. The challenges mainly focus on the immature fabrication process and materials quality. The RRAM based on CNT is an exploration of ultrahigh density RRAM, while the device only successfully switched 27 cycles.[45] Such a fragility comes from the quality of CNTs and the rough surface of bulk material a-C. Moreover, the alignment technology with nanometer precision is necessary to put the CNTs in order. Memory is formed by periodic repeated cells, the uniformity of the film is a key factor to decide the uniformity of memory. As Qian *et al.* has shown, the different quality of graphene as an electrode has a greatly different electrical performance.[48] As for the new type of device, the fabrication of memory array is a big fabrication challenge, such as the control of the breakdown point in the physical switch and GBs place in GB memory. In addition, exploring 2D materials as a switching medium or an inserted layer in the switching medium is also necessary for acquiring a more ideal interface, such as hexagonal boron nitride[64] and graphene oxide.[65–70]

Acknowledgment

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