Investigation on latch-up susceptibility induced by high-power microwave in complementary metal–oxide–semiconductor inverter*

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The latch-up effect induced by high-power microwave (HPM) in complementary metal–oxide–semiconductor (CMOS) inverter is investigated in simulation and theory in this paper. The physical mechanisms of excess carrier injection and HPM-induced latch-up are proposed. Analysis on upset characteristic under pulsed wave reveals increasing susceptibility under shorter-width pulsed wave which satisfies experimental data, and the dependence of upset threshold on pulse repetitive frequency (PRF) is believed to be due to the accumulation of excess carriers. Moreover, the trend that HPM-induced latch-up is more likely to happen in shallow-well device is proposed.Finally, the process of self-recovery which is ever-reported in experiment with its correlation with supply voltage and power level is elaborated, and the conclusions are consistent with reported experimental results.

Keywords: high-power microwave, latch-up, repetitive pulse frequency, supply voltage dependence

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1. Introduction

As electronic systems increasingly demand the reliability of integrated circuit especially in harsh electromagnetic environments, research on susceptibilities of devices and systems under electromagnetic interference (EMI) effect have been a hotspot. High-power microwave is a typical instance in inducing EMI, which is easy to couple into electronic systems through antennas of receiver (commonly referred to as front-door) or apertures on shell, interconnected wires and power cables (commonly referred to as back-door).[1] These intentional or unintentional electromagnetic pulses can result in temporary breakdown, permanent malfunction or catastrophic physical damage.[2]

Several pieces of experimental and theoretical research on HPM effects have been carried out in recent years. Influences on devices in different processes, computer systems[3] and radio link systems[1] are studied and summarized in experiment. Bargstädt-Franke *et al.*[4] and Wang *et al.*[5] revealed pulse width dependences, frequency dependences and supply voltage dependences of upset threshold power and energy. However, few theoretical analyses were carried out in the above works. Yu *et al.*[6] and Liu *et al.*[7] reported the HPM damage mechanism of high electron mobility transistor, which is widely used in the low noise amplifier in the radio frequency system. Ma *et al.*[8–11] and Chai *et al.*[12] presented the physical failure theory of bipolar transistor and proposed several hardening measures against HPM. In back-door couple scenario, it is believed that latch-up is a significant factor leading to upset.[13] Kim and Iliadis[14] explained latch-up mechanism and frequency dependence of complementary metal–oxide–semiconductor (CMOS) inverter by direct injection through gate terminals. Chen and Du[15,16] theoretically explained the effects of frequency, width, pulse repetitive frequency and device bias by simulation, whereas these analyses are based on circuit level. Yu *et al.* analytically discussed and deduced the effects of frequency, width and temperature combining with the distribution of fundamental physical quantities.[17–19] However, several experimental phenomena of latch-up in CMOS inverter induced by high-power microwave and relevant factors which are widely involved remain to be solved and explained in more detail.

In this work, a two-dimensional CMOS inverter is modeled and on the basis of this, the mechanism of high-power microwave-induced latch-up is studied. The latch-up dependence on high-power microwave signal parameters including duty cycle and pulse repetitive frequency is explained by comparing with existing data, and the relationship between upset average power threshold and duty cycle is obtained analytically. The dependence of upset power on depth of well is revealed. In addition, the supply voltage dependence along with the resulting self-recovery characteristic discovered in experiment before is explored.

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2. Simulation set-up

The schematic diagram of the tested CMOS inverter under n-well process with a parasitic p–n–p–n structure is depicted in Fig. 1, and several structural parameters including total lateral length, substrate thickness and well depth are marked. The gate length is specified to be 0.35 μm. Q_1 and Q_2 represent the parasitic NPN and PNP transistors, whereas R_s and R_w are equivalent resistances of substrate and well, respectively. The temperature of the device base is specified to be ambient (300 K) as a thermal boundary to simulate practical application condition. The inverter works at a supply voltage of 3.3 V under normal conditions with mid-point voltage (V_m) located at about 1.6 V as indicated in Fig. 2. The external HPM that is assumed to be sinusoidal plane wave and has been proved to be reasonable in experiment,[20] is injected into the device via the source terminal of NMOS to emulate the process of back-door coupling, in which power wires and ground wires are susceptive objects, especially in a digital integrated circuit.

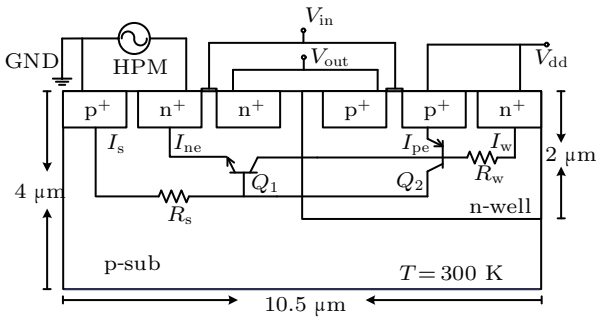


Fig. 1. Schematic diagram of CMOS inverter with a parasitic p–n–p–n structure.

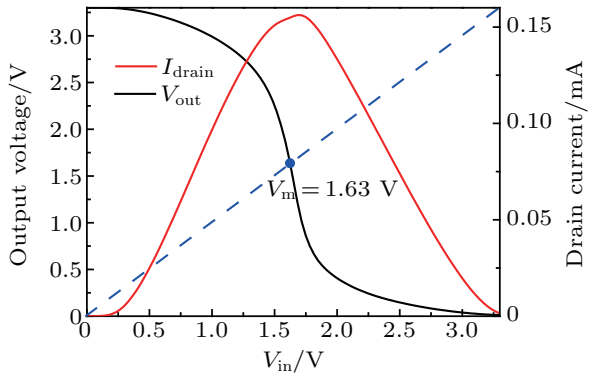


Fig. 2. (color online) Voltage transfer curve and current transfer curve of the inverter adopted with a mid-point voltage of about 1.63 V.

3. Results and discussion

3.1. Upset mechanism

The inverter output voltages varying with time versus microwave injected into NMOS source port are shown in Fig. 3. The high power microwave is applied in a time interval from 0 ns to 10 ns, and the black solid line and red solid line represent the inverter output voltage under microwave with power levels of 13.5 dBm and 19.5 dBm, respectively. It can be seen during the action of external microwave, the output voltages under both 19.5-dBm and 13.5-dBm microwave show bit errors. For the case of 13.5 dBm, the output voltage recovers to normal value (3.3 V) and succeeds in responding to input after the microwave signal has been removed. However, the output voltage affected by a microwave of 19.5 dBm still maintains a wrong value (about 1 V) after the HPM has been removed and the inverter fails to respond to input. Moreover, the source terminal currents of PMOS are displayed by dashed lines in Fig. 3. For an inverter, the source current should be kept at about zero without input change under normal circumstances, which gives rise to little static power consumption of CMOS inverter. The current response under 13.5-dBm microwave (represented by black dashed line) is kept at 0 mA after 10 ns, whereas the current under 19.5-dBm microwave (represented by red dashed line) shows an abnormal rise which cannot be ignored after the microwave has been removed, indicating that a latch-up current path from power supply terminal to ground forms.

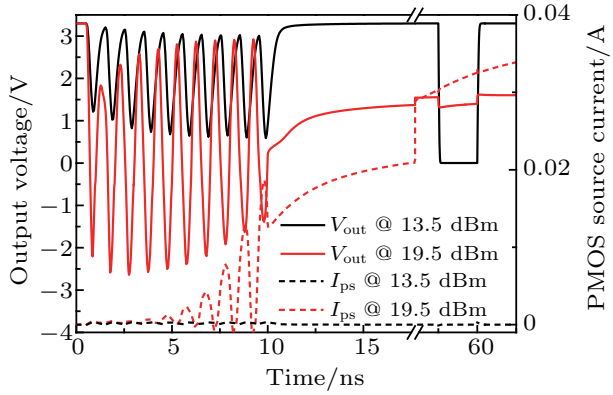


Fig. 3. (color online) Output voltage response and source current of PMOS under microwave powers of 13.5 dBm (in black) and 19.5 dBm (in red).

The emulated electron current density distribution of NMOS side during the negative half cycle of injected microwave is shown in Fig. 4(a). The grounded bulk terminal along with negative potential source terminal forms a forward PN junction current path, and a large number of carriers flow into the substrate. However, this PN junction is biased reversely hence few carriers flow out of the substrate during the positive half cycle (seen in Fig. 4(b)). Partial excess minor carriers (electrons in p-substrate) accumulate at the border of the substrate close to n-well, leading to the fact that drift rather than diffusion across depletion region plays a dominant role, and flow into n-well. Once the diffusion current formed by these carriers inside n-well is large enough to lead to a sufficient voltage drop, the parasitic PNP transistor is switched on. On the other hand, excess holes from n-well lead to a sufficient voltage drop through substrate and trigger NPN transistor, and there forms a latch-up path. Oppositely, the output voltage

gets back to normal if the injected carriers are unable to trigger latch-up path.

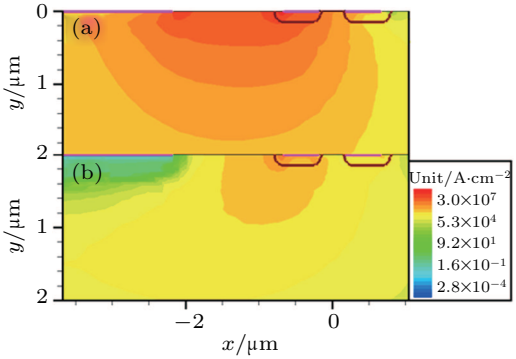


Fig. 4. (color online) Distributions of electron current density in near source and bulk terminal of NMOS. (a) At the negative half cycle of injected microwave; (b) at the positive half cycle of injected microwave.

3.2. Latch-up dependence on HPM duty cycle

Several studies on HPM signal parameter dependence of latch-up upset effect have been reported. However in these studies, continuous wave is generally used to substitute HPM. Actually, in real-world situation HPM is produced with a certain duty cycle which is usually not 100% nor certain repetitive intervals. In this section, the stimulus acted is specified by a single-shot sinusoidal source with various duty cycles. The condition under repetitive pulses will be presented in the following section.

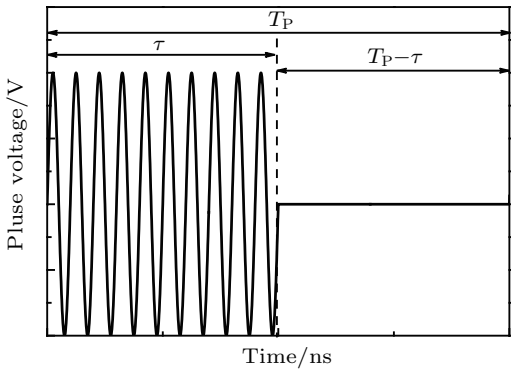


Fig. 5. Waveform pattern of injected HPM.

The waveform injected into the source terminal of NMOS is illustrated in Fig. 5, where τ and T_p represent pulse width and period, respectively. The injected average power (P_{ave}) and peak power (P_{peak}) are defined as follows:

$$P_{ave} = \frac{P_{peak} \times \tau}{T_p}. \tag{1}$$

A single-shot pulse with a fixed period of 20 ns is injected into source terminal of NMOS. Figure 6 shows simulated upset peak power threshold and calculated average power threshold as a function of pulse width. The curves show decreasing trend on upset peak voltage threshold as width (equivalent with duty cycle) increases, since a certain number of excess carriers are needed to trigger the latch-up path,[4] and the simulated result satisfies the experimental results reported in Ref. [21]. However, an opposite trend appears on the upset average power threshold. The result indicates that for pulses with the same period, the one with a shorter width (lower duty cycle) is easier to upset the device, that is to say, the CMOS inverter is more susceptible under a pulse with shorter width than under a continuous wave for a certain average power.

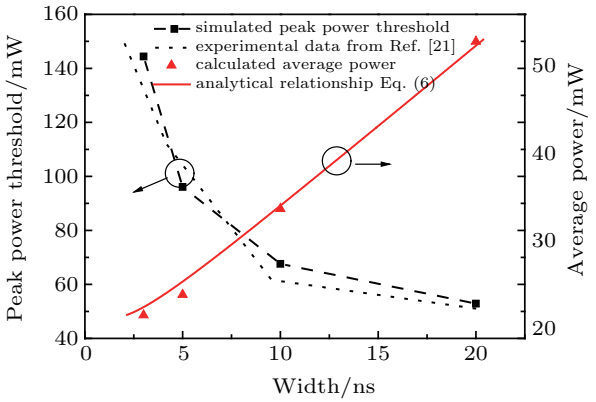


Fig. 6. (color online) Upset peak power compared with experimental result in Ref. [21] (normalized value) and average power thresholds along with analytical relationship (6) as a function of width.

A simplified process of calculation is presented to explain it as follows. Consider the injected carriers near NMOS source terminal. Now it is assumed that the PN junction formed by source terminal and substrate satisfies the ideal *I*–*V* relationship as follows:

$$I = I_{rs}\left(\exp\left(\frac{qV}{kT}\right)\right), \tag{2}$$

where I_{rs} is the reverse saturation current, q is the charge of an electron, k is the Boltzmann constant, T is the temperature, and V is the voltage across source terminal and substrate. The relationship between pulse width τ and average power P_{ave} is described as follows:

$$P_{ave} = \frac{V_a^2}{R} \times \frac{\tau}{T_p}, \tag{3}$$

where V_a is the voltage of injected microwave, τ is the pulse width, R is the device equivalent resistance, and T_p is the period of microwave. Combining Eqs. (2) and (3), the injected total quantity of charge Q is obtained as follows:

$$\begin{aligned} Q &= \int_0^{\tau} I_{rs} \exp\left[\frac{q}{kT}\left(\frac{P_{ave}T_pR}{\tau}\right)^{1/2}\alpha\right] \mathrm{d}t \\ &= I_{rs} \exp\left[\frac{q}{kT}\left(\frac{P_{ave}T_pR}{\tau}\right)^{1/2}\alpha\right]\tau, \end{aligned} \tag{4}$$

in which α is an equivalent coefficient in order to simplify the sinusoidal signal as DC one. According to the analysis above in Subsection 3.1, the inducement of latch-up is the imbalance of drift-diffusion between n-well and p-substrate, hence the minor carrier density of substrate close to n-well n_{sw} is the key to determining whether latch-up occurs. The relationship

between Q and n_{sw} is proposed in Ref. [19] and expressed as follows:

$$n_{sw} = \Delta n(x,\tau)|_{x=L_B} = \frac{Q}{S}\int_0^{D\tau} \frac{L_B}{2\sqrt{\pi D_n}} \times \frac{1}{(\sqrt{D\tau - t})^3 \exp\left[\left(\frac{L_B^2}{4D_n(D\tau - t)} + \frac{D\tau - t}{\tau_n}\right)\right]} dt. \quad (5)$$

where S is the cross sectional area of device, D is an equivalent coefficient to simplify the modeling process by converting the sinusoidal microwave pulse into a DC pulse, L_B is the lateral length of device, D_n is the diffusion coefficient, τ_n is the lifetime of electrons, and t is time. Combining Eqs. (4) and (5), the n_{sw} can be expressed as follows:

$$n_{sw} = \frac{I_{rs}}{S}\exp\left[\frac{q}{kT}\left(\frac{P_{ave}T_pR}{\tau}\right)^{1/2}\alpha\right]\tau \cdot \int_0^{D\tau} \frac{L_B}{2\sqrt{\pi D_n}} \times \frac{1}{(\sqrt{D\tau - t})^3 \cdot \exp\left[\left(\frac{L_B^2}{4D_n(D\tau - t)} + \frac{D\tau - t}{\tau_n}\right)\right]} dt, \quad (6)$$

Regarding n_{sw} as a constant value to trigger latch-up, equation (6) shows the relationship between average power P_{ave} and pulse width τ. The fitting curve is also exhibited in Fig. 6, and satisfies the simulation result, demonstrating the analytical relationship (6) and analysis in Subsection 3.1 is valid and reliable, and therefore microwave with a shorter duty cycle is easier to induce upset under the condition of same average power.

3.3. Dependence on pulse repetitive frequency

However, the discussion above is based on single-shot microwave pulse and the accumulation of excess carriers is not taken into consideration. The simulated variation of upset power threshold with PRF ranging from 0 MHz to 200 MHz is depicted in Fig. 7. Two periods of microwave pulse with intervals are injected and the width of each pulse is specified to be 5 ns. As can be seen, the upset power threshold keeps at 96.1 mW at low PRF, whereas an obvious decrement occurs with PRF exceeding about 60 MHz. Moreover, the data reported in Ref. [15] are also shown in Fig. 7 for comparison, and the two curves exhibit the same trend. According to Ref. [15], a lower power threshold appears when PRF is much larger than $1/\tau$. However in this work, the excess minor lifetime is extracted to be about 1 μs, indicating that there is another cause taking effects to lower the power threshold in repetitive pulses along with minor recombination effect proposed in Ref. [15].

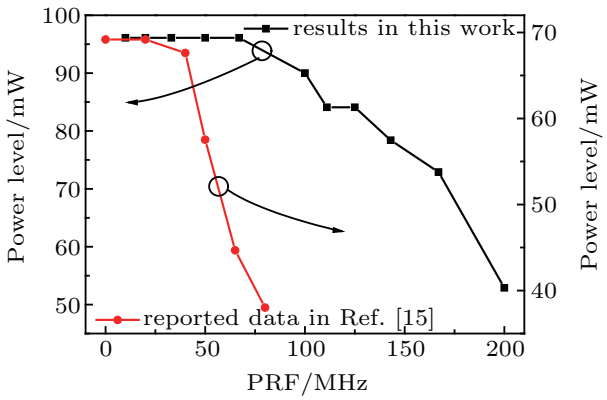


Fig. 7. (color online) Simulated upset threshold power dependence on pulse repetitive frequency and reported data in Ref. [15]. The width is specified to be 5 ns and two period pulses are injected in our work.

In order to investigate the repetitive pulse effect in more detail, electron density distributions as a function of lateral position x at the depth of 1 μm at different times are shown in Fig. 8, for the repetitive frequencies of (a) 0 MHz and (b) 100 MHz. The peak power is specified to be 90 mW.

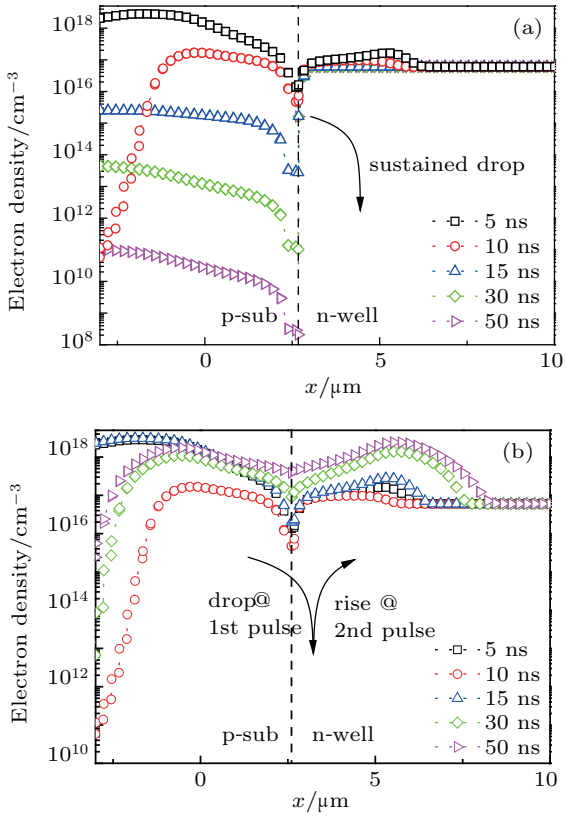


Fig. 8. (color online) Semi-logarithmic electron density distributions as a function of lateral position x at depth of 1 μm and their variations with time for PRF = (a) 0 MHz and (b) 100 MHz.

In Fig. 8(a), it is obvious that the excess electrons injected into p-substrate lessen with time, and it is because the injected excess electrons hinder the diffusion effect from n-well to p-substrate at n-well border and cause the electron drift effect to be dominant. For single-shot condition, electron drift effect lasts long enough so that neither sufficient cumulative electrons to form enough electron stream from p-sub to n-well, nor

latch-up occurs. For the condition of 100 MHz in Fig. 8(b), it is different. Electrons in p-substrate at 10 ns are fewer than at 5 ns due to drift effect. However at 10 ns, the second pulse works and makes electron density at 15 ns (blue line) more than at 5 ns (black line) due to the electron accumulation. The electron density on the n-well side of depletion region becomes large enough, causing the abundant diffusion current inside n-well to form a voltage drop which enables switching on the PNP transistor. Thereby, latch-up occurs under repetitive pulses. Higher PRF emphasizes this accumulation effect, leading to a decline on upset power threshold with PRF increasing. Moreover, for the repetitive pulses with low PRF, the interval between pulses is long enough so that almost all the carriers from the last pulse flow into n-well and thus the accumulation effect of p-substrate electrons can be ignored. Hence it is reasonable to treat the repetitive pulses as independent ones, and upset threshold power at low PRF is nearly constant. Besides, the recombination of excess carriers also contributes to this process.

3.4. Dependence on well depth

According to the analysis above, the requirement for latch-up is enough diffusion current to form sufficient voltage drop in n-well, and the diffusion current is dependent on the density of excess carriers across PN junction, considering the density of excess carriers in substrate close to n-well, which is affected by diffusion from p-substrate and drift from PN junction. Accumulated excess carriers from diffusion are irrelevant to the depth of well since these are formed by HPM injection essentially. However, the drift current from substrate to n-well is as follows:

$$I = \sigma E S, \tag{7}$$

where σ and E represent the conductivity and electric field strength of space charge region, and the current is in direct proportion to cross sectional area S, that is to say, a larger well depth results in a larger drift current, and the density of excess carriers in substrate close to n-well is lower, therefore diffusion current in n-well is lower. In order to trigger the parasitic transistor, a higher power level of HPM is needed.

The simulated upset power level variations with pulse width at different well depths are shown in Fig. 9. It can be seen that with the increase of well depth, the upset power level becomes larger, especially at short pulse width. Moreover, the electric field strength and electron density variation with vertical y axis at the border of substrate and well are shown in Fig. 10. The values of electric field strength are similar at different values of well depth D, whereas for a larger D, the electric field extends more, and the electron density becomes lower, which satisfies the analysis above. Therefore, it is believed that the devices are more resistant to HPM in deep well process.

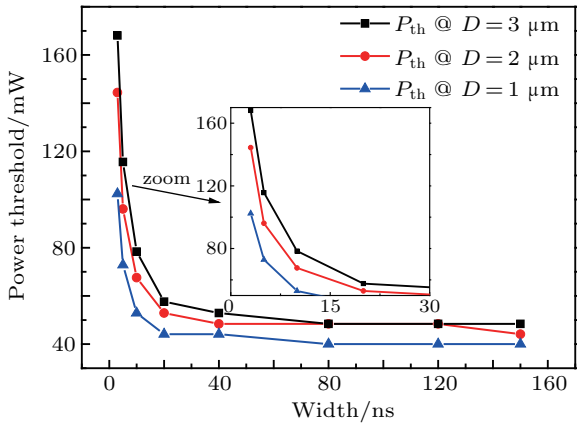


Fig. 9. (color online) Variations of upset power threshold with pulse width at diverse well depth.

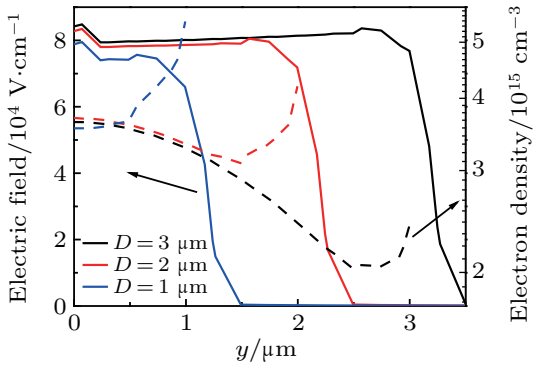


Fig. 10. (color online) Variations of electric field strength (solid lines) and electron density (dashed line) with y axis at the border between substrate and well.

3.5. Supply voltage dependence and self-recovery characteristic

Since the device may be used in a range of supply voltages according to the practical requirement, it is valuable to investigate the transient latch-up under diverse supply biases. The output responses under supply voltages of 3.3 V and 2.7 V are shown in Fig. 11, and the injected power level is specified to be 67.6 mW. It shows the malfunction after microwave pulse has been removed at 10 ns with $V_{dd} = 3.3$ V, however, the output voltage turns into self-recovery toward correct level after a period of time under 2.7 V supply voltage. The phenomenon is consistent with that indicated in Ref. [5], in which self-recoverable latch-up effect under low supply voltage is proposed. The duration from the removal of microwave to the occurrence of self-recovery is defined as delay time in this paper. The extracted simulated delay times as a function of supply voltage V_{dd} under different injection power levels are shown in Fig. 12. The result reveals that the delay time becomes shorter with the decrease of V_{dd}, whereas no self-recovery is discovered under higher supply voltage during simulation. Moreover, the injection power level increasing from 18.3 dBm to 19.5 dBm extends the delay time under the same supply voltage, however for an injection power of 17.9 dBm, the delay time has similar values under different supply voltages.

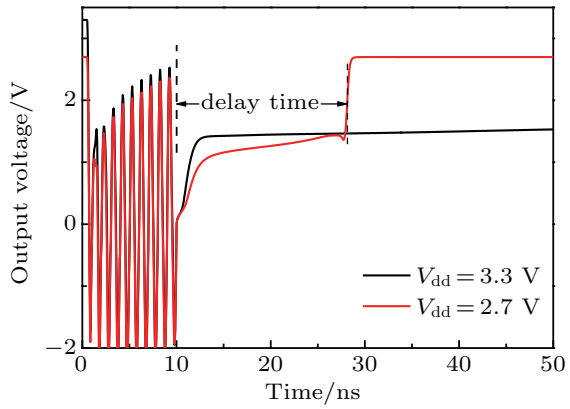


Fig. 11. (color online) Output voltage responses under different supply voltages. The power level of microwave injected through source terminal of NMOS is specified to be 67.6 mW.

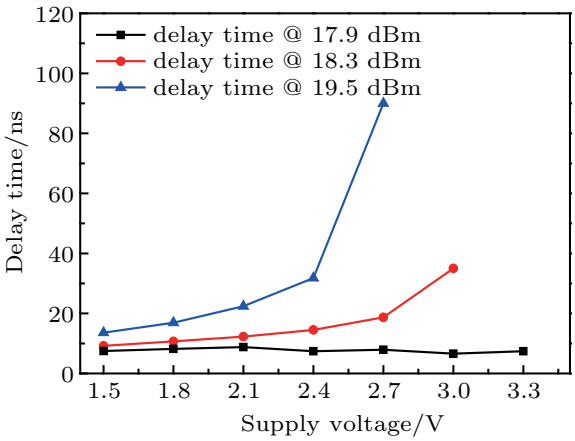


Fig. 12. (color online) Extracted delay times as a function of supply voltage V_{dd} under different power levels.

When the transient latch-up occurs, both NPN and PNP parasitic transistors work in the forward-active region, which satisfies the following equation:

$$V_{dd} - I_w R_w > I_s R_s, \tag{8}$$

where I_w and I_s are the currents flowing through resistances in n-well (R_w) and substrate (R_s), respectively (see Fig. 1). Because of the low-impedance of latch-up path, the current from P-source to N-source (I_{pe} and I_{ne} in Fig. 1) increases, while partial n-well/substrate currents through R_w and R_s (I_w and I_s) become larger at the same time due to the high potential of n^+ in n-well and low potential of p^+ in substrate. Once equation (8) does not hold true, the collector junctions of parasitic transistors are invalid, and the excess carriers flow out of device to supply or ground. This process is illustrated in Fig. 13, where increasing current appears to flow through substrate and source terminal after HPM has been removed. Besides, the increases of resistances in well and substrate due to temperature also contribute. Since the latch-up trigger current results from external carrier injection in essence, the value of I_w is irrelevant to V_{dd} at the beginning of latch-up. Consequently, a longer delay time is needed under higher supply voltage.

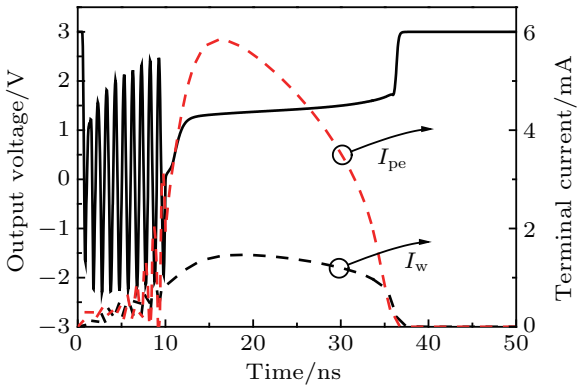


Fig. 13. (color online) Terminal current characteristics of PMOS and output voltage response.

However, the diffusion current is unable to form an adequate voltage drop in n-well to switch the PNP transistor if no sufficient excess carriers are injected as indicated by the analysis in Subsection 3.1, and the output returns to normal level after the excess carriers have flowed out of the device in the form of diffusion current. The time durations spent by this process are similar since diffusion current is only relevant to density gradient rather than supply voltage, and for this reason, delay times have similar values when the HPM power injected is relatively small.

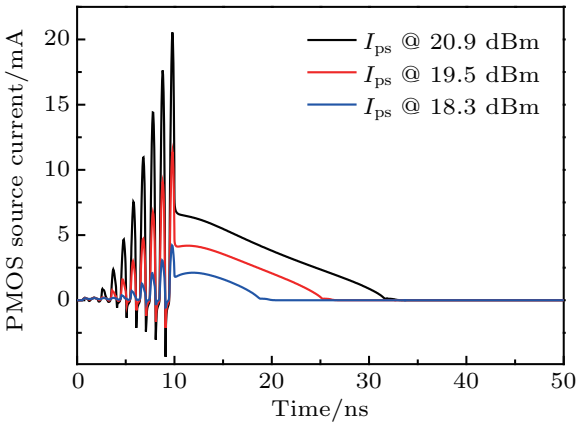


Fig. 14. (color online) Variations of PMOS source current with time under different power levels. The supply voltage is specified to be 1.8 V.

Furthermore, a higher injection power level leads to a longer delay time under the same supply voltage as figure 12 reveals. Figure 14 shows the currents of PMOS source terminal for different HPM power levels under the same supply voltage of 1.8 V. Obviously PMOS source current begins to decease after microwave has been removed and it can be inferred that the positive feedback has failed before 10 ns. The n-well diffusion current is larger due to higher injection power level and higher density of excess carriers at depletion layer border of collector side, hence a longer delay time is needed. In addition, the change of supply voltage is principally reflected in collector region rather than in substrate, and the accumulation of excess carriers in substrate is hardly related to supply voltage. Consequently, the supply voltage has little influence on

upset power threshold, which is consistent with experimental result.[5]

Actually in practice, a small delay time may not be detected in the circuit under the action of parasitic capacitance and specific operating frequency, hence it is feasible that insusceptibility can be obtained under a lower supply voltage at the expense of degradation in circuit performance.

4. Conclusions

The latch-up phenomenon and mechanism induced by high power microwave along with duty cycle, PRF, well depth dependence, supply voltage dependence are discussed in detail on the basis of constructed CMOS inverter model. The simulated result indicates that the density of excess carriers across PN junction between substrate and well is critical in HPM-induced latch-up to the formation of sufficient diffusion current in n-well. An analytical relationship between duty cycle and average $P_{\rm ave}$ is proposed, demonstrating that the shorter width pulsed wave is more efficient in upsetting inverter. Further, the upset threshold power begins to decrease when pulse repetitive frequency exceeds a certain value due to the accumulation of excess carriers. The increase of well depth weakens the accumulation of excess carriers and the resulting latch-up, due to the enhanced drift effect from substrate to well. Moreover, the reported experimental self-recovery phenomenon is elaborated and comes out a positive correlation between delay time and supply voltage when injected power exceeds a certain value, and a higher power level leads to a longer delay time. Moreover, the upset threshold is proved to be hardly dependent on supply voltage, which is consistent with experimental conclusion.

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