Novel high-K with low specific on-resistance high voltage lateral double-diffused MOSFET*

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A novel voltage-withstand substrate with high-K (HK, $k > 3.9$, k is the relative permittivity) dielectric and low specific on-resistance ($R_{on,sp}$) bulk-silicon, high-voltage LDMOS (HKLR LDMOS)is proposed in this paper. The high-K dielectric and highly doped interface N^+-layer are made in bulk silicon to reduce the surface field drift region. The high-K dielectric can fully assist in depleting the drift region to increase the drift doping concentration (N_d) and reshape the electric field distribution. The highly doped N^+-layer under the high-K dielectric acts as a low resistance path to reduce the $R_{on,sp}$. The new device with the high breakdown voltage (BV), the low $R_{on,sp}$, and the excellent figure of merit (FOM = $BV^2/R_{on,sp}$) is obtained. The BV of HKLR LDMOS is 534 V, $R_{on,sp}$ is 70.6 mΩ·cm^2, and FOM is 4.039 MW·cm^{-2}.

Keywords: LDMOS, high-K dielectric, highly doped N^+-layer, high voltage, specific on-resistance

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1. Introduction

The lateral double-diffused MOSFET (LDMOS) has been widely used in the power IC because of its compatibility with the standard CMOS process. But the conventional LDMOS has high $R_{on,sp}$ and low BV. So the reduced surface field (RESURF) technique is often used to modulate and optimize the electric field at the surface of the drift region of the conventional LDMOS to improve BV. RESURF technique was discovered by Appels *et al.* in the late 1970s.[1] The RESURF technique has been successfully applied to several high-voltage devices such as diodes and LDMOSs, which is one of the most applied methods of designing a high-voltage power device with low $R_{on,sp}$. The RESURF technique provides the ability to form a high-voltage lateral device through using an inherently low-voltage IC technology.[2–5] But the trade-off between BV and $R_{on,sp}$ still exists in the RESURF device.[6] The high-K dielectric has been introduced in the lateral and the vertical devices to realize a high BV because of its strong assisted depletion effect. Moreover, the optimal N_d is increased and a great reduction of $R_{on,sp}$ can be obtained.[7–14] In this paper, we propose a novel high-K low specific on-resistance structure. The device not only exhibits a higher BV and a lower $R_{on,sp}$, but also has a better figure of merit (FOM).

2. Device structure and mechanism

The HKLR LDMOS and its physical mechanism are shown in Fig. 1. The value of high-K dielectric is K. N_d and N_{n+} are the concentrations of the drift region and highly doped interface N^+-layer, respectively. L_d is the length of the drift region. t_K, t_g, t_n, t_s, and t_{sub} are the thickness values of high-K dielectric layer, trench gate, highly doped interface N^+-layer, top silicon layer, and substrate layer, respectively.

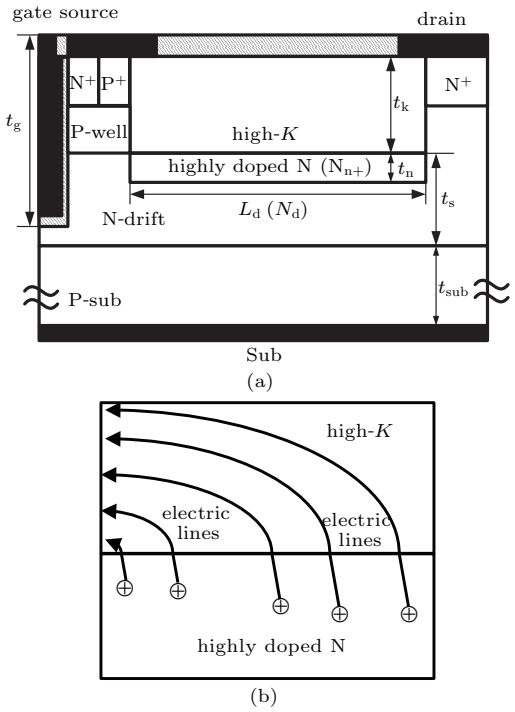


Fig. 1. (a) Structure and (b) mechanism of the HKLR LDMOS. The structure parameters for the HKLR LDMOS are shown in Table 1.

Figure 1(a) shows the high-K dielectric and highly doped interface N^+-layer made in bulk silicon of single RESURF

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drift region. The high-K dielectric, highly doped interface N^+-layer, and bulk silicon substrate form the sustain voltage layer of HKLR LDMOS. The high-K assists in depleting the N^+-layer and the drift region. The highly doped N^+-layer affords a low on-resistance path to reduce $R_{on,sp}$. The HKLR LDMOS structure reshapes the electric field distribution and enhances RESURF effect. The electric field distribution of the HKLR LDMOS is optimized by the HK dielectric, from which the enhanced RESURF effect realizes both high BV and low $R_{on,sp}$, simultaneously. Figure 1(b) shows the work mechanism of the HKLR LDMOS. The high-K and low specific on-resistance structure makes the field lines flow horizontally. The highly doped interface N^+-layer shortens the ionization integral path. Reduced ionization integral path can increase the bulk electric field, which converts the additional electric field into the drift doping concentration. The HKLR LDMOS structure can sustain a high BV in off-state and the silicon layer of the HKLR LDMOS can achieve low on-resistance in the on-state.

Table 1. Device parameters used in the simulation.

Parameter	Value
Length of n^- drift region, L_d/μm	10–120
Thickness of high-K, t_K/μm	2–5
Thickness of highly doped interface N^+-layer, t_n/μm	0.5
Thickness of n^- silicon, t_s/μm	1–10
Thickness of p^- substrate, t_{sub}/μm	80
Concentration of n^- drift region, N_d/cm^{-3}	optimized
Concentration of p^- substrate, N_{sub}/cm^{-3}	1×10^{14}–8×10^{14}
Concentration of highly doped interface N^+-layer, N_{n+}/cm^{-3}	1×10^{16}–5×10^{16}
Coefficient K, K	10–1400

3. Results and discussion

Figure 2 shows the distributions of equipotential contours at breakdown for the HKLR LDMOS and the conventional LDMOS. The conventional LDMOS has a vertical trench gate single RESURF structure with the cell pitch 40 μm. Equipotential contours of the HKLR LDMOS are dense. However, the conventional LDMOS has extremely sparse equipotential contour distribution in the bulk. The BV of the HKLR LDMOS increases from 447 V of the conventional structure to 534 V. High-K dielectric auxiliary depletes the interface highly doped N^+-layer and N-type drift region to improve the doping concentrations of the two regions, which reduces the $R_{on,sp}$. High-K dielectric modulates the body electric field and enhances the vertical electric field, which improves the BV. In the N^+/N drift region, the high concentration of the N^+ region forms a low resistance current path, which reduces the $R_{on,sp}$ in the on-state and the low concentration N region improves the breakdown voltage in the off-state. High-K dielectric and low resistance path realize low $R_{on,sp}$ and high voltage, whose performance is better than that of the conventional single RESURF structure.

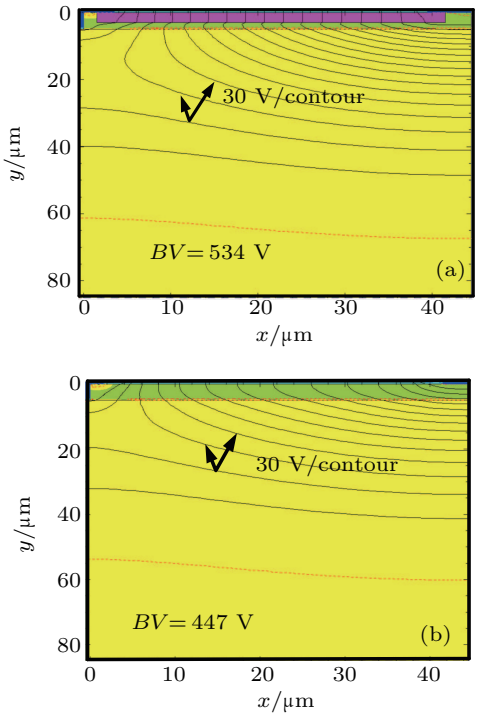


Fig. 2. (color online) Equipotential contours at breakdown voltage for (a) HKLR LDMOS and (b) the conventional LDMOS.

The FOMs of HKLR, HK dielectric, and N^- drift region (without highly doped N^+-layer) and the conventional LDMOSs each are a function of N_d as shown in Fig. 3.

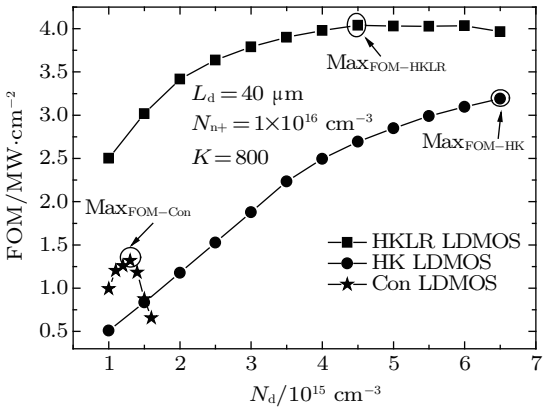


Fig. 3. Figures of merit (FOM = $BV^2/R_{on,sp}$) for HKLR, HK, and the conventional (Con) LDMOSs.

The FOM of the HKLR LDMOS first increases and then saturates with the increase of N_d. The maximum FOM is 4.039 MW·cm^{-2} with $R_{on,sp}$ of 70.6 mΩ·cm^2 when the N_d is 4.5×10^{15} cm^{-3} and the N_{n+} is 1×10^{16} cm^{-3}. The FOM of the HK (HK dielectric without highly doped N^+-layer) LDMOS first increases and then the drift region is non-depleted with the increase of N_d. The maximum FOM is 3.191 MW·cm^{-2} with $R_{on,sp}$ of 90.7 mΩ·cm^2 when the

N_d is 6.5×10^{15} cm^{-3}. However, the N_d of the conventional LDMOS cannot be depleted when the N_d is more than 1.6×10^{15} cm^{-3}. The FOMs of the conventional LDMOS are limited to a narrow range of N_d. The maximum FOM is 1.319 MW·cm^{-2} and its $R_{on,sp}$ is 151.4 mΩ·cm^2 when the N_d is 1.3×10^{15}cm^{-3} for the conventional LDMOS. The process tolerance performance of the new structure is more superior to that of the conventional LDMOS. The largest FOM serves as the standard for the three devices to be optimized, not breakdown voltage.

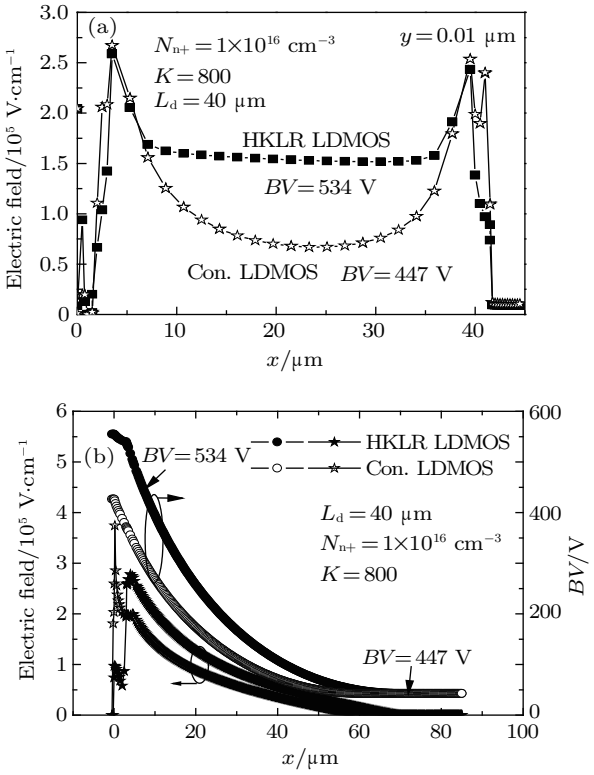


Fig. 4. (a) Surface, (b) vertical electric fields and potential contours for the HKLR LDMOS and the conventional LDMOS.

Figure 4 shows the surface, vertical electric fields and potential contours for the HKLR LDMOS and the conventional LDNOS. Horizontal electric field distributions along the surface ($y = 0.01$ μm) of the two structures are given in Fig. 4(a). It can be seen from Fig. 4(a) that the HKLR LDMOS modulates the distribution of the electric field in the drift region, and the electric field in the middle of the drift region is raised, which will lead to a uniform lateral electric field for the HKLR LDMOS. Generally, the electric field under the drain in the off-state is relatively low for the the conventional LDMOS as shown in Fig. 4(a), and therefore, the electric field peak at the source-drain for the HKLR LDMOS can be controlled to be less than the critical electric field ($E_{s,c}$) to avoid a premature breakdown by controlling K. Moreover, the assistant depletion effect of the high K results in a higher impurity doping for the drift region, and the optimal N_d at the maximum BV for the HKLR LDMOS is larger than that of the conventional LDMOS. The simulation results show that the surface electric field of the HKLR LDMOS is increased from about 0.75×10^5 V/cm of the conventional LDMOS to about 1.75×10^5 V/cm in the middle of the drift region. The additional lateral electric field ΔE_x of the new device is about 1×10^5 V/cm. Figure 4(b) shows the vertical electric field and potential distributions at breakdown under the drain. It can be seen that vertical electric field of the HKLR LDMOS increases from about 2×10^5 V/cm of the conventional LDMOS to 3×10^5 V/cm. The HKLR LDMOS has a BV of 534 V higher than 447 V of the conventional LDMOS.

BV and $R_{on,sp}$ are functions of N_d for both the HKLR LDMOS and the conventional LDMOSs as shown in Fig. 5(a). As N_d increases, BV of the HKLR LDMOS first slowly decreases and then cannot be fully depleted when N_d is more than 6.5×10^{15} cm^{-3}. The BV of 534 V is obtained with $R_{on,sp} = 70.6$ mΩ·cm^2, $N_d = 4.5 \times 10^{15}$ cm^{-3}, and $N_{n+} = 1 \times 10^{16}$ cm^{-3}. The $R_{on,sp}$ of the HKLR LDMOS first rapidly decreases with the increase of N_d and then cannot be fully depleted when N_d is more than 6.5×10^{15} cm^{-3}. However, the drift region of the conventional LDMOS cannot be depleted only when N_d is more than 1.6×10^{15} cm^{-3}. Therefore, not only the BV but also the $R_{on,sp}$ of the conventional single RESURF LDMOS is limited to a narrow range by N_d. The maximum BV is 447 V and the $R_{on,sp}$ is 151.4 mΩ· cm^2 for the conventional LDMOS. The maximum FOMs are 4.039 MW·cm^{-2} and 1.319 MW·cm^{-2} for the HKLR LDMOS and the conventional LDMOS, respectively. Figure 5(b) shows BV and $R_{on,sp}$ as functions of L_d for both devices. As L_d increases, BV and $R_{on,sp}$ of the HKLR LDMOS increase. At the same time, the BV and $R_{on,sp}$ of the conventional LDMOS also increase with the increase of L_d. However, the increase of the BV with the increase of L_d for the HKLR LDMOS is quicker than that of the conventional LDMOS. Meanwhile, the increase of the $R_{on,sp}$ with the increase of L_d for the HKLR LDMOS is slower than that of the conventional LDMOS. The process tolerance performance of the new structure is more superior to that of the conventional single RESURF device.

Figure 6 shows that the BV and $R_{on,sp}$ are also functions of K and N_{n+} for the HKLR LDMOS. Figure 6(a) shows the influences of K value on BV and $R_{on,sp}$. With the high K value, almost all of the N$^+$-layers are depleted by the high-K dielectric, which leads to a similar optimized electric field of the HKLR LDMOS. As a result, the constant BV is observed with K being over 200, which indicates the optimal region of the new device. Figure 6(b) shows that the BV and $R_{on,sp}$ first reduce and then undeplete when N_{n+} is more than 5×10^{16} cm^{-3}, which has a large range from 1×10^{16} cm^{-3} to

5×10^{16} cm^{-3} for N_{n+}, too. The new structure shows excellent process tolerance characteristics at geometric parameters and all kinds of concentrations, respectively.

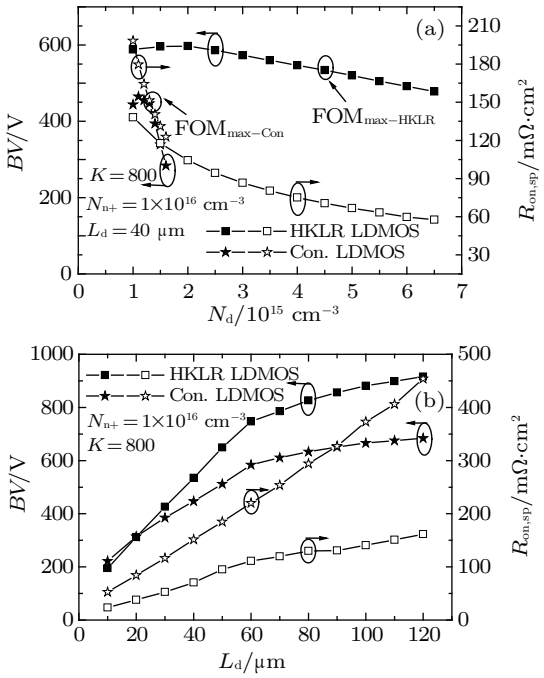


Fig. 5. $R_{on,sp}$ versus BV for the HKLR LDMOS and the conventional LDMOS. (a) BV and $R_{on,sp}$ are functions of N_d, (b) BV and $R_{on,sp}$ are functions of L_d.

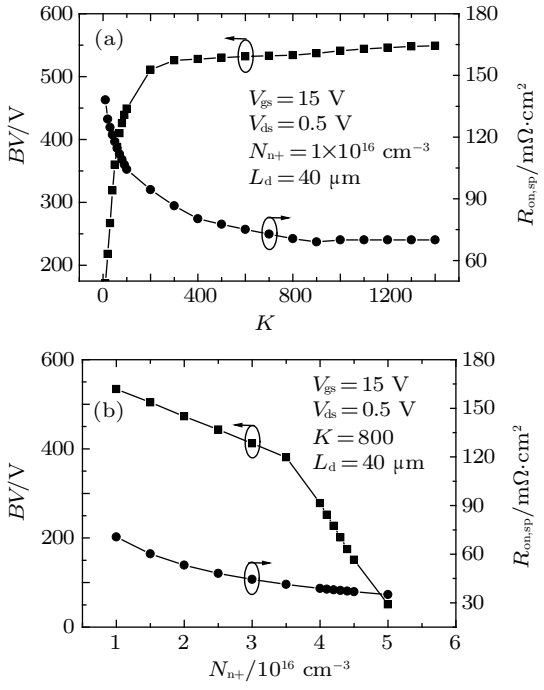


Fig. 6. $R_{on,sp}$, BV as functions of K and N_{n+} for the HKLR LDMOS. (a) $R_{on,sp}$, BV as functions of K for the HKLR LDMOS, (b) $R_{on,sp}$, BV as functions of the N_{n+} for the HKLR LDMOS.

The plots of BV versus the thickness of high-K dielectric layer (t_k) and top silicon layer (t_s) for the HKLR LDMOS are shown in Fig. 7(a). The BVs of the HKLR LDMOS first rapidly reduce and then slowly increase with the increase of t_s when the value of t_k is increased. So high-K dielectric is suitable for wide and shallow structures. The trench gate in the device has great influence on the $R_{on,sp}$.[15–17] Figure 7(b) shows the influences of length of trench gate (t_g) on BV and $R_{on,sp}$. The trench gate and the N drift region form an MIS capacitor. The BV reduces with the length of trench gate increasing, because the electric field of the drift region is easily concentrated in the corner of the trench oxide in off-state. Meanwhile, the electrons are accumulated at the interface between the drift region and the trench oxide layer by the MIS capacitor, which increases the concentration of the drift region to provide a low resistance path and realize low on-resistance in on-state. The length of the trench gate (t_g) is determined to be 5 μm by three factors of BV, $R_{on,sp}$, and FOM.

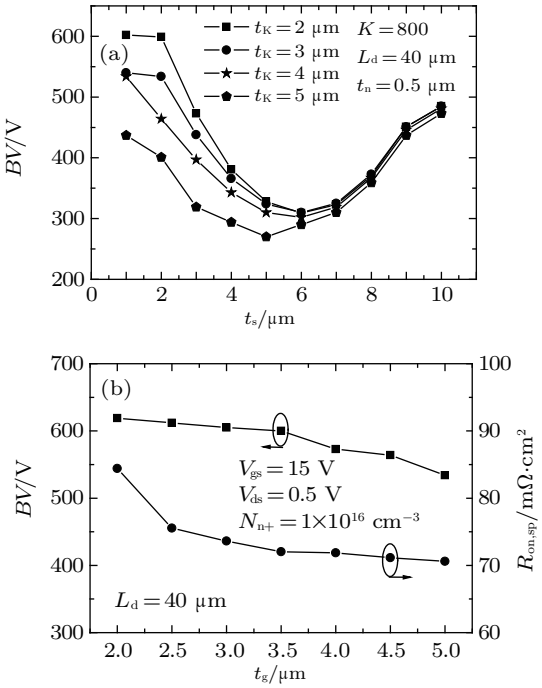


Fig. 7. (a) BVs as functions of t_k and t_s for HKLR LDMOS. (b) BV, $R_{on,sp}$ as functions of t_g for the HKLR LDMOS.

4. Conclusions

A novel structure with high-K dielectric and low specific on-resistance is proposed to develop high-voltage LDMOS. A high-K dielectric region is introduced into the drift region to raise the drift doping concentration (N_d) and reduce the specific on-resistance ($R_{on,sp}$). The simulation using TCAD tool (Medici) shows that the proposed device enables a 19.5% improvement in breakdown voltage, 53.4% reduction in specific on-resistance, and three times increase in FOM in comparison with that of the conventional single RESURF LDMOS.

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