Positive gate bias stress-induced hump-effect in elevated-metal metal–oxide thin film transistors*

Dong-Yu Qi(齐栋宇), Dong-Li Zhang(张冬利), and Ming-Xiang Wang(王明湘)†

Department of Microelectronics, Soochow University, Suzhou 215006, *China*

(Received 11 July 2017; revised manuscript received 22 August 2017; published online 20 October 2017)

Under the action of a positive gate bias stress, a hump in the subthreshold region of the transfer characteristic is observed for the amorphous indium–gallium–zinc oxide thin film transistor, which adopts an elevated-metal metal–oxide structure. As stress time goes by, both the on-state current and the hump shift towards the negative gate-voltage direction. The humps occur at almost the same current levels for devices with different channel widths, which is attributed to the parasitic transistors located at the channel width edges. Therefore, we propose that the positive charges trapped at the back-channel interface cause the negative shift, and the origin of the hump is considered as being due to more positive charges trapped at the edges along the channel width direction. On the other hand, the hump-effect becomes more significant in a short channel device ($L = 2$ μm). It is proposed that the diffusion of oxygen vacancies takes place from the high concentration source/drain region to the intrinsic channel region.

Keywords: amorphous indium–gallium–zinc oxide, thin film transistors, positive bias stress, hump

PACS: 81.05.Gc, 81.05.Ea, 85.30.Tv **DOI:** 10.1088/1674-1056/26/12/128101

1. Introduction

Metal–oxide–semiconductor thin film transistors (TFTs), considered as the substitutions of amorphous silicon (a-Si) TFTs, are widely used as pixel switching elements in high resolution and large area flat-panel displays.[1] Amorphous indium–gallium–zinc oxide (a-IGZO) TFT, first reported by Nomura *et al*. in 2004,[2] exhibits some superior properties, such as higher field-effect mobility ($\mu_{\rm FET}$) than that of a-Si TFT, low off-state current ($I_{\rm off}$), low sub-threshold swing (SS), high on/off-current ratio, good uniformity, low temperature processing, and high transparency in the visible light range.[1–9]

Recently, a new TFT structure named elevated-metal metal–oxide (EMMO) TFT (as shown in Fig. 1) was developed. The EMMO TFT is superior to the conventional back-channel-etch (BCE) or etch-stop (ES) TFT.[10] The BCE TFT is criticized for channel damage during patterning the source/drain (S/D) electrodes.[11] In order to protect the channel, an ES layer is introduced. However, the ES structure carries with it an extra mask.[12] The EMMO TFT tactfully makes a tradeoff by elevating the S/D electrodes onto the passivation, and the passivation layer plays the role of an ES layer. Next, a heat-treatment in oxygen induces n^+ S/D regions, which cancels the requirement for an extension of the gate electrode to underlap the S/D electrode contacts.[10] Therefore, the device footprint and parasitic capacitance are reduced. The superiority of the EMMO structure is obvious. However, a hump in the subthreshold region of the transfer characteristic is observed when the EMMO TFT is under the action of large positive gate bias stress (PBS). The hump-effect was already reported in low temperature polycrystalline silicon (LTPS)[13,14] and MO[15,16] TFTs. As reported, the hump-effect is mainly attributed to the edge effect[13–15] or back-channel conduction.[16] In this paper, we investigate the origin of this PBS induced hump-effect by using TFTs with a fixed channel length and different channel widths. It is found that the humps occur almost at the same current levels, therefore we exclude the back-channel conduction effect. We also investigate the relationship between the hump-effect and channel length, and the result shows that the hump-effect becomes more significant in a short channel device ($L = 2$ μm). In addition, the hump-effect becomes more severe under higher gate bias stress ($V_{\rm g}$ stress) and stress temperature.

2. Experiment

The EMMO TFT used in this paper employs a bottom gate inverted staggered structure. The indium–tin oxide (ITO) is first sputtered and patterned into a gate electrode on an oxidized silicon wafer. Next, a 100-nm-thick silicon oxide (SiO_x) gate insulator layer is deposited at a temperature of 420 °C by low pressure chemical vapor deposition (LPCVD). A 30-nm active layer of In_2O_3:Ga_2O_3:Zn = 1:1:1 is deposited by RF magnetron sputtering in a gas mixture of 10% oxygen and 90% argon with the total working pressure being 3 mTorr

*Project supported by the Science and Technology Program of Suzhou City, China (Grant No. SYG201538) and the National Natural Science Foundation of China (Grant No. 61574096).

†Corresponding author. E-mail: mingxiang_wang@suda.edu.cn

© 2017 Chinese Physical Society and IOP Publishing Ltd

(1 Torr = 1.33322×10^2 Pa). After the a-IGZO active island is patterned by using the dilute hydrofluoric acid solution, a 300-nm passivation layer, deposited by LPCVD, is then covered. The contact holes are formed by using the plasma enhanced etching method, and a molybdenum/aluminum (Mo/Al) bi-layer is sputtered and patterned, with a 4-μm overlap of the gate electrode to form the S/D electrodes (Fig. 1). Then an annealing treatment is carried out under O^2 atmosphere at 400 °C for 2 hours to form the conductive n^+ S/D region and the highly resistive intrinsic channel region, which ensures that the EMMO TFTs can work properly.[17]

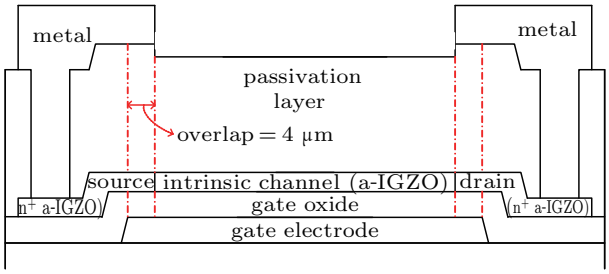


Fig. 1. (color online) Schematic cross-section of an EMMO TFT.

The TFT transfer characteristic measurement and PBS application are performed by using an Agilent 4156C semiconductor parameter analyzer. Some electrical parameters are obtained from the initial transfer characteristics measured at a drain voltage (V_d) of 1 V. The threshold voltage (V_{TH}) is about 0.4 V extracted by using the linear extrapolation method. The *SS* is about 120 mV/dec and μ_{FET} is about 12 cm^2/V·s, determined by the maximum $\partial I_d/\partial V_g$ and $\partial(\log I_d)/\partial V_g$ respectively. In order to monitor the degradation, we measure the transfer characteristics after each stress test. A fresh TFT is used after each stress test series.

3. Results and discussion

Figure 2 shows the typical evolutions of transfer characteristics of an EMMO TFT ($W/L = 50/12$ μm) under V_g stress of +20 V and at 50 °C. Under the action of PBS, a hump appears in the subthreshold region of the transfer characteristics, and the hump becomes more apparent as the stress time goes by. The parallel shift of the on-state current occurs while the variation of *SS* and μ_{FET} is negligible (Fig. 2), which indicates that the shift is induced by the charge trapping without generating any new defect states.[16,18]

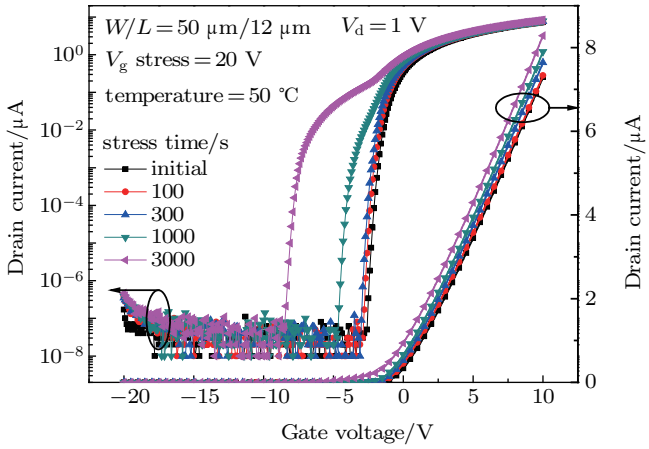


Fig. 2. (color online) Time evolutions of transfer characteristics, measured at V_d of 1 V, of an EMMO TFT with $W/L = 50/12$ μm subjected to PBS with V_g stress of 20 V at 50 °C. The transfer curves are plotted in both linear and logarithmic scales.

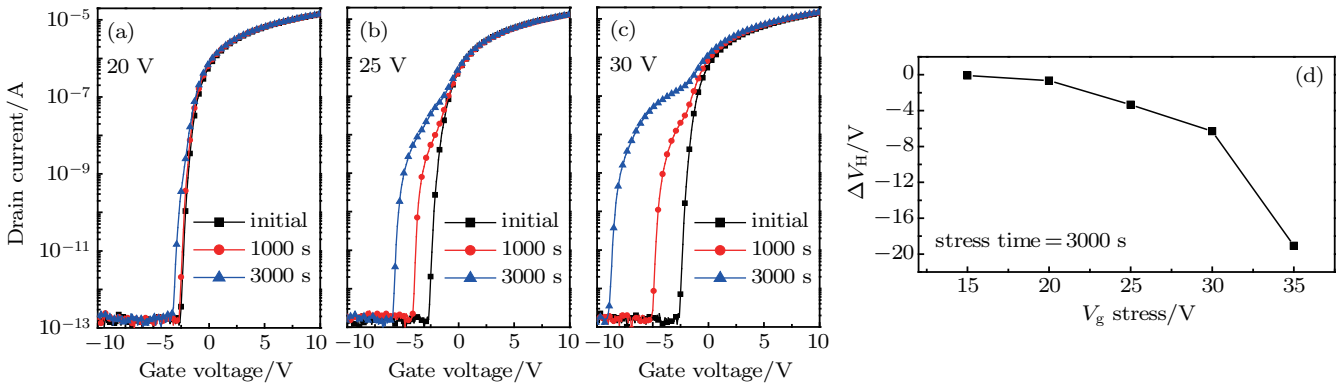


Fig. 3. (color online) Time evolutions of transfer characteristics under PBS with values of V_g stress of (a) 20 V, (b) 25 V, (c) 30 V at 20 °C. The TFTs have geometry $W/L = 100/12$ μm. (d) Voltage shift of V_H versus gate bias stress.

Figure 3 shows the time evolutions of transfer characteristics under PBS under different V_g stresses at 20 °C. The hump-effect is almost negligible against V_g stress ($\leq$ 20 V) within 3000 s. However, as V_g stress becomes larger than 20 V, the hump in the subthreshold region is clearly observed. A reference voltage for the hump (V_H) is defined as the gate voltage at a drain current (I_d) of 10^{-11} A for V_d of 1 V. It is clear that the shift of V_H (ΔV_H) increases with V_g stress rising (Fig. 3(d)), indicating that the hump-effect is gate voltage induced. In Fig. 4, the time dependence of $-\Delta V_H$ under PBS with the same V_g stress but at different temperatures is plotted in log-log scale. The $-\Delta V_H$ increases with stress time, following a power-law, and the time exponent *n* increases from 0.48 to 0.75 with stress temperature varying from 30 °C to 70 °C.

The hump-effect is enhanced at higher stress temperature. It is found that the hump-effect is activated electrically and thermally.

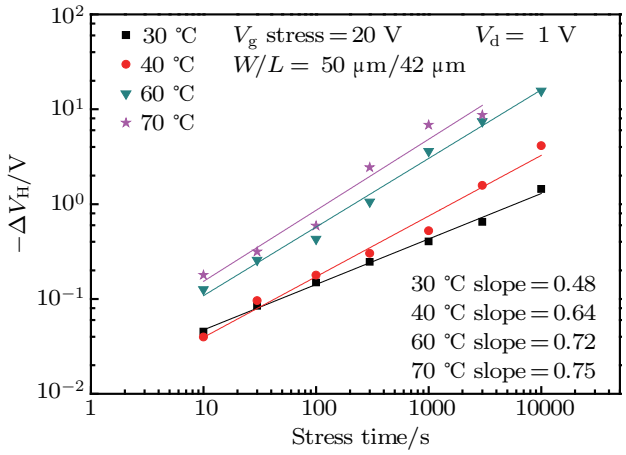


Fig. 4. (color online) Plots of $-\Delta V_H$ versus stress time in log–log scales under PBS at different temperatures. The degradations of $-\Delta V_H$ follows the time-dependent power-law with the exponent n ranging from about 0.83 to 1.03.

As reported, the hump-effect could be due to the existence of more than one logical transistor, which are connected in parallel in a single TFT device. There are two main ways to form these parasitic transistors. One is the effect of back-channel conduction,[16] which is related to bulk effects, and the other is attributed to the edge effects.[13–15] In order to figure out the origin of the PBS induced hump in EMMO TFTs, we carry out the experiments by using the devices with a fixed channel length and various channel widths.

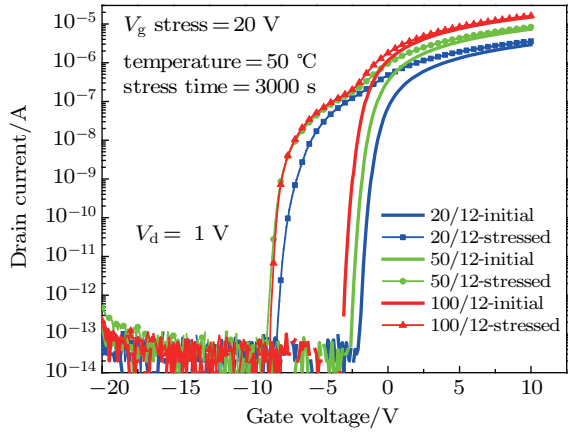


Fig. 5. (color online) Transfer characteristics of the EMMO TFTs with channel width ranging from 20 to 100 μm under the condition without and with the action of PBS.

Figure 5 shows the transfer characteristic curves of devices with various channel widths, under the condition without and with exerting the PBS. Obviously, the humps occur almost at the same current levels and ΔV_H is independent of W, indicating that the hump is related to the edge effect[13,15] rather than the conduction in the back-channel, because the magnitude of the hump varies proportionally with channel width in the case of the back-channel conduction effect.[19] It is reported in top gate LTPS TFTs that the hump is caused by the edge effect of the gate insulator (GI). Owing to the thinner GI at the edge sides, higher electric field at the edges will contribute to trapping more charges and thus a hump appears.[13] The thickness of the gate dielectric layer is ideally uniform in the bottom gate structure. Whereas the a-IGZO island is patterned by using the wet etching method, which is isotropic, resulting in the edge effect of the a-IGZO active layer. The parasitic transistor is located at the edges along the channel width direction (Fig. 6(a)). Theoretically, they are independent of channel width.

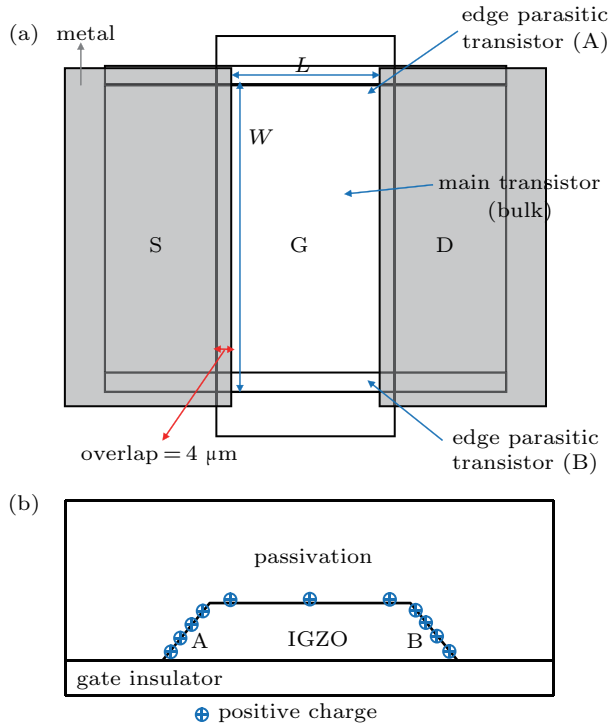


Fig. 6. (color online) (a) Plane view of the device composed of a main transistor and two edge parasitic transistors. (b) Positive charges trapping at the back-channel interface and/or into the passivation induce the transfer characteristic to negatively shift, while more positive charges trapped at the edges lead to the formation of the hump.

Generally, the transfer characteristics of a-IGZO TFT shift positively under the action of PBS, which is due to the negative charges trapping at the interface of a-IGZO/GI and/or into the GI.[12] However, the contrary results are observed in this study. Therefore, we propose that the dominant mechanism be due to the positive charges, which are repelled to the back-channel interface by a vertical electric field, trapping at the interface of a-IGZO/passivation and/or into the passivation. The accumulation of positive charges at the back-channel interface will reduce the channel/source and channel/drain potential barrier, which causes the drain current to increase, i.e., the transfer characteristics shift negatively. These aforementioned positive charges can be ionized oxygen vacancies (V_O^{2+}) or zinc.[20–22] The edges are not covered by photoresist during the etching of a-IGZO island. Therefore, the quality of

back-channel interface at the edges is much poorer than that of the bulk. In other words, the number of defect states is much higher at the edges, and these states will contribute to the trapping of positive charges, leading to the trapping of more repelled positive charges at the back-channel interface of the edges (Fig. 6(b)). More trapped positive charges at the edges causes more negative shift of the parasitic transistor than the main transistor, i.e., the parasitic transistor turns on earlier. In the subthreshold region, the parasitic transistors are dominant, and the main transistor controls the on-state region, thus the hump appears.

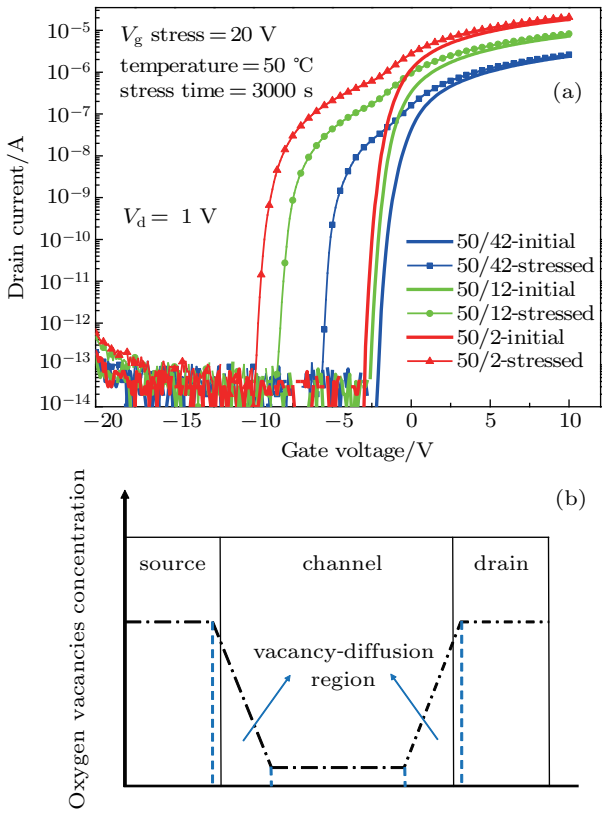


Fig. 7. (color online) (a) Transfer characteristics of the EMMO TFTs with channel lengths ranging from 2 μm to 42 μm under the condition without and with the action of PBS. (b) Oxygen vacancy diffusion model: oxygen vacancies diffuse from the high concentration S/D regions into the intrinsic channel region, forming a vacancy-diffusion region.

Figure 7(a) shows the initial and stressed transfer characteristics of devices with various channel lengths. It is interesting to notice that the hump is strongly dependent on channel length. The hump occurs at a higher current level and larger ΔV_H is observed in the subthreshold region in the device with shorter channel ($L = 2$ μm) compared with those with the longer channel devices. However, simple L reduction of edge transistor can only lead to a higher current rather than a larger ΔV_H. Therefore, a diffusion model is proposed to explain the ΔV_H dependence on the channel length. The concentration of oxygen vacancies (V_O) in the n^+ S/D region is much higher than that in the intrinsic channel region.[10,17] This concentration difference makes V_O diffuse from the S/D region into the intrinsic channel region, which will build vacancy concentration gradients at the channel/source and channel/drain junctions to form a vacancy-diffusion region (Fig. 7(b)). Because the diffusion mainly occurs at the junction, as the channel length decreases, the influence of the vacancy-diffusion region will be more significant, which means that more positive charges (produced by the ionization of V_O) in a unit area will be trapped under the action of PBS, leading to a larger ΔV_H. As a result, the hump effect is more significant in short channel devices than in long channel devices.

4. Conclusion and perspectives

In summary, the stress-induced hump in EMMO TFT is caused by the edge effect of a-IGZO layer, rather than the back channel conduction, which is confirmed by the independence of the hump size of channel width. In other words, the fabrication process to profile the active area should be improved. In EMMO TFT, the n^+ S/D region will affect the intrinsic channel region by oxygen vacancy diffusion, and the influence is more significant in the short channel device ($L = 2$ μm).

References

[1] Kamiya T, Nomura K and Hosono H 2010 *Sci. Technol. Adv. Mater.* **11** 044305
[2] Nomura K, Ohta H, Takagi A, Kamiya T, Hirano M and Hosono H 2004 *Nature* **432** 488
[3] Li S S, Liang C X, Wang X X, Li Y H, Song S M, Xin Y Q and Yang T L 2013 *Acta Phys. Sin.* **62** 077302 (in Chinese)
[4] Ning H L, Hu S B, Zhu F, Yao R H, Xu M, Zou J H, Tao H, Xu R X, Xu H, Wang L, Lan L F and Peng J B 2015 *Acta Phys. Sin.* **64** 126103 (in Chinese)
[5] Tang L F, Yu G, Lu H, Wu C F, Qian H M, Zhou D, Zhang R, Zheng Y D and Huang X M 2015 *Chin. Phys. B* **24** 088504
[6] Qian H M, Yu G, Lu H, Wu C F, Tang L F, Zhou D, Ren F F, Zhang R, Zheng Y L and Huang X M 2015 *Chin. Phys. B* **24** 077307
[7] Huang X M, Wu C F, Lu H, Xu Q Y, Zhang R and Zheng Y D 2012 *Chin. Phys. Lett.* **29** 067302
[8] Yabuta H, Sano M, Abe K and Aiba T 2006 *Appl. Phys. Lett.* **89** 112123
[9] Kamiya T, Nomura K and Hosono H 2009 *J. Disp. Technol.* **5** 273
[10] Lu L, Li J, Zhou Q F, Kwok H S and Man W 2016 *IEEE Electron Dev. Lett.* **37** 728
[11] Yamazaki S, Hirohashi T, Takahashi M, Adachi S, Tsubuku M, Koezuka J, Okazaki K, Kanzaki Y, Matsukizono H, Kaneko S, Mori S and Matsuo T 2014 *J. Soc. Inf. Disp.* **22** 55
[12] Lan L L, Zhang P and Peng J B 2016 *Acta Phys. Sin.* **65** 128504 (in Chinese)
[13] Huang C F, Peng C Y, Yang Y J, Sun H C, Chang H C, Kuo P S, Chang H L, Liu C Z and Liu C W 2008 *IEEE Electron Dev. Lett.* **29** 1332
[14] Valletta A, Gaucci P, Mariucci L, Fortunato G and Templier F 2008 *J. Appl. Phys.* **104** 124511
[15] Mativenga M, Seok M and Jin J 2011 *Appl. Phys. Lett.* **99** 122107
[16] Tsai Y S and Chen J Z 2012 *IEEE Trans. Electron Dev.* **59** 151
[17] Lu L and Man W 2015 *IEEE Trans. Electron Dev.* **62** 574
[18] Chen T C, Chang T C, Tsai C T, Hsieh T Y, Chen S C, Lin C S, Hung M C, Tu C H, Chang J J and Chen P L 2010 *Appl. Phys. Lett.* **97** 112104
[19] Mativenga M, Min H C, Jin J, Mruthyunjaya R, Tredwell T J, Mozdy E and Williams C K 2011 *IEEE Trans. Electron Dev.* **58** 2440
[20] Lany S and Zunger A 2005 *Phys. Rev. B* **72** 035215
[21] Clark S J, Robertson J, Lany S and Zunger A 2010 *Phys. Rev. B* **81** 115311
[22] Lu L and Man W 2014 *IEEE Trans. Electron Dev.* **61** 1077