Capacitance extraction method for a gate-induced quantum dot in silicon nanowire metal–oxide–semiconductor field-effect transistors*

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An improved method of extracting the coupling capacitances of quantum dot structure is reported. This method is based on measuring the charge transfer current in the silicon nanowire metal–oxide–semiconductor field-effect transistor (MOSFET), in which the channel closing and opening are controlled by applying alternating-current biases with a half period phase shift to the dual lower gates. The capacitances around the dot, including fringing capacitances and barrier capacitances, are obtained by analyzing the relation between the transfer current and the applied voltage. This technique could be used to extract the capacitance parameters not only from the bulk silicon devices, but also from the silicon-on-insulator (SOI) MOSFETs.

Keywords: nanowire MOSFETs, coupling capacitance, fringing capacitance, quantum dot

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1. Introduction

Recently, electrostatically defined quantum dots have become of increasing interest because of their applications in quantum information processing,[1–3] single-electron logic circuits,[4] high-sensitivity detection,[5,6] quantum dot cellular automata,[7,8] etc. These devices have great advantages, such as stable characteristics, simple device structure, high operating temperature, and high compatibility of their fabrication process with integrated circuits.[9,10] For the operation of these devices, it is important to control the coupling capacitances between the quantum dots and the effective device structures, which are determined by charge configurations in the quantum dots. In the most popular quantum dot structures comprised of nanowire or two-dimensional electron gas, the coupling capacitances can be controlled by gate biases, which can modulate the tunnel barriers around the quantum dots. Thus, extracting capacitances around the quantum dots is a vital aspect for guiding the design of device structure and the analysis of its characteristics.[11–14]

Since the device size becomes so small that it is difficult to directly measure ultra-small capacitances, it is necessary to explore a simple and efficient method of measuring capacitances. By measuring the transfer currents with the gate pulses, Inokawa et al. have presented a simple test structure for extracting capacitances at room temperature.[15] According to their test results of a silicon-on-insulator (SOI) metal–oxide–semiconductor field-effect transistor (MOSFET) structure, they pointed out that the transfer current was not only proportional to the gate pulse frequency, but also linearly dependent on the drain voltage. However, we find experimentally that the transfer current does not linearly depend on the drain voltage for the bulk silicon device. Then, an improved method is presented to extract the capacitances of the test structure, which can be used not only for SOI devices but also for the bulk silicon ones.

The rest of this paper is organized in four sections. In Section 2, the test device structure and the capacitance network are presented. In Section 3, the capacitance extraction method is proposed by analyzing the relation between the transfer current and the voltage of each electrode. In Section 4, the measured results and the extracted capacitance values are provided. Finally, in Section 5 some conclusions are drawn from this work.

2. Device structure and capacitance network

Figure 1(a) shows the cross-sectional view of the fabricated silicon nanowire MOSFET by a 65-nm bulk CMOS process. The two lower polysilicon gates (denoted as LG1 and LG2) cross a narrow silicon nanowire to create potential profiles that act as tunneling barriers for the electron transfer process. The region in the nanowire between the two lower gates forms a charge island (that is, a quantum dot). The two lower MOSFETs and the entire nanowire are covered with an upper polysilicon gate (UG), which serves as an input gate for controlling the potential of the dot and a field plate for inducing an inversion layer extending from the source to the drain. This structure is efficient for shielding electromagnetic disturbance in a single electron transfer or a quantum logic operation due to the screening effect of the UG. The lower gate length L, the channel width W, the gate spacing S, the thickness of UG oxide, and the oxide thickness beneath the LGs are 70, 110, 170,

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640, and 5 nm respectively.

An equivalent circuit with six mutual capacitances is depicted in Fig. 1(b), where C_u, C_{1f}, C_{2f}, C_s, C_d, and C_b are the capacitances between the island and the UG, LG1, LG2, source, drain, and substrate, respectively. The six capacitances can be divided into two groups. One is called 'operable capacitances', including C_u, C_{1f}, and C_{2f}. With the operation of these operable capacitances, the electron number and the potential profile on the dot can be changed conveniently. The other is called 'non-operable capacitances', including C_s, C_d, and C_b. They are usually biased at the fixed voltages in the charge transfer process. Figure 1(c) shows the top-view scanning electron microscope image before the UG formation.

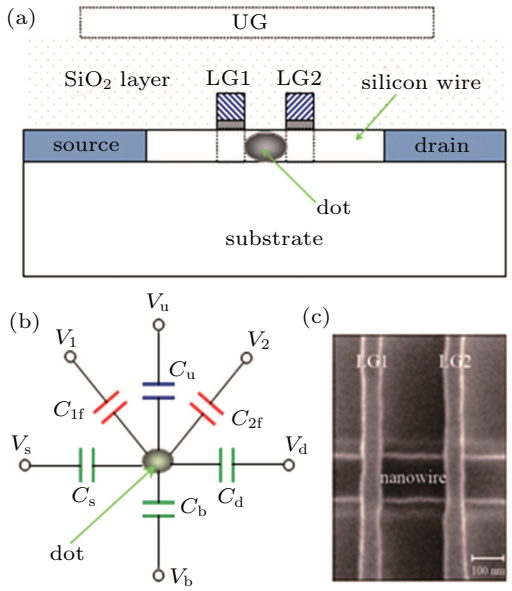


Fig. 1. (color online) (a) Cross-sectional view of the measured device structure, (b)diagram of the capacitance network around the dot, and (c) top-view scanning electron microscope image before UG formation.

The measured drain currents of the charge transfer device with high-frequency clock pulses are obtained by using the Agilent 81110A and 4156C. The pulse sequences for UG, LG1, and LG2 are shown in Fig. 2(a). The high and low bias levels of UG are denoted as V_{uH} and V_{uL} respectively. The threshold voltage for UG MOSFET is extracted as $V_{uth} = -5.41$ V from the measured I_d–V_u curve at the biasing voltages of other terminals $V_1 = 2$ V for LG1, $V_2 = 2$ V for LG2, $V_s = 0$ V for the source, $V_d = 10$ mV for the drain and $V_b = 0$ V for the substrate, respectively.[16] Thus, in all the subsequent measurements, the inequality $V_{uH} \geq V_{uL} > V_{uth} = -5.41$ V must hold in order to keep the nanowire channel in an inversion state. The two quarter period pulses with a half period shift are applied to the lower gates to turn the channel on and off alternatively, and the threshold voltages of the two lower MOSFETs should be between their high and low bias levels ($V_{1H} > V_{1th} > V_{1L}$, $V_{2H} > V_{2th} > V_{2L}$). The pulse frequency varies from 0.1 MHz to 5 MHz while their rise and fall times are kept at 18 ns, and such pulses can be treated approximately as square waves. All the measurements are performed at room temperature.

The charge transfer mode is shown in Fig. 2(b). In step (i), LG1 MOSFET is in an on state while LG2 MOSFET is in an off state, electrons enter into the silicon wire from the source; then the two channels beneath the LG1 and LG2 MOSFETs are closed (see step (ii) in Fig. 2(b)), some of those electrons are confined on the quantum dot (the charge quantity on the dot is denoted as Q_1 in this case); next, LG1 is turned off while LG2 is turned on in step (iii), the electrons can be transferred into the drain from the dot; in step (iv), the channel between the LG1 and LG2 is closed again, and some electrons are confined on the quantum dot (the charge quantity on the dot is denoted asQ_2 in this case). The difference between Q_1 and Q_2, i.e., $\Delta Q = Q_1 - Q_2$, indicates the number of electrons transferred from the source into the drain in one period of the clock pulses.

3. Capacitance extraction method

In the charge transfer mode, there are charges Q_1 (or Q_2) confined on the dot when the voltage of LG1 (or LG2) changes from the high level to the low level (see Fig. 2).

In step (ii) of Fig. 2(b), when the source is grounded, the charge quantity Q_1 is expressed as[15]

$$Q_1 = -C_d V_d - C_u V_{uH} - C_{1f} V_{th1} - C_{2f} V_{2L} - C_b V_{b1}, \quad (1)$$

where V_{1H} is replaced by V_{th1} as LG1 MOSFET is at the above threshold. The V_{th1} equals the original threshold voltage (V_{th10}) in the DC measurement, i.e., $V_{th1} = V_{th10}$, for the potential of the dot is zero since the dot is connected to the source at the previous moment in step (i) of Fig. 2(b).

Similarly, in step (iv) of Fig. 2(b), the charge quantity Q_2 is expressed as[15]

$$\begin{aligned} Q_2 = {} & (C_{1f} + C_{2f} + C_u + C_s + C_b) V_d - C_u V_{uL} \\ & - C_{1f} V_{1L} - C_{2f} V_{th2} - C_b V_{b2}, \end{aligned} \quad (2)$$

where V_{2H} is replaced by V_{th2} when LG2 MOSFET is on the above threshold. However, V_{th2} is raised from the original threshold voltage (V_{th20}) in the DC measurement roughly by V_d, i.e. $V_{th2} = V_{th20} + V_d$, for the potential of the dot is V_d since the dot is connected to the drain at the previous moment in step (iii) of Fig. 2(b).

The transferred charge ΔQ is the difference between Q_1 and Q_2,

$$\begin{aligned} \Delta Q = {} & Q_1 - Q_2 = -(C_T - C_{2f}) V_d - C_u \Delta V_u \\ & - C_{1f} (V_{th10} - V_{1L}) - C_{2f} (V_{2L} - V_{th20}) - C_b \Delta V_b, \end{aligned} \quad (3)$$

where $\Delta V_u = V_{uH} - V_{uL}$, $\Delta V_b = V_{b1} - V_{b2}$, and C_T is the total capacitance of the dot and defined as

$$C_T = C_s + C_d + C_b + C_{1f} + C_{2f} + C_u. \quad (4)$$

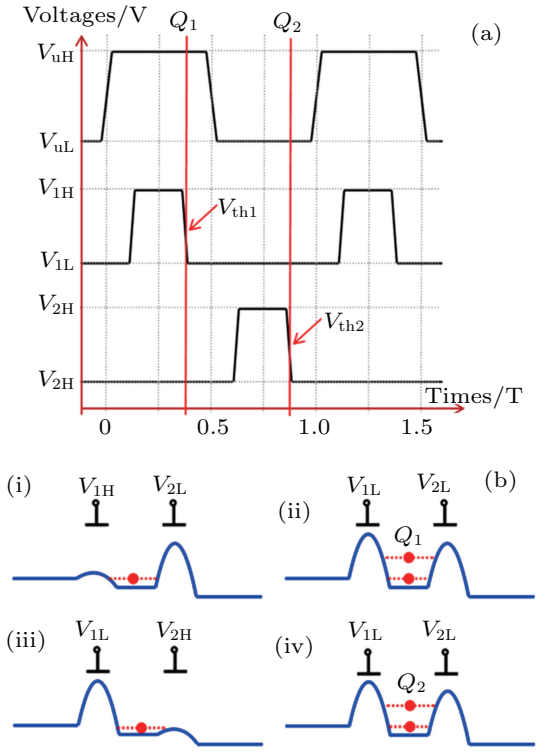


Fig. 2. (color online) (a) Pulse sequence for electron transfer operation and (b) corresponding potential diagrams between source and drain.

The transfer current i_d can be defined as the net charge quantity transferred per second from the source to the drain. Thus, the differential charge ΔQ is expressed as

$$\Delta Q = -\frac{i_d}{f}, \tag{5}$$

where f is the frequency of the clock pulse.

By combining Eqs. (3) and (5), we may derive the transfer current as follows:

$$\begin{aligned} i_d = {} & (C_T - C_{2f}) V_d f + C_u \Delta V_u f + C_{1f} (V_{th10} - V_{1L}) f \\ & + C_{2f} (V_{2L} - V_{th20}) f + C_b \Delta V_b f. \end{aligned} \tag{6}$$

Firstly, the two fringing capacitances C_{1f} and C_{2f} are extracted. The transfer current i_d versus V_d is measured when V_{1L} or V_{2L} is changed but V_u, V_b, and f are kept constant. From Eq. (6), the two fringing capacitances C_{1f} and C_{2f} at a fixed drain bias are expressed by

$$C_{1f} = \left| \frac{di_d}{dV_{1L}} \right| f^{-1}, \quad \text{or} \quad C_{2f} = \left| \frac{di_d}{dV_{2L}} \right| f^{-1}, \tag{7}$$

where di_d/dV_{1L} or di_d/dV_{2L} is the slope of curve $i_d \sim V_{1L}$ or $i_d \sim V_{2L}$ at a given drain voltage, respectively.

Similarly, the transfer current i_d versus V_d is measured when ΔV_u is changed but V_{1H} /V_{1L}, V_{2H}/V_{2L}, V_b, and f are kept constant. From Eq. (6), the capacitance C_u at a fixed drain bias is expressed by

$$C_u = \left| \frac{di_d}{d(\Delta V_u)} \right| f^{-1}, \tag{8}$$

where $di_d/d(\Delta V_u)$ is the slope of the curve $i_d \sim \Delta V_u$ at a given drain voltage.

Next, the total capacitance C_T is extracted. The transfer current i_d versus V_d is measured when f is changed while V_u, V_b, V_{1H}/V_{1L}, and V_{2H}/V_{2L} are kept constant. It is worth pointing out that the threshold voltages V_{th10} and V_{th20} change with the drain voltage V_d, especially for the bulk MOS devices, thus the drain current i_d does not linearly depend on the drain voltage V_d (see Eq. (6)). For varying V_d, we will obtain different C_T. Here, we extract C_T at a fixed drain voltage. According to Eq. (6), we can develop the following equation:

$$\frac{di_d}{df} = (C_T - C_{2f}) V_d + C_{1f} (V_{th10} - V_{1L}) + C_{2f} (V_{2L} - V_{th20}), \tag{9}$$

where di_d/df is the slope of the curve $i_d \sim f$ at a fixed drain bias. We can extract C_T from Eq. (9).

If the drain voltage V_d is restricted in a very small range $(V_d - dV_d, V_d + dV_d)$, the threshold voltages V_{th10} and V_{th20} can be assumed to be the constants approximately. On this condition, equation (6) can be rewritten as follows:

$$i_d = (C_T - C_{2f}) V_d f + C_b \Delta V_b f + \text{const.}, \tag{10}$$

when V_d and ΔV_b are varying while V_u, V_{1H}/V_{1L}, V_{2H}/V_{2L}, and f are kept constant. Thus, C_b is extracted from the contour of i_d between V_d and ΔV_b and expressed as

$$C_b = (C_T - C_{2f}) \left| \frac{dV_d}{d(\Delta V_b)} \right|. \tag{11}$$

Finally, C_s andC_d are extracted. On the basis of Eq. (4) and assuming that $C_s \approx C_d$, the equation is obtained as follows:

$$C_s = C_d = (C_T - C_{1f} - C_{2f} - C_b - C_u)/2. \tag{12}$$

4. Results and discussion

Figure 3(a) shows the plot of threshold voltage V_{th10} versus drain voltage V_d of LG1 MOSFET when $V_s = 0$ V, $V_u = 10$ V, $V_2 = 2$ V, and $V_b = -0.6$ V. It is obvious that the threshold voltage V_{th10} is a function of drain voltage V_d. From Fig. 3(a), the threshold voltage V_{th10} has a maximal value at about $V_d = 0.2$ V, and V_{th10} decreases rapidly as V_d changes to more negative values from the maximal point while V_{th10} decreases slowly as V_d has more positive values. Similarly, the threshold voltage V_{th20} of LG2 MOSFET is a function of the drain voltage V_d as shown in Fig. 3(b) when $V_s = 0$ V, $V_u = 10$ V, $V_1 = 2$ V, and $V_b = -0.6$ V, and its maximal value point also appears at about $V_d = 0.2$ V. The dependence of V_{th10} and V_{th20} on V_d may be mainly caused by the change of substrate surface state as the drain voltage changes. Thus, the transfer current i_d does not linearly depend on the drain voltage V_d, as discussed in the previous section. We further infer

that these capacitances abound the dot must be dependent on the drain bias. Therefore, the capacitances must be extracted only at a fixed drain bias, which is called the work-point-bias (WPB). In the following extraction processes, all the WPB is set to be $V_d = 10$ mV, which is the common drain bias in the DC measurement.

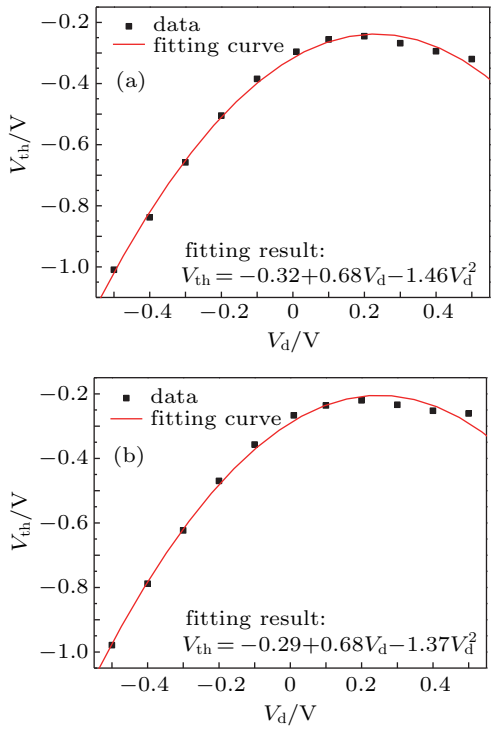


Fig. 3. (color online) (a)Threshold voltage vs. drain voltage for LG1 MOSFET and (b) LG2 MOSFET at direct current measurement. These relations can be fitted as quadratic curves.

Figure 4(a) shows the $i_d - V_d$ curves at different low bias levels V_{1L} of LG1 from -2 to -1.6 V in steps of 0.1 V when $V_s = 0$ V, $V_u = 10$ V, $V_{2H}/V_{2L} = \pm 1.8$ V, $V_{1H} = 1.8$ V, $V_b = -0.6$ V, and $f = 2$ MHz. We obtain the transfer currents $i_d = 0.081$, -0.094, -0.325, -0.554, -0.778 pA for $V_{1L} = -2$, -1.9, -1.8, -1.7, -1.6 V respectively, where the slope scatter points are shown in the inset of Fig. 4(a). The fringing capacitance between the LG1 and the dot is extracted as $C_{1f} = 1.089$ aF by the linear fitting method. Figure 4(b) shows the $i_d - V_d$ curves at different low bias levels V_{2L} of LG2 from -2 V to -1.6 V in steps of 0.1 V when $V_s = 0$ V, $V_u = 10$ V, $V_{1H}/V_{1L} = \pm 1.8$ V, $V_{2H} = 1.8$ V, $V_b = -0.6$ V, and $f = 2$ MHz. The transfer currents are $i_d = -0.833$, -0.528, -0.333, -0.083, 0.203 pA for $V_{2L} = -2$, -1.9, -1.8, -1.7, -1.6 V respectively. The fringing capacitance between the LG2 and the dot is $C_{2f} = 1.259$ aF from the linear fitting of these transfer current data shown in the inset of Fig. 4(b). Figure 4(c) shows the $i_d - V_d$ curves when the difference ΔV_u between V_{uH} and V_{uL} changes from 5.0 V to -5.0 V in steps of -2.5 V at $V_s = 0$ V, $V_{1H}/V_{1L} = \pm 1.8$ V, $V_{2H}/V_{2L} = \pm 1.8$ V, $V_b = -0.6$ V, and $f = 2$ MHz. From the transfer currents $i_d = -0.235$, -0.259, -0.325, -0.415, -0.569 pA for $\Delta V_u = 5$, 2.5, 0, -2.5, -5 V respectively, $C_u = 0.0165$ aF is obtained by the linear fitting method as shown in the inset of Fig. 4(c).

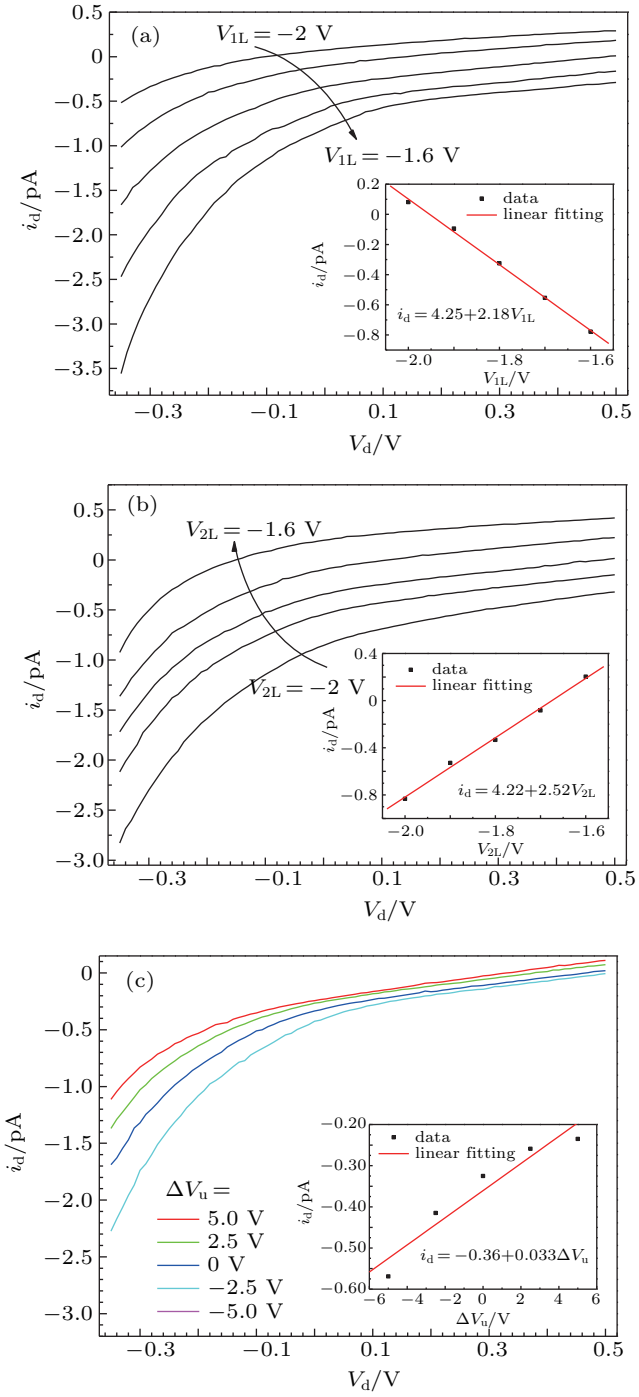


Fig. 4. (color online) Transfer currents versus drain voltages for changing (a) V_{1L}, (b) V_{2L} (b), and (c) ΔV_u, in which the inset figures show the corresponding slope of i_d versus (a) V_{1L}, (b)V_{2L} and (c) ΔV_u at the WPB $V_d = 10$ mV respectively.

Figure 5 shows the electron transfer characteristics of the device for gate pulse frequencies from 0.1 MHz to 5 MHz when $V_s = 0$ V, $V_u = 10$ V, $V_{1H}/V_{1L} = \pm 1.8$ V, $V_{2H}/V_{2L} = \pm 1.8$ V, and $V_b = -0.6$ V. All the six curves are partially bent, which means that the transfer current i_d is not proportional to the drain bias V_d in the whole range, mainly resulting from the threshold voltages V_{th10} and V_{th20} dependent on the

drain voltage V_d. However, the device conductance is approximately proportional to the pulse frequency f as shown in the inset of Fig. 5, indicating that an approximate fixed quantity of charges is transferred in one period of the gate pulses.[15] The inset of Fig. 5 shows the transfer current $i_d = -0.929$, -0.769, -0.665, -0.469, -0.274, -0.052 pA for $f = 5$, 4, 3, 2, 1, 0.1 MHz respectively and the corresponding linear fitting curve. Based on the slope of the fitting curve and Eq. (9), the total capacitance is obtained to be $C_T = 13.759$ aF.

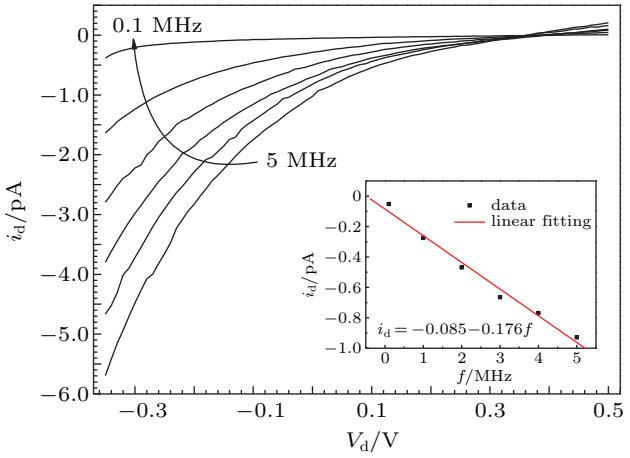


Fig. 5. (color online) Transfer currents vs. drain voltages for changing gate pulse frequencies from 0.1 MHz to 5 MHz, in which the inset (in color) shows the corresponding slope of i_d versus f at the WPB $V_d = 10$ mV.

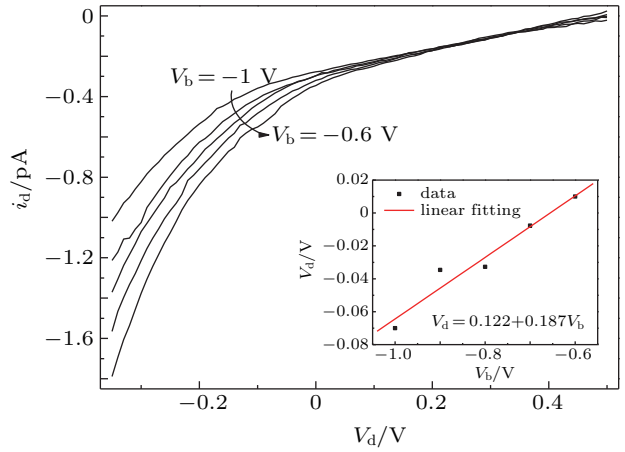


Fig. 6. (color online) Transfer currents vs. drain voltages for changing substrate bias from -1 V to -0.6 V, in which the inset shows the current contour between the drain voltage and the substrate voltage at the reference current $i_d = -0.33$ pA.

Figure 6 shows the i_d–V_d curves at different substrate bias voltages from -1 V to -0.6 V in steps of 0.1 V when $V_s = 0$ V, $V_u = 10$ V, $V_{1H}/V_{1L} = \pm 1.8$ V, $V_{2H}/V_{2L} = \pm 1.8$ V, and $f = 2$ MHz. The current value $i_d = -0.33$ pA is selected as a reference current, at which the corresponding drain voltages are obtained to be $V_d = -0.07$, -0.0346, -0.0327, -0.00769, 0.01 V when $V_b = -1$, -0.9, -0.8, -0.7, -0.6 V by the linear interpolation method, which is shown in the inset of Fig. 6. From the slope of the fitting curve in the inset of Fig. 6 and Eq. (10), $C_b = 2.34$ aF is obtained. Finally, the two capacitances C_s and C_d are calculated to be $C_s = C_d = 4.527$ aF.

It is worth noting that the capacitance C_s or C_d, which could be called 'barrier capacitance' from the source/drain to the dot,[17] is more than three times the fringing capacitance C_{1f} or C_{2f}. It means that the barrier capacitance dominates the total capacitance of the dot. In the test device structure, the silicon dioxide layer thickness beneath the lower gate is 5 nm. If the oxide layer decreases, the fringing capacitances may increase. In general transfer operation, the barrier capacitances would be kept constant, but at the same time the clock pulses are biased on the lower gates to push the charges into (out of) the dot. Thus, the fringing capacitances C_{1f} and C_{2f}, together with C_u, are called the operable capacitances in the previous section, for the electron number on the dot and the potential of the dot could be modulated by the effects of these capacitances.

5. Conclusions

According to the quantum dot structure in the silicon nanowire MOSFET, we present an improved method to extract the coupling capacitances around the dot. Simple formulas to describe the transfer current and the electrode biases are obtained to calculate the total capacitance and the coupling capacitances. By modulating the two barrier potentials beneath the lower gates with phase-shifted pulse voltages, the transfer current is measured and analyzed. The transfer current is proportional to the pulse frequency, but it does not linearly depend on the drain voltage. The barrier capacitances dominate the total capacitance around the dot, but the fringing capacitances are very important for manipulating the charge transfer from the source to the drain. This capacitance extraction technique could be used to determine the capacitance parameters not only in the bulk silicon devices, but also in the SOI MOSFETs.

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