Effects of post-annealed floating gate on the performance of AlGaN/GaN heterostructure field-effect transistors*

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AlGaN/GaN heterostructure field-effect transistors (HFETs) with different floating gate lengths and floating gates annealed at different temperatures, are fabricated. Using the measured capacitance–voltage curves of the gate Shottky contacts for the AlGaN/GaN HFETs, we find that after floating gate experiences 600 °C rapid thermal annealing, the larger the floating gate length, the larger the two-dimensional electron gas electron density under the gate region is. Based on the measured capacitance–voltage and current–voltage curves, the strain of the AlGaN barrier layer in the gate region is calculated, which proves that the increased electron density originates from the increased strain of the AlGaN barrier layer.

Keywords: AlGaN/GaN HFETs, floating gate, rapid thermal annealing, strain

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1. Introduction

Because of the high electron mobility and high breakdown electric field, AlGaN/GaN heterostructure field-effect transistors (HFETs) have been an outstanding candidate for applications in high-frequency and high-power fields.[1,2] In order to take full advantage of the material properties, advanced device structures and device processing, such as field plate, passivation, T-gate, recessed-gate, and back barrier, have been widely used.[3–7]

A floating gate (FG), located in free-contact areas, can be used to enhance the breakdown voltage.[8,9] An appropriate gate annealing temperature can change the strain of the AlGaN barrier layer and improve the electrical properties of AlGaN/GaN heterostructure field-effect transistors.[10] However, the AlGaN/GaN heterostructure field-effect transistors with post-annealed FG have hardly been reported.

In this paper, a novel AlGaN/GaN heterostructure field-effect transistor by employing a post-annealed floating gate is fabricated. Using the measured current–voltage (I–V) and capacitance–voltage (C–V) characteristics, the effect of the post-annealed floating gate on the performance of the AlGaN/GaN heterostructure field-effect transistor is investigated.

2. Experiments

The AlGaN/GaN heterostructure was grown by molecular beam epitaxy (MBE) on a sapphire substrate. The epitaxial structure consists of an $Al_{0.24}Ga_{0.76}N$ (14.9 nm) barrier layer, an AlN (1 nm) interlayer, a GaN (1.5 μm) channel layer, and an AlN (100 nm) buffer layer. Hall measurement shows a sheet electron density (n_{2D}) of 9.89×10^{12} cm^{-2} and an electron mobility (μ) of 2068 cm^2/V·s. Device processing began with device isolation by utilizing Cl_2/BCl_3 inductively coupled plasma (ICP) etching. Ti/Al/Ni/Au was deposited and annealed at 850 °C for 40 s in a rapid thermal annealing (RTA) system to form the source and drain ohmic contacts. After that, Ni/Au FGs were deposited and subsequently annealed in the same rapid thermal annealing system for 40 s. For the remaining property of the ohmic contact (especially considering that the melting point of aluminum in the ohmic contact is about 660 °C), the floating gate (FG) annealing temperatures were chosen as 200 °C, 400 °C, and 600 °C, respectively. Finally, the Ni/Au gate Schottky contact was located in the middle of the source and drain contacts.

As shown in Fig. 1, the gate length (L_G) is 10 μm, the gate width (W) is 100 μm, the source-drain spacing (L_{SD}) is 60 μm, and the FG-gate spacing (L_{FG-G}) is 5 μm. The floating gates are symmetrically located on each side of the gate, and their lengths (L_{FG}) are 0 μm, 5 μm, 10 μm, and 15 μm, which are marked as sample 1, sample 2, sample 3, and sample 4, respectively. The C–V measurements were performed using an Agilent B1520A at 1 MHz; the I–V measurements were performed using an Agilent B1500A semiconductor parameter analyzer.

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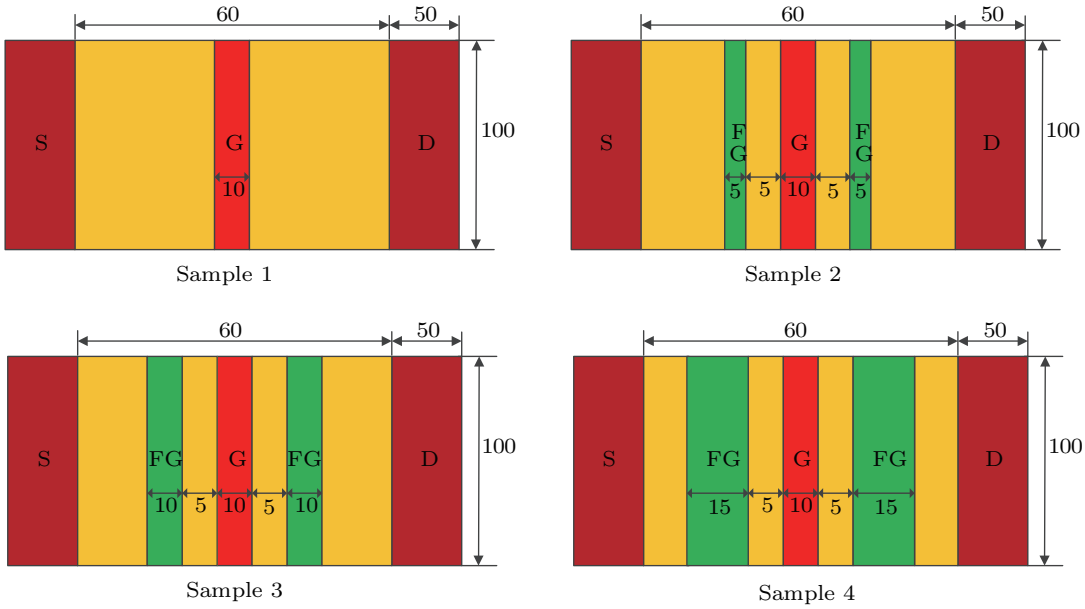


Fig. 1. (color online) Top views for the four samples with the sizes being in units of micrometer.

3. Results and discussion

Using the transmission line method (TLM), the values of specific resistivity ρ_C for the samples after FG RTA processing (0 °C, 200 °C, 400 °C, and 600 °C) are obtained and shown in Fig. 2. The increase of the ρ_C is caused by the degradation of the ohmic contact surface morphology. [11] The increase of the ρ_C can be attributed to forming more TiN after further annealing, which can further reduce the barrier height of the ohmic contact and also the ohmic contact resistance.[11]

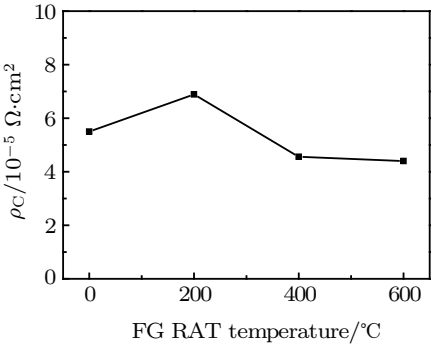


Fig. 2. Variation of specific resistivity ρ_C with floating gate annealing temperature.

The *I*–*V* output characteristics for the four samples after FG RTA processing are shown in Fig. 3. The transfer characteristics for the four samples after FG RTA processing are measured as shown in Fig. 4. It is apparent after FG RTA processing that the samples retain excellent output and transfer characteristics. Figure 5 shows the *C*–*V* curves of the gate Schottky contacts for the samples after FG RTA at different temperatures. $C_0 = \varepsilon_0 \cdot \varepsilon_{\mathrm{AlGaN}} \cdot S_G / d_{\mathrm{AlGaN}}$, where C_0 is the measured capacitance value at zero gate bias for the Schottky contact, ε_0 is the vacuum permittivity, $\varepsilon_{\mathrm{AlGaN}}$ is the relative permittivity of the AlGaN barrier layer, S_G is the Schottky contact area, and d_{AlGaN} is the thickness of the AlGaN barrier layer.[12] The relative permittivity, which is closely related to the spontaneous polarization and piezoelectric polarization in the AlGaN/GaN HFETs, can be changed by the device processing, such as ohmic contacts and Schottky contacts.[12,13] The thermal stress can also affect the relative permittivity.[14–16] Hence the capacitance difference among the four samples after FG RTA processing should originate from the variation of the relative permittivity. This also means that the FG RTA processing can change the relative permittivity of the AlGaN barrier layer. By integrating *C*–*V* curves, the two-dimensional electron gas (2DEG) electron density n_{2D} in the gate region can be obtained as shown in Fig. 6.[17] For the devices without FG RTA (also called as-deposited) or after FG 200 °C RTA, the values of n_{2D} for the four samples are almost the same. After FG 400 °C RTA, the values of n_{2D} for these samples begin to show a little difference. This difference in value of n_{2D} becomes significant after FG 600 °C RTA, and at this annealing temperature the n_{2D} increases with FG length increasing. This means that the FG structure has an important influence on n_{2D} after FG 600 °C RTA. This variation of n_{2D} after FG 600 °C RTA can be explained as follows.

The 2DEG is induced by the spontaneous and piezoelectric polarization in the AlGaN/GaN heterostructure.[18,19] The alloy composition, barrier layer thickness, and barrier layer strain can influence the value of n_{2D}. Because these samples are fabricated on the same AlGaN/GaN heterostructure material, the alloy composition and the barrier layer thickness are uniform. Therefore, the difference in the value of n_{2D} in the gate region after FG 600 °C RTA likely originates from the

variation of the strain of the AlGaN barrier layer.

Using the measured *I*–*V* and *C*–*V* characteristics of the Schottky contacts, we can calculate the total polarization sheet charge density σ_{total} as follows: [10,20]

$$\frac{(\sigma_{\text{total}} - qn_{2\text{D}0})q}{V_0/n_1} = \frac{C_0}{S_{\text{G}}}. \tag{1}$$

Here $n_{2\text{D}0}$ is the 2DEG electron density corresponding to 0 V gate voltage, V_0 is the flat-band voltage, n_1 is the ideality factor. The V_0 and n_1 can be obtained from the forward *I*–*V* characteristics of the gate–source Schottky diode.[21,22] The forward *I*–*V* characteristics of the gate Schottky contacts for the four samples after FG 600 °C RTA are measured as shown in Fig. 7.

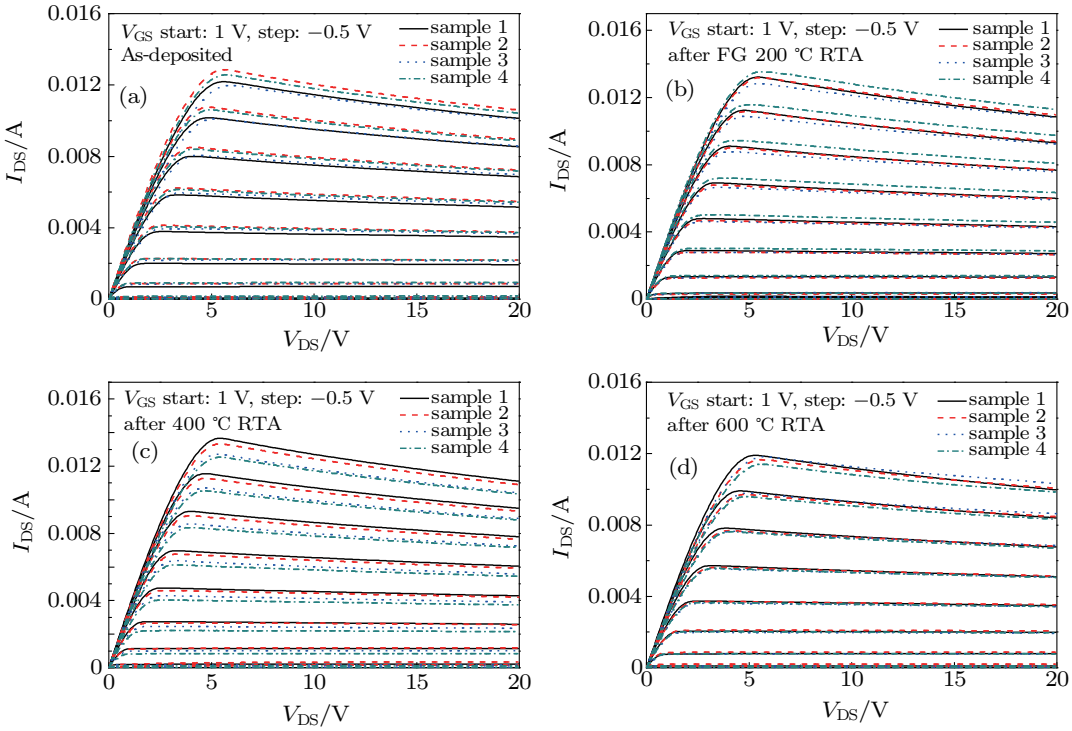


Fig. 3. (color online) Variations of measured *I*–*V* output characteristics for the four samples after FG RTA processing.

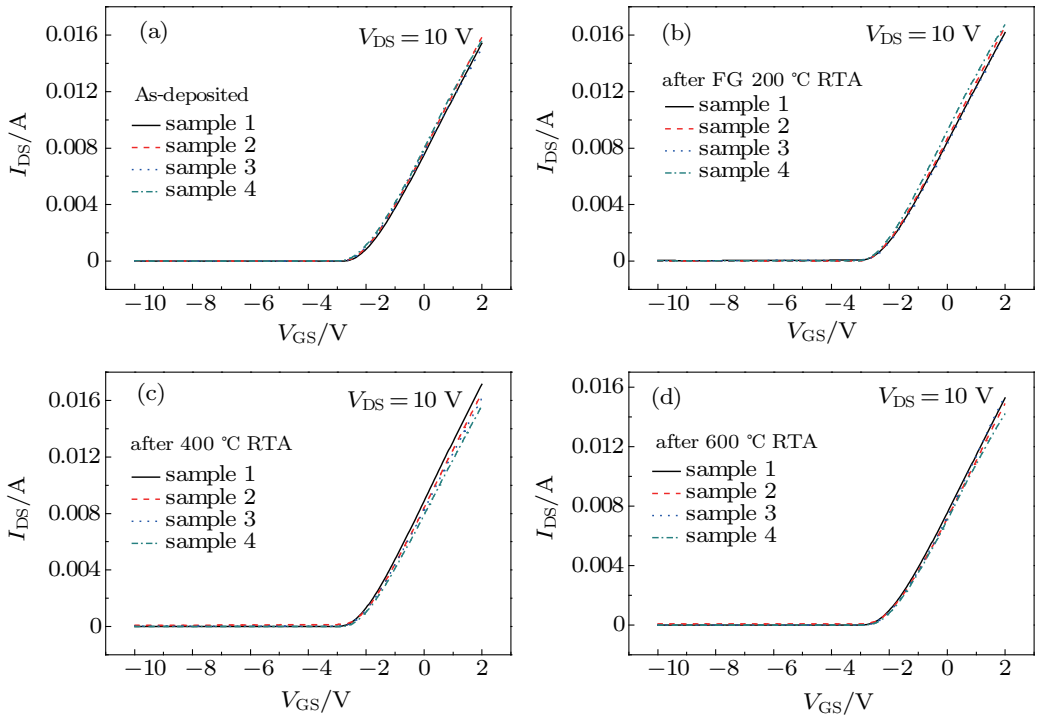


Fig. 4. (color online) Measured transfer characteristics for the four samples after FG RTA processing.

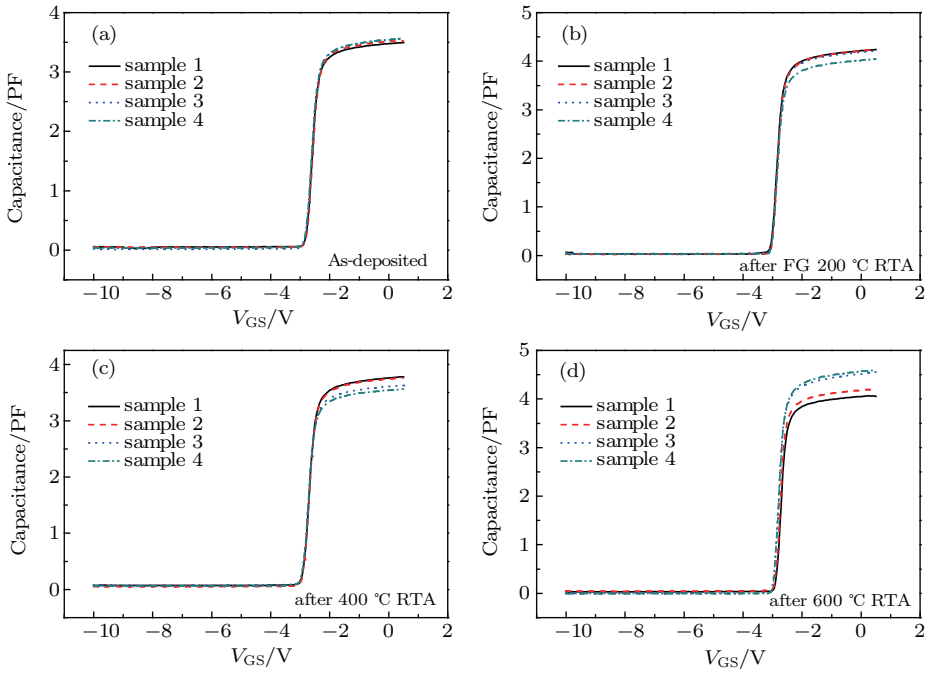


Fig. 5. (color online) Measured *C*–*V* curves for the four samples after FG RTA.

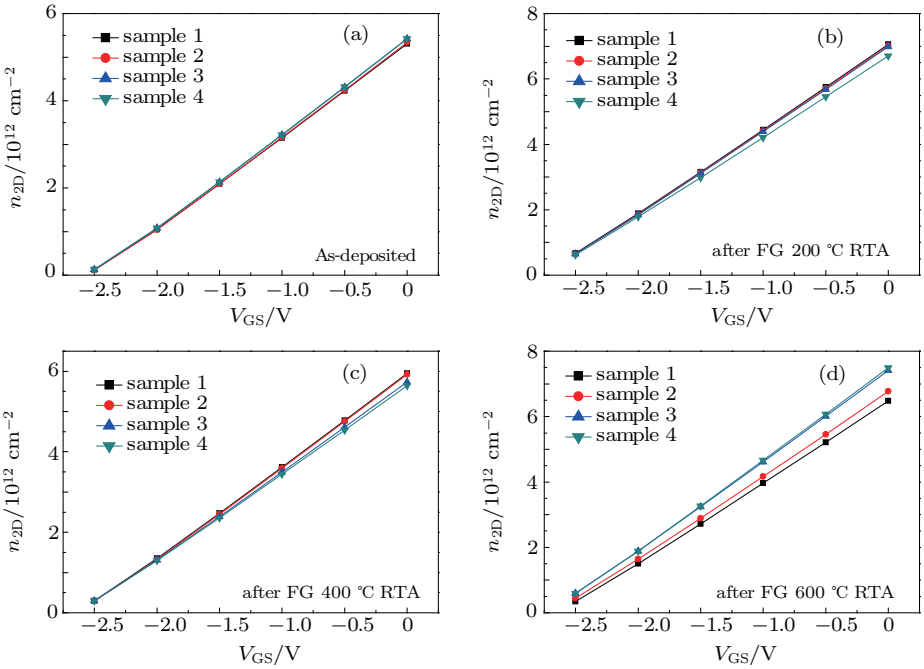


Fig. 6. (color online) Obtained values of n_{2D} under different gate biases for the four samples after FG 200 °C.

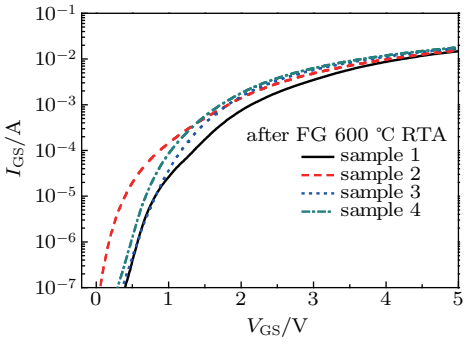


Fig. 7. (color online) Forward *I*–*V* characteristics of the gate Schottky contacts for the AlGaN/GaN HFETs after FG 600 °C RTA.

Based on the obtained σ_{total} and the polarization effect of the AlGaN/GaN heterostructures, the strain of the AlGaN barrier layer can be determined from [18]

$$\sigma_{total} = P_{SP}^{GaN} - (P_{SP}^{AlGaN} + P_{PE}^{AlGaN}), \quad (2)$$

$$P_{SP}^{Al_xGa_{1-x}N} = -0.090x - 0.034(1-x) + 0.019x(1-x), \quad (3)$$

$$P_{PE}^{AlGaN} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right), \quad (4)$$

$$\varepsilon = \frac{a-a_0}{a_0}. \quad (5)$$

Here, P_{SP} and P_{PE} refer to the spontaneous polarization and

piezoelectric polarization, respectively; a_0 and a represent the a-axis lattice constants of the unstrained AlGaN and of the strained AlGaN, respectively; e_{31} and e_{33} are the piezoelectric coefficients; C_{13} and C_{33} are the elastic constants; ε is the a-axis in-plane strain of the AlGaN barrier layer.

The measured and calculated parameters of the four samples after FG 600 °C RTA are shown in Table 1. Table 1 shows that with the increase of the floating gate length, the strain of the barrier layer rises, even reaches a value more than twice the strain of the barrier layer when $L_{FG} = 10$ μm. This means that the floating gate after 600 °C RTA can enhance the strain of the AlGaN barrier layer in the gate region. The larger the floating gate length is, the larger the strain under the gate region is.

Table 1. Measured and calculated parameters of the four samples after FG 600 °C RTA.

After FG 600 °C RTA	$n_{2D0}/10^{16}$ m^{-2}	$C_0/10^{-12}$ F	V_0/V	n_1	$\sigma_{total}/10^{-2}$ (C/m^{-2})	$P_{PE}^{AlGaN}/10^{-3}$ (C/m^2)	ε/%
Sample 1	6.48	4.05	1.004	3.349	1.17	–1.612	0.107
Sample 2	6.77	4.18	0.535	2.528	1.18	–1.746	0.116
Sample 3	7.41	4.52	1.158	3.649	1.32	–3.319	0.220
Sample 4	7.49	4.57	0.989	3.108	1.35	–3.468	0.230

During FG 600 °C RTA, the gate metal atoms (Ni and Au) are at high temperatures and have large energy. The high-energy metal atoms can diffuse into the AlGaN barrier layer and then destroy the lattice structure in the FG region. This destruction of the lattice structure means that the spontaneous and piezoelectric polarization in the AlGaN barrier layer decrease.[10,23] The decrease of the polarization effect makes the tensile strain in the FG region weaker. Consequently, due to the decrease of the tensile strain, the lattice constant of the AlGaN barrier layer in the FG region decreases. Because of the lattice continuity, the lattice in the gate region can be stretched by the contractive lattice in the FG region. The stretched lattice in the gate region results in the increase of the strain. As the FG length increases, the number of FG metal atoms increases with the FG area increasing. During the annealing processing, there are more FG metal atoms which can diffuse into the AlGaN barrier layer. The increase of the diffused metal atoms can further destroy the lattice structure and reduce the lattice constant in the FG region, which can enhance the lattice stretch in the gate region and increase the strain of the AlGaN barrier layer. Therefore, the strain in the gate region can increase with the FG length increasing. For sample 2 with $L_{FG} = 5$ μm, the FG length is not big enough to affect the strain in the gate region, and the increase of strain is less. For sample 3 with $L_{FG} = 10$ μm, the FG length is big enough to change the strain in the gate region, and the sample has the largest strain increase. Because the AlGaN barrier layer is clamped by the GaN channel layer, the increase of strain can be limited after reaching a big enough value, leading to the fact that the increase of strain for sample 4 with $L_{FG} = 15$ μm is smaller than that for sample 3 with $L_{FG} = 10$ μm.

The increase of the strain can cause the increase of the electric field across the AlGaN barrier layer. The electrons in the surface states are identified as the source of the 2DEG electrons in the channel.[19] The surface electric potential energy can be lifted by the increased electric field. More electrons in the surface state are then able to transfer from occupied surface states to empty conduction band states at the interface, leading to the fact that the electrons in the triangular potential well are increased.

4. Conclusions

In this work, the AlGaN/GaN HFETs with different FG lengths and different FG annealing temperatures are fabricated. It is found that for the AlGaN/GaN HFETs after FG 600 °C RTA, the larger the FG length, the larger the value of n_{2D} in the gate region is. Based on the measured C–V and I–V curves, the strain of the AlGaN barrier layer is determined, which proves that the increased n_{2D} originates from the increased strain. It offers a possible approach to improving the performance of AlGaN/GaN HFET with a post-annealed floating gate structure.

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