Reconfigurable dynamic all-optical chaotic logic operations in an optically injected VCSEL*

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In a chaotic system of vertical cavity surface emitting laser (VCSEL) with external optical-injection, we propose a novel implementation scheme for reconfigurable dynamic all-optical chaotic logic operations (AOCLOs). Under different key parameters, such as the bias current, the injection strength and the frequency detuning of the injected light field and the VCSEL, we also explore the evolutions of the polarization-bistability with the amplitude of the injected light field when the output of VCSEL is chaotic wave. According to the dynamic evolutions, we find out the optimal value of the frequency detuning that is considered as a control logic signal, and further implement different AOCLOs, such as AND, NAND, OR, NOR, XOR, and XNOR, by controlling the logic operation of the control logic signal between two logic inputs. Moreover, the ability to reconstruct these logic operations is demonstrated under relatively low noise strength of the spontaneous emission.

Keywords: vertical-cavity surface emitting lasers (VCSEL), polarization switching, chaos, logic design

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1. Introduction

It is well known that chaotic systems have rich dynamic behaviors, which are sensitive to perturbation or instability. In recent years, there has been a new research direction in chaos application that is exploiting the rich patterns inherent in the chaotic systems to do chaos computing. Chaos computing has attracted great interest since it provides a new reconfigurable logic operation scheme, where different logic operations are easily converted by the slight change of the parameters in a chaotic system. This provides a possible way to implement dynamic logic operation architecture. In the process of logic operation, the system structure itself changes dynamically. Therefore, chaotic logic devices have many advantages over the traditional logic ones, in the areas such as more security, more flexible and lower power cost.[1–6] Recently, the most fundamental computing functions based on chaotic elements have been implemented in many experimental and theoretical researches. For example, in 2003, Murali *et al.* put forward the implementation scheme of NOR gate based on logistic map.[1] In 2006, they constructed the dynamic logic gates and realized all logic operations in a single discrete-time chaotic system.[2] In 2008, using the logistic map, Yang *et al.* proposed dynamic logic gates by designing three thresholds and using the different analog-logic mapping relations between the output signals.[3] In 2010, Peng *et al.* provided a chaotic logic operation scheme in a drive-response chaotic synchronization system in a nonlinear circuit.[4] In 2015, Beyki and Yaghoobi explored a new chaotic logic gate implementation scheme by using genetic algorithm.[5]

The chaotic logic operations in a semiconductor laser system have many advantages over those in the nonlinear circuit system, in some aspects such as wider bandwidth, faster response speed, higher security, and lower power cost. Optical chaotic logic operations are the most critical technology in future optical chaotic network secure communication, however, the technology of the optical chaotic logic operations still lags behind. And it has received little attention and is still in the initial stage of research. For most of the logic processing of optical chaotic signals, such as multiplexing, demultiplexing, switching, regeneration, storage and calculation, it is necessary to implement all-optical chaotic logic devices and sequential logic ones with low power consumption and high speed. Vertical cavity surface emitting laser (VCSEL), as a microchip semiconductor laser, exhibits many advantages over edge emitting laser, in some areas such as low threshold current, single longitudinal mode operation, high modulation frequency, low cost and large-scale integration into two-dimensional arrays.[7–13] There are two polarization components (PCs) in the VCSEL with the spin flip mode (SMF),[14] due to the weak material and cavity anisotropies. Much effort has been devoted to the observation of the polarization-bistability (PB) of the VCSEL subjected to different polarization light feedbacks and injection current sweep rates.[7–10] The PB has a faster response time than the absorption bistability. It is very attractive that the all-optical chaotic logic operations (AOCLOs) with low power and high speed can be implemented by using the PB of the optically injected VCSEL.

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Several researches have been done to explore logic gates by using the chaotic synchronization between two semiconductor lasers[11–15] or the PB of the VCSEL[16–31] In 2013, according to a master-slave-response synchronization system of chaotic multiple-quantum-well lasers, Yan proposed the computing methods of chaotic XNOR, NOR, NOT logic gates,[11] and implemented optoelectronic NOR and XNOR logic gates by using parallel synchronization of three chaotic lasers.[13] Recently, different types of chaotic logic gates have been explored by using the PB of the optically injected VCSEL in different setups.[7–10]

However, at present, most of optical chaotic logic operations are implemented under static conditions.[7–13,16,20,32] Since the VCSEL with external optical feedback or external optical injection, as a nonlinear system with high dimension, has not only rich nonlinear dynamic behaviors, but also generates PB. It is great prospect that reconfigurable dynamic AOCLOs are implemented by using the rich patterns of the optically injected VCSEL and its PB. However, there are many fundamental scientific problems that need solving in this field, such as the ability to restructure AOCLOs, the constraint relations between chaotic logic operations and the key parameters of the VCSEL, the selection of logic control signal, etc. Motivated by these problems, in an optically injected VCSEL, we explore the dynamic evolutions of the PB with some key parameters such as the bias current, the light injected strength, the frequency detuning of the injected field and the VCSEL. We further propose the implementation steps for reconfigurable dynamic AOCLOs, and elaborate the ability to reconstruct basic AOCLOs, such as AND, NAND, OR, NOR, XOR, XNOR. The rest of this paper is organized as follows. In Section 2 we give the schematic diagram of AOCLOs in an optically injected VCSEL, and present the corresponding theory model. In Section 3 we present the results and discuss the implementation of basic AOCLOs, and demonstrates their reconfiguration abilities. Finally, we draw some conclusions from the present study in Section 4.

2. Theory and model

Using the rich patterns in a chaotic system based on the optically injected VCSEL, the implementation scheme for AOCLOs is put forward as shown in Fig. 1. Figure 1(a) and 1(b) show the principle block diagram and light paths in detail, respectively. In Fig. 1(a), when the optically injected VCSEL is considered as a chaotic processor, the chaotic states of the output two PCs depend on the following rate equations:[15]

$$\dot{E}_x(t) = f_1(I, C, E_x, E_y, N, n), \tag{1}$$

$$\dot{E}_y(t) = f_2(I, C, E_x, E_y, N, n), \tag{2}$$

$$\dot{N}(t) = f_3(E_x, E_y, N, n), \tag{3}$$

$$\dot{n}(t) = f_4(E_x, E_y, N, n), \tag{4}$$

Here, $\dot{E}$, $\dot{N}$, and $\dot{n}$ represent the first order differential; f represents a function; x and y represent the x-PC and the y-PC emitted by the VCSEL, respectively; $E_x(t)$ and $E_y(t)$ are the

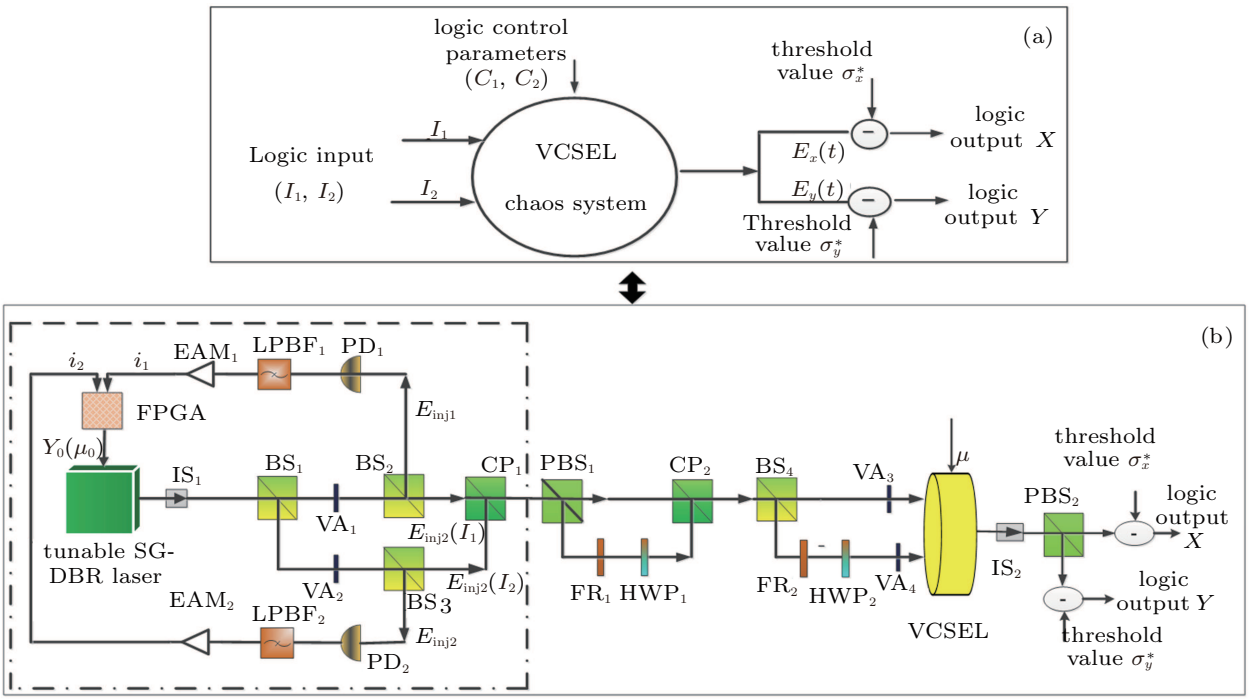


Fig. 1. (color online) Schematic diagram of all-optical chaotic logic operations in an optically injected VCSEL, showing (a) principle block diagram; (b) detailed light paths; SG-DBR laser: sampled grating distributed Bragg reflector laser; VCSEL: vertical cavity surface emitting laser; IS: isolator; μ: normalized injection current of VCSEL; μ_0: normalized injection current of SG-DBR laser; EAM: electric amplifier; PD: photo-detector; BS: beam splitter; PBS: polarization beam splitter; HWP: half-wave plate; FR: faraday rotator; CP: coupler; VA: variable attenuator; LPBF: low pass Bessel filter; FPGA: field programmable gate array; parameters σ_x* and σ_y*: thresholds of x-PC and y-PC respectively; i: electric signal.

amplitudes of the x-PC and the y-PC, respectively; I is the injected light amplitude and is the sum of two square waves that encode two logic inputs, i.e., $I = I_1 + I_2$; the control parameter C equals the sum of two square waves that encode two control logic signals, i.e., $C = C_1 + C_2$; N is the total carrier concentration; n is the difference in concentration between spin-up carriers and spin-down carriers. Since that the chaotic-state of the output x-PC and y-PC are varied simultaneously when the chaotic processor is subjected to the injection of external light, the output x-PC and y-PC are considered as two logic outputs, defined as X and Y, respectively. Suppose that the mean square errors (MSEs) of $E_x(t)$ and $E_y(t)$ are defined as σ_x and σ_y, and their thresholds are fixed at σ_x^* and σ_y^*, respectively, we obtain that $X = 0$ and $Y = 0$ if $\sigma_x - \sigma_x^* \leq 0$ and $\sigma_y - \sigma_y^* \leq 0$; $X = 1$ and $Y = 1$ when $\sigma_x - \sigma_x^* > 0$ and $\sigma_y - \sigma_y^* > 0$. To implement AOCLOs, we put forward the technical steps below.

Step 1 Firstly, the dynamic state mappings of the output x-PC and y-PC in the parameter space of I and C are calculated, and the variation ranges of I in chaotic region are found when C_1 and C_2 are fixed at different values. Then the evolutions of the PB of the VCSEL with the parameter space of I and C_1 (C_2) are further calculated. By observing the location of the PB loop at the value of I to realize chaotic output, the optimal values of I, C_1 and C_2 are selected.

Step 2 Add the external injection and control parameters $I(t) = I_1(t) + I_2(t)$ and $C(t) = C_1(t) + C_2(t)$ for chaotic logic AND, OR, NAND, NOR, XOR, and XNOR operation; $I(t) = I_1(t)$ and $C(t) = C_1(t) + C_2(t)$ for the logic NOT operation.

Step 3 The chaotic state of the output x-PC and y-PC are updated by recalculating the rate-equations (1)–(4). And their MSEs, σ_x and σ_y, need further calculating.

Step 4 Threshold mechanism for obtaining the logic output, i.e., with the fixed thresholds σ_x^* and σ_y^*, $X = 0$ and $Y = 0$ if $\sigma_x - \sigma_x^* \leq 0$ and $\sigma_y - \sigma_y^* \leq 0$; $X = 1$ and $Y = 1$ if $\sigma_x - \sigma_x^* > 0$ and $\sigma_y - \sigma_y^* > 0$.

An all-optical logic operation can be realized when C meets a certain logic relation between I_1 and I_2. When the steps 2-4 above are repeated, the others can be performed by varying the logic operation of C between two inputs. According to the above-mentioned principle, Fig. 1(b) gives the detailed light path for the implementation of AOCLOs. Here, the center wavelength of the VCSEL is 1550 nm; the optical isolator 1 (IS_1) is used to avoid the light from the polarization beam splitter 1 (PBS_1) to feedback into the SG-DBR laser; the IS_2 is used to avoid the light from the PBS_2 to feedback into the VCSEL; the variable attenuator 3 (VA_3) and the VA_4 are used to control the injected strengths of the x-PC and the y-PC, respectively. The wavelength of sampled grating distributed Bragg reflector (SG-DBR) laser is tuned by the injection current. The light emitted by the SG-DBR laser is divided into two beams by the beam splitter 1 (BS_1). They are again separated into two beams of light with the same energy by the 1×2 BS_2 and 1×2 BS_3, respectively. So, the amplitudes of two beams of light from the BS_2 are represented by E_{inj1}, and those from the BS_3 are denoted as E_{inj2}. The E_{inj1} and E_{inj2} are used to encode two logic inputs I_1 and I_2, respectively. E_{inj1} and E_{inj2} are varied by the VA_1 and VA_2, respectively, but unvaried with the injection current μ_0. Here, the frequency detunings $\Delta\omega_1$ and $\Delta\omega_2$ between the SG-DBR laser and the VCSEL are used to encode two control logic signals C_1 and C_2, respectively, where $\Delta\omega_1$ and $\Delta\omega_2$ are generated by the injection currents μ_{01} and μ_{02}, respectively. To implement AOCLOs, the control signal needs to meet different logic relations between two logic inputs. So, it will be varied with the logic inputs for different all-optical logic operations. How to synchronize the control signal with the logic inputs is a key problem. For this purpose, we propose a scheme to solve the problem as follows. One beam of light with the amplitude of E_{inj1} from the BS_2 is converted into the electric signal $i_1$by the photo-detector 1 (PD_1). The i_1 is amplified by electric amplifier 1(EAM_1), the noise in it from the PD_1 is filtered out by the low pass Bessel filter 1. The electric signal i_2 converted by the light with the amplitude of E_{inj2} is processed in the same way. The i_1 and i_2 are encoded into two electric logic inputs, which are logically consistent with the I_1 and I_2, respectively. Moreover, the injection current μ_0 is encoded into the logic output Y_0 of the field programmable gate array (FPGA). If $\mu_0 = \mu_{01}$, $Y_0 = 0$, correspondingly, $\Delta\omega = \Delta\omega_1$ ($C = C_1$); when $\mu_0 = \mu_{02}$, $Y_0 = 1$. As a result, $\Delta\omega = \Delta\omega_2 (C = C_2)$. By using the FPGA, the μ_0 can be implemented by different logic operations between the i_1 and i_2, such as logic AND, OR, NAND, NOR, XOR, and XNOR operation. In this way, the control logic C can be realized indirectly by different logic operations between the two optical logic inputs I_1 and I_2. For each logic operation, the control logic C can also be changed synchronously with the optical logic inputs. Therefore, it is prospective that AOCLOs can be further performed by varying the logic relation of the control signal between the two logic inputs.

In addition, the polarized direction of the SG-DBR laser may emerge in an arbitrary direction. To ensure the polarized light from the SG-DBR to be accurately injected into the x-PC and the y-PC of the VCSEL, respectively, the polarized light from the SG-DBR needs converting into linear polarization light by some optical passive devices placed between the coupler 1 (CP_1) and the VCSEL. Here we consider the converted linear polarization light is the x-PC. For this purpose, the arbitrary polarized light from CP_1 is separated into the x-PC and y-PC by the PBS_1. The x-PC from the PBS_1 is directly injected into CP_2. The y-PC from the PBS_1 is firstly switched into the x-PC by the faraday rotator 1 (FR_1) and half wave plate 1 (HWP_1), then injected into the CP_2. Thus, the light

from the CP_2 is ensured to be the x-PC, and is split into two beams by BS_4. One of the two beams is directly injected into the x-PC of the VCSEL, the other is firstly converted into the y-PC by FR_2 and HWP_2, then injected into the y-PC of the VCSEL. The injected x-PC and y- PC have the same amplitude. Their amplitudes are considered as logic inputs. With a fixed bias current, the output x-PC and y-PC from the VCSEL are a digital chaotic wave, and set to be two logic outputs, X and Y. Besides, in Fig. 1(b), the rate-equations. (1)–(4) are replaced by the following specific expressions:[14]

$$\begin{aligned}\frac{\mathrm{d}E_x(t)}{\mathrm{d}t} &= k(1+ia)\left[N(t)E_x(t)+in(t)E_y(t)-E_x(t)\right]\\ &\quad -i\left(\gamma_\mathrm{p}+\Delta\omega\right)E_x-\gamma_\mathrm{a}E_x\\ &\quad +\sqrt{\beta_{sp}\gamma_e N}\xi_x+K_xE_\mathrm{inj}, \qquad (5)\\ \frac{\mathrm{d}E_y(t)}{\mathrm{d}t} &= k(1+ia)\left[N(t)E_y(t)-in(t)E_x(t)-E_y(t)\right]\\ &\quad +i\left(\gamma_\mathrm{p}-\Delta\omega\right)E_y+\gamma_\mathrm{a}E_y\\ &\quad +\sqrt{\beta_{sp}\gamma_e N}\xi_y+K_yE_\mathrm{inj}, \qquad (6)\\ \frac{dN(t)}{\mathrm{d}t} &= -\gamma_e\left[N\left(1+|E_x|^2+|E_y|^2\right)\right]\\ &\quad +\gamma_e\mu-i\gamma_e n\left(E_yE_x^*-E_xE_y^*\right), \qquad (7)\\ \frac{dn(t)}{\mathrm{d}t} &= -\gamma_s n-\gamma_e n\left(|E_x|^2+|E_y|^2\right)\\ &\quad +\gamma_e\mu-i\gamma_e N\left(E_yE_x^*-E_xE_y^*\right), \qquad (8)\end{aligned}$$

where x and y represent the x-PC and the y-PC, respectively; E is the normalized amplitude, $E=\sqrt{g/\gamma_e}A$, with g being the differential material gain, A is the slowly varying amplitude; N is the total carrier concentration; n is the difference in concentration between carriers with spin-up and carriers with spin-down; k is the field decay rate; γ_e is the decay rate of N; γ_s is the spin-flip relaxation rate; a is the linear enhancement factor; γ_a is the linear dichroism; γ_p is the linear birefringence; $\mu=(\Gamma g/k)[U/(2eV\gamma_\mathrm{e})-N_0]$ (μ is the normalized injection current which equals 1 at the lasing threshold current); V is the volume of the active layer, Γ is the field confinement factor to the active region, e is the electron charge, U is the injected current, N_0 is the half the transparency carrier density; D is the noise strength parameter and defined as $\sqrt{\beta_\mathrm{sp}\gamma_e N}$, with β_sp being the spontaneous emission factor; ξ_x and ξ_y are two independent Gaussian white noises with the mean value of 0 and the variance of 1, and their correlation coefficients are $\langle\xi_\mathrm{i}(t)\xi_\mathrm{j}(t)^*\rangle=2\delta_\mathrm{ij}\delta(t-t')$. Here, the above-mentioned parameters are considered above the threshold value; K_x and K_y are the injection strengths of the x-PC and y-PC, respectively. $E_\mathrm{inj}=\sqrt{g/\gamma_e}A_\mathrm{inj}$ is the normalized amplitude of the injected field, which is the sum of E_inj1 and E_inj2. A_inj is the slowly varying amplitude of the injected field; the frequency detuning of the injected field $\Delta\omega=\omega_\mathrm{inj}-\omega_\mathrm{ref}$, ω_inj is the optical angular frequency of the injected field, and the reference angular frequency ω_ref is defined as $(\omega_x+\omega_y)/2$, with ω_x and ω_y being the angular optical frequency of the x-polarization and the y-polarization of the free-running VCSEL, respectively. Here, $\omega_x=-\gamma_\mathrm{p}+a\gamma_\mathrm{a}$, $\omega_y=\gamma_\mathrm{p}-a\gamma_\mathrm{a}$.

3. Results and discussion

Using the fourth-order Runge–Kutta method, we firstly calculate Eqs. (5)–(8). The numerical values in calculation are presented in Table 1. Figure 2 shows the polarization-resolved P–U curve for the free-running 1550-nm-VCSEL. It can be seen from this diagram that the threshold current U_th is 6.8 mA. When $U=6.8$ mA, only the y-PC begins to oscillate; for 6.8 mA $< U <$ 7.6 mA, the y-PC continues to oscillate; when $U>7.6$ mA, the x-PC will oscillate while the y-PC begins to be suppressed; for $U>7.76$ mA, the x-PC continues to oscillates and the y-PC is suppressed completely.

According to Step 1, in this work, we take the frequency detuning $\Delta\omega$ as the control parameter C, and consider the injected amplitude E_ing as logic input. With the aim of implementing AOCLOs, we calculate the mapping of the dynamic states of the x-PC and that of the y-PC in the parameter space of E_inj and $\Delta\omega$ under $K_x=0$ ns^{-1} and $K_y=10$ ns^{-1} (see Fig. 3). From this diagram, one sees that some typical dynamical states such as period-one oscillation (P_1), period-two oscillation (P_2), quasi-periodic oscillation (QP) and chaotic state

Table 1. Numerical values for all-optical chaotic logic operations.

The parameter and symbol	value	The parameter and symbol	value
Line-width enhancement factor a	3	The noise strength D	10^8
The field decay rate k	300 ns^{-1}	Field confinement factor to the active region Γ	0.5
Spin relaxation rate γ_s	50 ns^{-1}	One half of transparency carrier density N	8×10^{23} m^{-3}
Nonradiative carrier relaxation rate γ_e	1 ns^{-1}	Volume of the active layer V	21.206 μm^3
Dichroism γ_a	2 ns^{-1}	The duration of the bit T	10 ns
Birefringence γ_p	60 ns^{-1}	The slowly varying amplitude of the injected field A_{inj}	1.114×10^{10} m$^{-3/2}$
The normalization pump current μ	2.0	Threshold current of VCSEL U_th	6.8 mA
Injection strength of x polarization K_x	0 ns^{-1}	The differential material gain g	2.9×10^{-12} m^3·s^{-1}
Injection strength of y polarization K_y	10 ns^{-1}	The injection strength $E_\mathrm{inj\ II}$	0.67
Center wavelength λ	1550 nm	The injection strength $E_\mathrm{inj\ III}$	0.72
The injection strength $E_\mathrm{inj\ I}$	0.62		

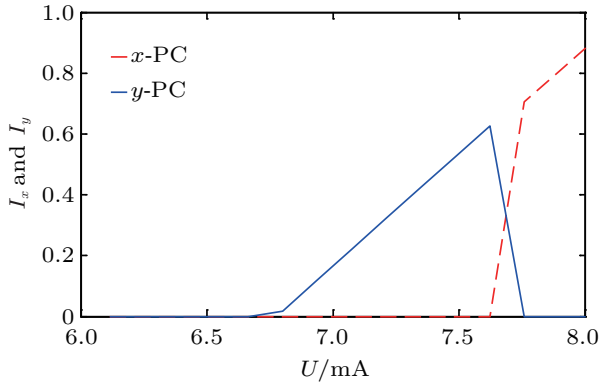


Fig. 2. (color online) *P–U* curve for a free running 1550-nm-VCSEL, where the red dash line represents *x*-polarization component (*x*-PC) and the blue solid line refers to *y*-polarization component (*y*-PC). Here, $I_x = |E_x|^2$, $I_y = |E_y|^2$.

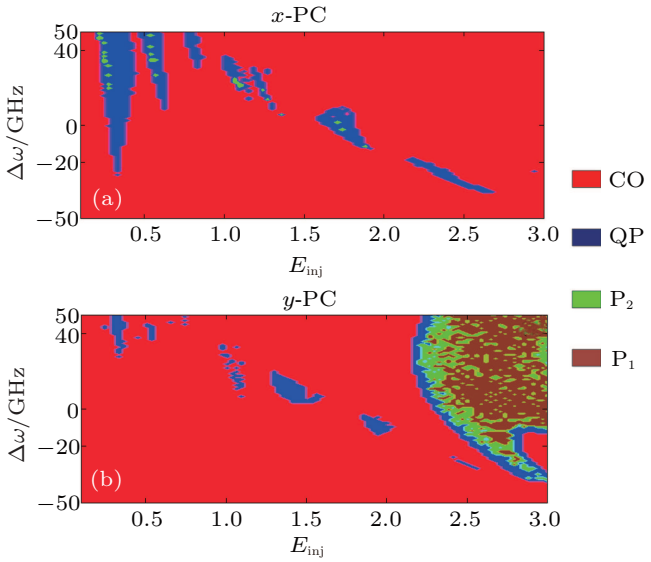


Fig. 3. (color online) Mappings of dynamic states in the parameter space of $\Delta\omega$ and $E_{\rm inj}$ under $K_x = 0$ ns^{-1}, $K_y = 10$ ns^{-1}, $\mu = 2.0$. Here, CO: chaotic state; QP: quasi-periodic oscillation; P_1: period-one oscillation; P_2: period–two oscillation.

(CO) can be observed, through regulating $E_{\rm inj}$ and $\Delta\omega$. Here, $\Delta\omega_1 = 40$ GHz and $\Delta\omega_2 = -20$ GHz are considered as two components of C (C_1 and C_2), respectively. Correspondingly, the values of logic output Y of the FPGA are 1 and 0, respectively (see Fig. 1). So we mainly concern the chaotic region under $\Delta\omega_1 = 40$ GHz and $\Delta\omega_2 = -20$ GHz. By carefully observing Fig. 3(a), for $\Delta\omega_1 = 40$ GHz, while $E_{\rm inj}$ varies in several spaces such as 0.1–0.28, 0.41–0.48, and 0.59–0.74, the output *x*-PC is in CO. The output *y*-PC presents CO when $E_{\rm inj}$ varies from 0.1 to 0.36, or from 0.39 to 0.52, or from 0.57 to 2.18; If $\Delta\omega_2 = -20$ GHz, the output *x*-PC shows CO when $E_{\rm inj}$ is in turn between 0.1 and 0.36, 0.38 and 2.23, as well as 2.43 and 3. The output *y*-PC exhibits CO while $E_{\rm inj}$ varies from 0.1 to 2.56.

To obtain the optimal value of I in Step 1, in the following, we take $\Delta\omega_1 = 40$ GHz for an example to calculate the dynamic evolutions of the PB with some different key parameters such as μ, K_x, and K_y. Figure 4 gives the evolutions of the PB with μ, where the scanning period of $E_{\rm inj}$ is 10 ns. One sees from Fig. 4 that for the *x*-PC and the *y*-PC, with the further increase of the injection current, their bistability-loops (BLs) shift toward the direction of $E_{\rm inj}$ increasing. When μ increases to 2, the BLs are located in the range of $E_{\rm inj}$ from 0.32 to 0.73, where the outputs *x*-PC and the *y*-PC may be in CO, or P_2, or QP (see Fig. 3).

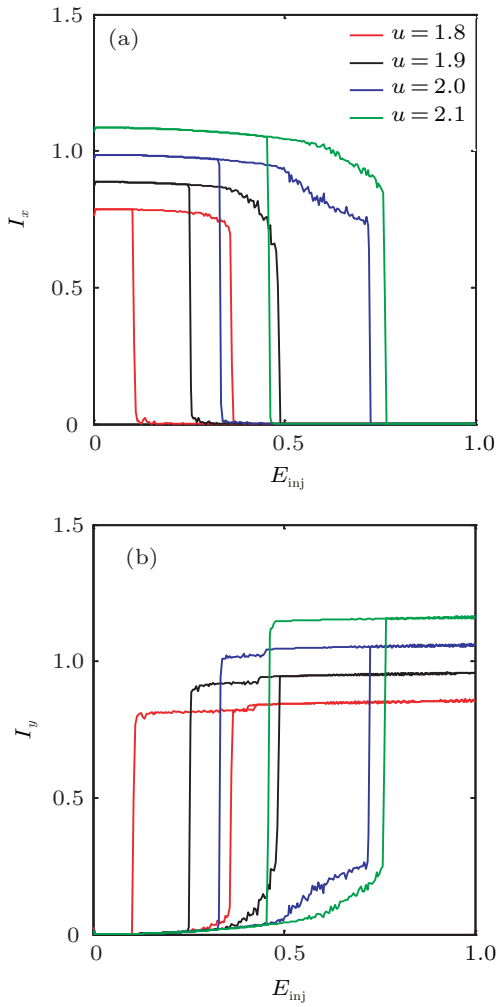


Fig. 4. (color online) Variations of the polarization bistabilities with $E_{\rm inj}$ for different values of μ, where $K_x = 0$ ns^{-1}, $K_y = 10$ ns^{-1}, $T = 10$ ns, and $\Delta\omega_1 = 40$ GHz.

Figure 5 further shows the bistability evolutions of the *x*-PC and the *y*-PC with $E_{\rm inj}$ for different values of K_x, where $\mu = 2$ and the other parameters are given in Fig. 4. From this diagram, it is found that there is no effect of K_x on the shifting of their BLs. All BLs are almost the same and located in the parameter space of $E_{\rm inj}$ from 0.37 to 0.74, where the output PCs may be in CO, or P_2, or QP (see Fig. 3). Also we calculate the evolution of the PB with K_y in Fig. 6. One sees from Fig. 6 that with K_y increasing from 3 ns^{-1} to 20 ns^{-1}, the width of the BLs are gradually shrunk, and the BLs are shifted toward the direction of $E_{\rm inj}$ decreasing. It is noted that if K_y is fixed at 10 ns^{-1}, the BLs both occur in the range of $E_{\rm inj}$ between 0.32 and 0.74, where the output two PCs may exhibit CO, or P_2, or QP state (see Fig. 3).

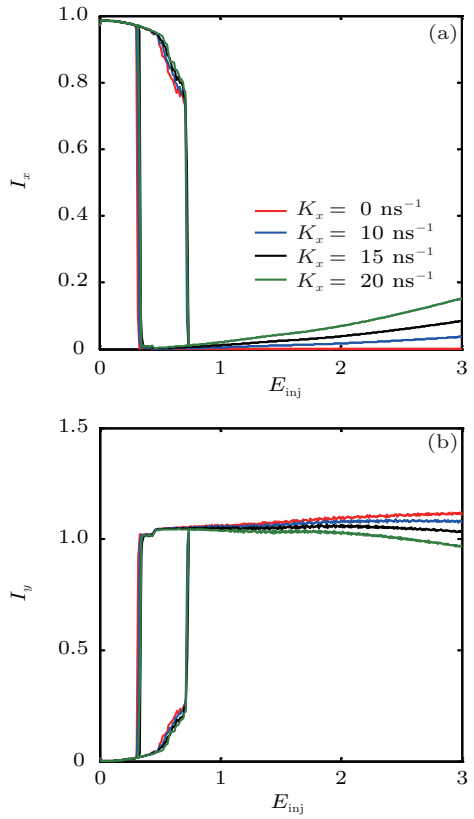


Fig. 5. (color online) Evolutions of the polarization bistabilities with $E_{\rm inj}$ for different values of K_x, where $\mu = 2$ and the other parameters are the same as those given in Fig. 4.

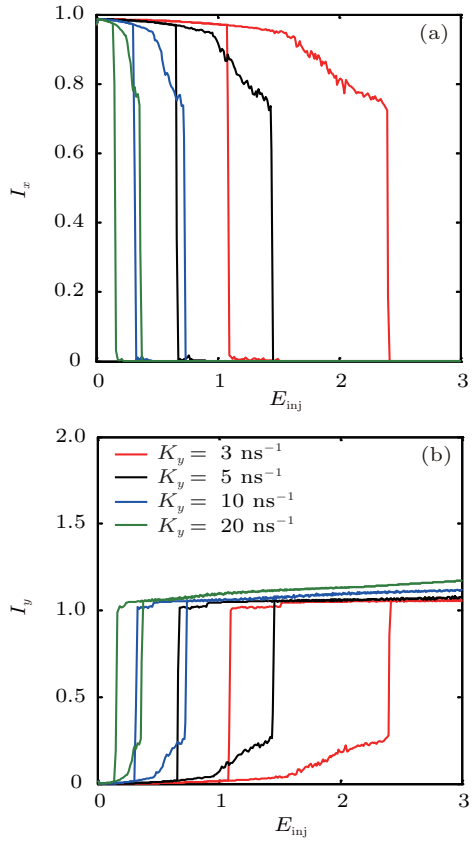


Fig. 6. (color online) Evolutions of the polarization bistabilities with $E_{\rm inj}$ for different values of K_y, where $\mu = 2$ and the other parameters are the same as those given in Fig. 4.

Under $\Delta\omega_2 = -20$ GHz, the evolutions of the PB with the above-mentioned parameters have similar behaviors to those under $\Delta\omega_1 = 40$ GHz. To further determine the specific value of $E_{\rm inj}$ that encodes logic input, we present the bistability of the x-PC and the y-PC under $\Delta\omega_1 = 40$ GHz and that under $\Delta\omega_2 = -20$ GHz as shown in Fig. 7. From this diagram, it is found that the BLs of the x-PC and the y-PC are located at $E_{\rm inj}$ that possesses a variation range of about 0.37–0.73 to realize chaotic output when $\Delta\omega_1 = 40$ GHz. But for $\Delta\omega_2 = -20$ GHz, the BLs occur at $E_{\rm inj}$ that varies from 1.89 to 2.98, where the two outputs PCs may be in CO, or QP, or P_2, or P_1.

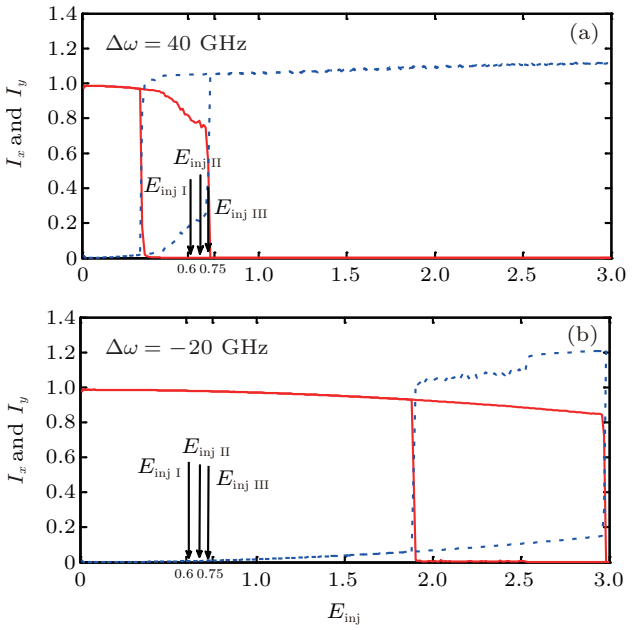


Fig. 7. (color online) Bistability of the x-PC and the y-PC under $\Delta\omega_1 = 40$ GHz (a) and (b) that under $\Delta\omega_2 = -20$ GHz, where the other parameters are the same as those presented in Fig. 4; the red-solid line: the x-PC; the blue-dash line: the y-PC. Arrows indicate the three-level signals used to encode the logic inputs (see text for details).

Suppose that $E_{\rm inj}$ equals the sum of two square waves that encode two logic inputs, i.e., $E_{\rm inj} = E_{\rm inj1} + E_{\rm inj2}$. Here, $E_{\rm inj1}$ and $E_{\rm inj2}$ are considered as logic input I_1 and I_2, respectively. Since the logic inputs can be either 0 or 1, there exist four distinct input sets: (0, 0), (0, 1), (1, 0), (1, 1). We can encode four logic input sets with three-level signals $E_{\rm inj\,I}$, $E_{\rm inj\,II}$, and $E_{\rm inj\,III}$, where $E_{\rm inj\,II}$ represent the (0, 1) and (1, 0), the $E_{\rm inj\,I}(E_{\rm inj\,II} - \Delta E_{\rm inj})$ represents the set (0, 0) and $E_{\rm inj\,III}(E_{\rm inj\,II} + \Delta E_{\rm inj})$ denotes the set (1, 1). The three-level signal used to vary $E_{\rm inj}$ is constant during a time interval T, and defined as bit duration time. Here, T is set to be 10 ns, i.e., the rate of all-optical logic gates is 0.1 GHz. Since that the two PCs both present chaotic states in the range of $E_{\rm inj}$ from 0.59 to 0.73 under $\Delta\omega_1 = 40$ GHz and $\Delta_2 = -20$ GHz (see Fig. 3) we take $E_{\rm inj\,I} = 0.62$, $E_{\rm inj\,II} = 0.67$ and $E_{\rm inj\,III} = 0.72$ as the three-level signals (see Fig. 7). Here, $I_1 = 0$ and $I_2 = 0$ when $E_{\rm inj1} = 0.31$ and $E_{\rm inj2} = 0.31$, and $I_1 = 1$ and $I_2 = 1$ if $E_{\rm inj1} = 0.36$ and $E_{\rm inj2} = 0.36$.

Furthermore, according to Step 4, the logic outputs X and Y depend on the amplitude threshold values of the out-

puts x-PC and the y-PC, respectively. How to determine their threshold values is the key to judging logic outputs. For this purpose, suppose that $C = 0$ when $\Delta\omega = -20$ GHz; $C = 1$ if $\Delta\omega = 40$ GHz, we consider that C has different logic operations between I_1 and I_2, such as logic AND, NAND, OR, NOR, XOR, and XNOR. For different cases of logic operation C, we calculate the maximum MSEs of the outputs x-PC and y-PC under $C = 0$, and their minimum MSEs under $C = 1$, respectively, which are displayed in Table 2. Here, the maximum MSEs of the output x-PC and y-PC are defined as $\sigma_{x\ \max}$ and $\sigma_{y\ \max}$, respectively; the corresponding minimum MSEs are defined as $\sigma_{x\ \min}$ and $\sigma_{y\ \min}$, respectively. Considering that the logic outputs X and Y have the same threshold, i.e., $\sigma_x^* = \sigma_y^* = M$, for each logic operation, we find out that the threshold M needs to satisfy the following condition (See Table 2): $(\sigma_{x\ \max}, \sigma_{y\ \max})_{\max} < M < (\sigma_{x\ \min}, \sigma_{y\ \min})_{\min}$. One sees from Table 2 that $(\sigma_{x\ \min}, \sigma_{y\ \min})_{\min} = 0.1182$ and $(\sigma_{x\ \max}, \sigma_{y\ \max})_{\max} = 0.0617$. Hence we take M as 0.09. It is concluded that $X = 0$ and $Y = 0$ if $\sigma_{x\ \min}$ and $\sigma_{y\ \min}$ are no more than M; $X = 1$ and $Y = 1$ when $\sigma_{x\ \max}$ and $\sigma_{y\ \max}$ are more than M.

By performing Steps 2–4, we give the implementation of the logic AND and NAND operations, as shown in Fig. 8, where the amplitude of the external injection light varies with fast three-level signals. For $\mu = 2.0$, $K_x = 0$ ns^{-1}, $K_y = 10$ ns^{-1}, and $T = 10$ ns. Tables 3 and 4 show the combinations of input and output for logic AND and NAND operations, respectively. As seen from Fig. 8(a) and Table 2, if $C = I_1 \cdot I_2$,

Table 2. For different cases of logic operations C between I_1 and I_2, the maximum MSEs ($\sigma_{x\ \max}$ and $\sigma_{y\ \max}$) of the outputs x-PC and y-PC under $C = 0$, respectively, and their minimum MSEs, $\sigma_{x\ \min}$ and $\sigma_{y\ \min}$, under $C = 1$.

Different control	$(I_1 I_2)$ =(0, 0)			$(I_1 I_2)$ =(0, 1) /(1.0)			$(I_1 I_2)$ =(1, 1)		
logic operations	C	σ_x	σ_y	C	σ_x	σ_y	C	σ_x	σ_y
$C = I_1 \cdot I_2$	0	$\sigma_{x\ \max} = 0.0011$	$\sigma_{y\ \max} = 0.0063$	0	$\sigma_{x\ \max} = 0.0285$	$\sigma_{y\ \max} = 0.0343$	1	$\sigma_{x\ \min} = 0.1566$	$\sigma_{y\ \min} = 0.1696$
$\overline{C = I_1 \cdot I_2}$	1	$\sigma_{x\ \min} = 0.1269$	$\sigma_{y\ \min} = 0.1227$	1	$\sigma_{x\ \min} = 0.1310$	$\sigma_{y\ \min} = 0.1408$	0	$\sigma_{x\ \max} = 0.0371$	$\sigma_{y\ \max} = 0.0346$
$C = I_1 + I_2$	0	$\sigma_{x\ \max} = 0.0410$	$\sigma_{y\ \max} = 0.0591$	1	$\sigma_{x\ \min} = 0.1314$	$\sigma_{y\ \min} = 0.1406$	1	$\sigma_{x\ \min} = 0.1598$	$\sigma_{y\ \min} = 0.1690$
$\overline{C = I_1 + I_2}$	1	$\sigma_{x\ \min} = 0.1182$	$\sigma_{y\ \min} = 0.1287$	0	$\sigma_{x\ \max} = 0.0212$	$\sigma_{y\ \max} = 0.0336$	0	$\sigma_{x\ \max} = 0.0015$	$\sigma_{y\ \max} = 0.0074$
$C = I_1 \oplus I_2$	0	$\sigma_{x\ \max} = 0.0409$	$\sigma_{y\ \max} = 0.0617$	1	$\sigma_{x\ \min} = 0.1311$	$\sigma_{y\ \min} = 0.1424$	0	$\sigma_{x\ \max} = 0.0415$	$\sigma_{y\ \max} = 0.0566$
$C = I_1 \odot I_2$	1	$\sigma_{x\ \min} = 0.1182$	$\sigma_{y\ \min} = 0.1287$	0	$\sigma_{x\ \max} = 0.0285$	$\sigma_{y\ \max} = 0.0342$	1	$\sigma_{x\ \min} = 0.1566$	$\sigma_{y\ \min} = 0.1696$

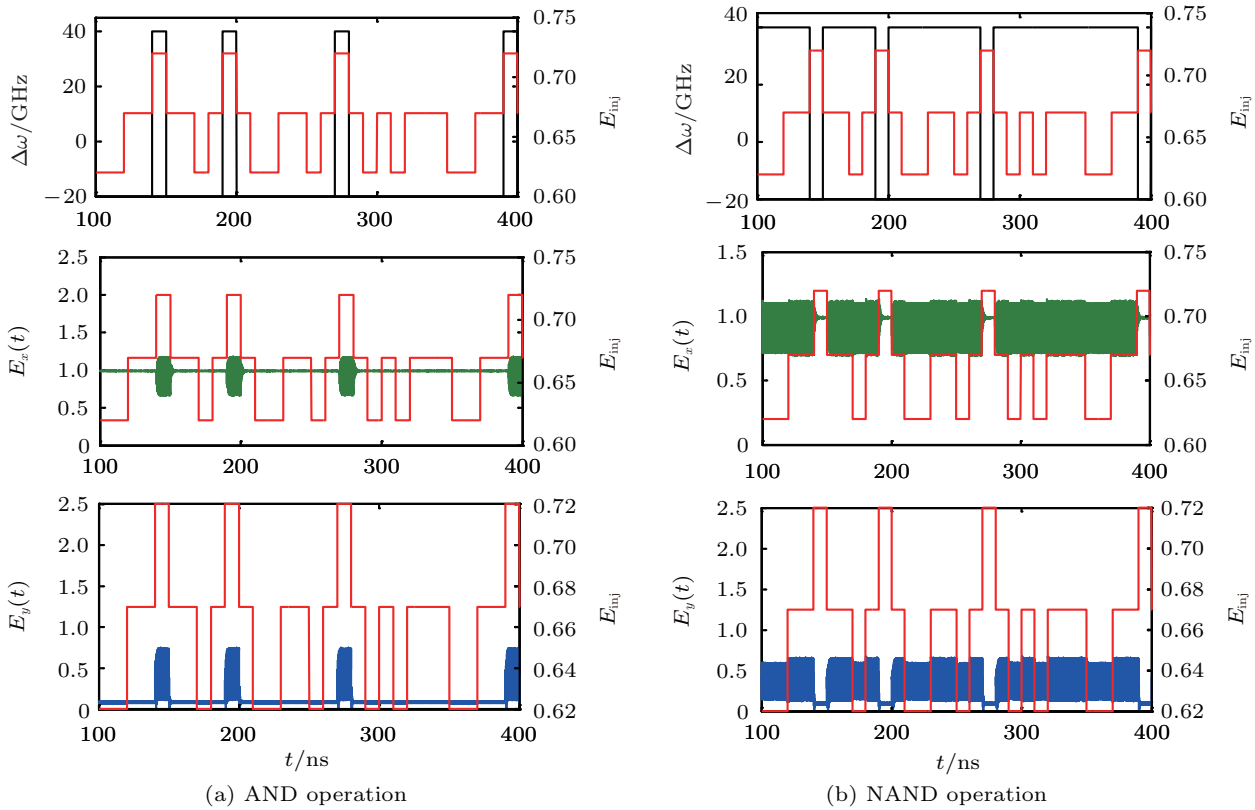


Fig. 8. (color online) Logic AND and NAND operations, for $\mu = 2.0$, $K_x = 0$ ns^{-1}, $K_y = 10$ ns^{-1}, and $T = 10$ ns; the black solid-line: frequency detuning $\Delta\omega$ (control logic signal); the blue line: the y-PC; bottle green line: the x-PC; the red solid line: three-level signals.

Table 3. Combinations of input and output for logic AND operation. The logic inputs are encoded with the amplitude of the optically injected field; the logic output X is decoded with the difference between the MSEs of the x-PC and its threshold; the output Y is decoded with the difference between that of the y-PC and its threshold.

$E_{\rm inj}(I_1, I_2)$	Control logic signal C	Threshold judgment	AND gate: logic output X	AND gate: logic output Y
$E_{\rm inj\ I}(0,0)$	0	$\sigma_{x\ \rm max} < M$; $\sigma_{y\ \rm max} < M$	0	0
$E_{\rm inj\ II}(0,1)$	0	$\sigma_{x\ \rm max} < M$; $\sigma_{y\ \rm max} < M$	0	0
$E_{\rm inj\ II}(1,0)$	0	$\sigma_{x\ \rm max} < M$; $\sigma_{y\ \rm max} < M$	0	0
$E_{\rm inj\ III}(1,1)$	1	$\sigma_{x\ \rm min} > M$; $\sigma_{y\ \rm min} > M$	1	1

Table 4. Combinations of input and output for logic NAND operation.

$E_{\rm inj}(I_1, I_2)$	Control logic signal C	Threshold judgment	NAND gate: logic output X	NAND gate: logic output Y
$E_{\rm inj\ I}(0, 0)$	1	$\sigma_{x\ \rm min} > M$; $\sigma_{x\ \rm min} > M$	1	1
$E_{\rm inj\ II}(0, 1)$	1	$\sigma_{x\ \rm min} > M$; $\sigma_{y\ \rm min} > M$	1	1
$E_{\rm inj\ II}(1, 0)$	1	$\sigma_{x\ \rm min} > M$; $\sigma_{y\ \rm min} > M$	1	1
$E_{\rm inj\ III}(1, 1)$	0	$\sigma_{x\ \rm max} < M$; $\sigma_{y\ \rm max} < M$	0	0

$\sigma_{x\ \rm max} = 0.0285$ and $\sigma_{y\ \rm max} = 0.0343$ when $(I_1, I_2) = (0,0)$, $(I_1, I_2) = (0,1)$, and $(I_1, I_2) = (1,0)$. It is obtained that $X = 0$ and $Y = 0$, owing to the fact that $\sigma_{x\ \rm max} < M$ and $\sigma_{y\ \rm max} < M$; if $(I_1, I_2) = (1,1)$, $\sigma_{x\ \rm min} = 0.1566$ and $\sigma_{y\ \rm min} = 0.1696$. We obtain $X = 1$ and $Y = 1$ since $\sigma_{x\ \rm min} > M$ and $\sigma_{y\ \rm min} > M$. As a result, $X = I_1 \cdot I_2$ and $Y = I_1 \cdot I_2$. This means that logic AND operation can be implemented successfully when $C = I_1 \cdot I_2$. From Fig. 8(b) and Table 4, it is seen that the two logic outputs are both logic NAND operations when C has NAND operation between the two logic outputs, i.e. $X = \overline{I_1 \cdot I_2}$, $Y = \overline{I_1 \cdot I_2}$ and when $C = \overline{I_1 \cdot I_2}$.

Logic OR, NOR, XOR, and XNOR operations are further presented in Fig. 9, and the corresponding input-output combinations, in turn, are displayed in Tables 5–8. Here, $\mu = 2.0$, $K_x = 0$ ns^{-1}, $K_y = 10$ ns^{-1}, and $T = 10$ ns. Like the implementation method of logic AND and NAND operations, the other different basic logic operations can be implemented when C meets different logic operations between two logic inputs. For example, $X = I_1 + I_2$, $Y = I_1 + I_2$ if $C = I_1 + I_2$ (see Fig. 9(a) and Table 5). From Fig. 9(b) and Table 6, it can be seen that $X = \overline{I_1 + I_2}$, $Y = \overline{I_1 + I_2}$ when $C = \overline{I_1 + I_2}$. The results given in Fig. 9(c) and Table 7 further show that $X = I_1 \oplus I_2$ and $Y = I_1 \oplus I_2$ when $C = I_1 \oplus I_2$. Finally, $X = I_1 \odot I_2$ and $Y = I_1 \odot I_2$, owing to the case that $C = I_1 \odot I_2$ (see Fig. 9(d) and Table 8.)

The above analyses show that different logic operations, such as logic AND, NAND, OR, NOR, XOR, and XNOR, can be implemented by the control of the logic operation between C and two logic inputs. In particular, under the same control logic signal and logic inputs, two logic outputs have the same logic operations between two logic inputs.

All of the above basic logic operations are implemented under static conditions. In the following, we further demonstrate the ability of some basic reconfigurable dynamic logic operations to implement the reconfiguration, such as AND, NAND, OR, NOR, XOR, and XNOR under different values of noise strength D as shown in Fig. 10. Here, $\mu = 2.0$, $K_x = 0$ ns^{-1}, $K_y = 10$ ns^{-1}, $T = 10$ ns. From Figs. 10(a) and 10(b), it is found that when the values of D are 10^7 and 10^8, respectively, the different logic operations at different time periods can be implemented, controlling the logic operation between C and two logic inputs. For example, if $C = I_1 \cdot I_2$ when the time t is between 100 ns and 200 ns, we obtain the logic AND operation, i.e., $X = I_1 \cdot I_2$ and $Y = I_1 \cdot I_2$; while t is between 200 ns and 300 ns, the logic NAND operation can be performed when $C = \overline{I_1 \cdot I_2}$, i.e.,$X = \overline{I_1 \cdot I_2}$, $Y = \overline{I_1 \cdot I_2}$; with t varying from 300 ns to 400 ns, $X = I_1 + I_2$ and $Y = I_1 + I_2$ if $C = I_1 + I_2$, the logic outputs are logic OR operation; In the case that $C = \overline{I_1 + I_2}$, the two logic outputs are of logic NOR operation, i.e., $X = \overline{I_1 + I_2}$, $Y = \overline{I_1 + I_2}$, and when 400 ns$\leq t \leq$ 500 ns; If $C = I_1 \odot I_2$, they are converted into the XNOR operation, i.e., $X = I_1 \odot I_2$, $Y = I_1 \odot I_2$ in the time period from 500 ns to 600 ns. Finally, with t being between 600 ns to 700 ns, the logic outputs are further converted into logic XOR operation due to the fact that $C = I_1 \oplus I_2$. However, if D increases to 10^9, according to the threshold mechanism given in Step 4, there exists one error bit in logic AND, NOR and XNOR operation in turn. Consequently, these three logic operations are invalid. For example, for logic AND operation during 150 ns and 170 ns, if $(I_1, I_2) = (0,1)$, $\sigma_{x\ \rm max} = 0.2671$ and $\sigma_{y\ \rm max} = 0.2931$. Since $\sigma_{x\ \rm max} > M$ and $\sigma_{y\ \rm max} > M$, $X = 1$ and $Y = 1$, which indicates that one error bit occurs in the two logic outputs, respectively. Under this condition, it is impossible to achieve the logic AND operation. Similarly, logic operations NOR and XNOR cannot be implemented. With the value of D further increasing to 10^{10}, for an arbitrary logic operation, $\sigma_{x\ \rm min} = 0.1471$ and $\sigma_{y\ \rm min} = 0.1462$. The two logic outputs are converted into 1 because $\sigma_{x\ \rm min} > M$ and $\sigma_{y\ \rm min} > M$. This shows that all logic operations are invalid.

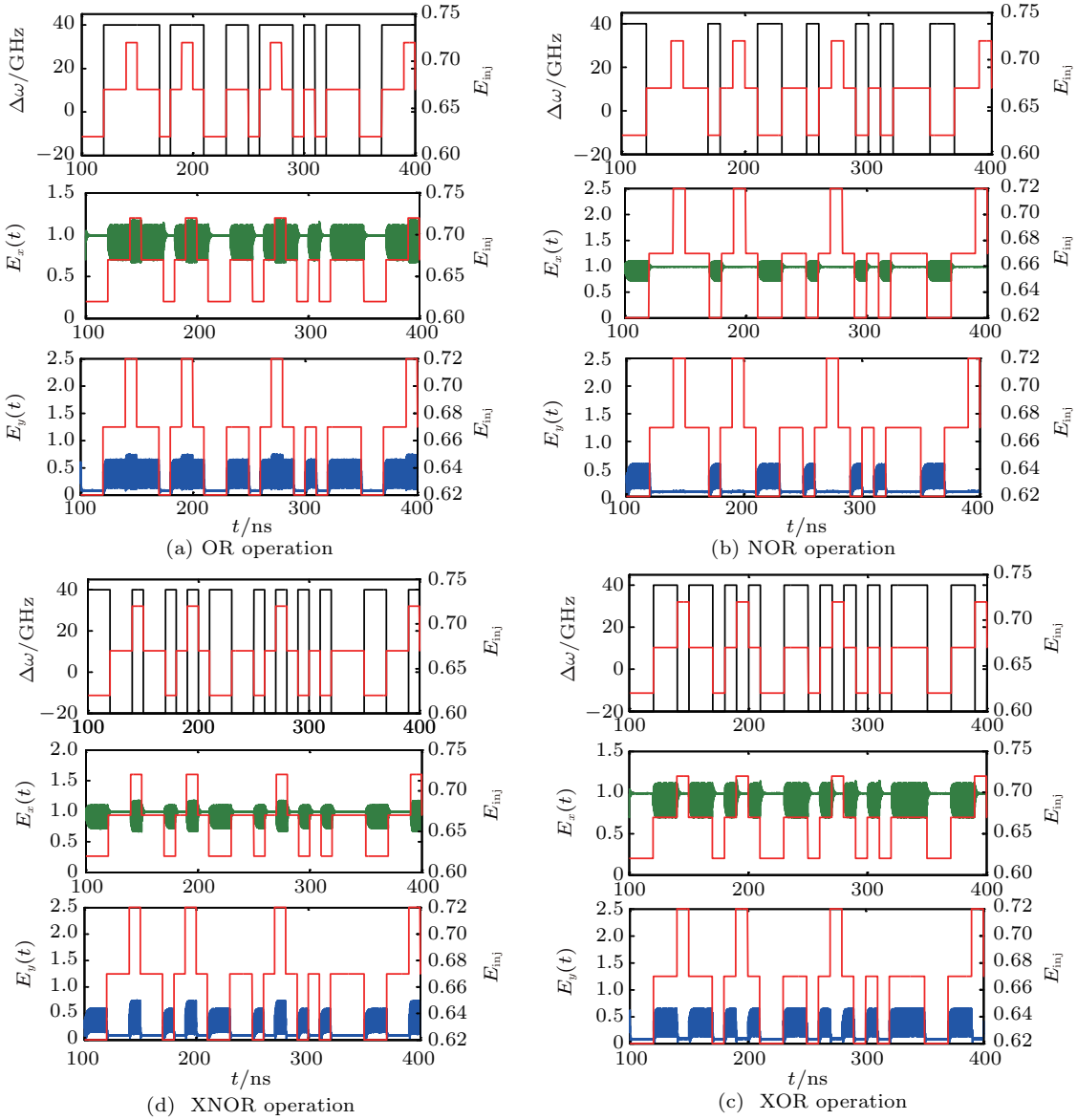


Fig. 9. (color online) Logic OR, NOR, XOR, and XNOR operations: (a) OR operation (b) NOR operation (c) XOR operation and (d) XNOR operation for $\mu = 2.0$, $K_x = 0$ ns^{-1}, $K_y = 10$ ns^{-1}, and $T = 10$ ns where the black solid-line denotes the frequency detuning (control logic signal); blue line: the y-PC; bottle green line: the x-PC; red solid line: the three-level signals.

Table 5. Combinations of input and output for logic OR operation.

$E_{inj}(I_1, I_2)$	Control logicsignal C	Threshold judgment	OR gate: logic output X	OR gate: logic output Y
$E_{inj\ I}(0, 0)$	0	$\sigma_{x\ max} < M$; $\sigma_{y\ max} < M$	0	0
$E_{inj\ II}(0, 1)$	1	$\sigma_{x\ min} > M$; $\sigma_{y\ min} > M$	1	1
$E_{inj\ II}(1, 0)$	1	$\sigma_{x\ min} > M$; $\sigma_{y\ min} > M$	1	1
$E_{inj\ III}(1, 1)$	1	$\sigma_{x\ min} > M$; $\sigma_{y\ min} > M$	1	1

Table 6. Combinations of input and output for logic NOR operation.

$E_{inj}(I_1, I_2)$	Control logic signal C	Threshold judgment	NOR gate: logic output X	NOR gate: logic output Y
$E_{inj\ I}(0, 0)$	1	$\sigma_{x\ min} > M$; $\sigma_{y\ min} > M$	1	1
$E_{inj\ II}(0, 1)$	0	$\sigma_{x\ max} < M$; $\sigma_{y\ max} < M$	0	0
$E_{inj\ II}(1, 0)$	0	$\sigma_{x\ max} < M$; $\sigma_{y\ max} < M$	0	0
$E_{inj\ III}(1, 1)$	0	$\sigma_{x\ max} < M$; $\sigma_{y\ max} < M$	0	0

Table 7. Combinations of input and output for logic XOR operation.

$E_{inj}(I_1, I_2)$	Control logic signal C	Threshold judgment	XOR gate: logic output X	XOR gate: logic output Y
$E_{inj\ I}(0, 0)$	0	$\sigma_{x\ max} < M$; $\sigma_{y\ max} < M$	0	0
$E_{inj\ II}(0, 1)$	1	$\sigma_{x\ min} > M$; $\sigma_{y\ min} > M$	1	1
$E_{inj\ II}(1, 0)$	1	$\sigma_{x\ min} > M$; $\sigma_{y\ min} > M$	1	1
$E_{inj\ III}(1, 1)$	0	$\sigma_{x\ max} < M$; $\sigma_{y\ max} < M$	0	0

Table 8. Combinations of input and output for logic XNOR operation.

$E_{\text{inj}}(I_1, I_2)$	Control logic signal C	Threshold judgment	XNOR gate: logic output X	XNOR gate: logic output Y
$E_{\text{inj I}}(0, 0)$	1	$\sigma_{x\ \min} > M; \sigma_{y\ \min} > M$	1	1
$E_{\text{inj II}}(0, 1)$	0	$\sigma_{x\ \max} < M; \sigma_{y\ \max} < M$	0	0
$E_{\text{inj II}}(1, 0)$	0	$\sigma_{x\ \max} < M; \sigma_{y\ \max} < M$	0	0
$E_{\text{inj III}}(1, 1)$	1	$\sigma_{x\ \min} > M; \sigma_{y\ \min} > M$	1	1

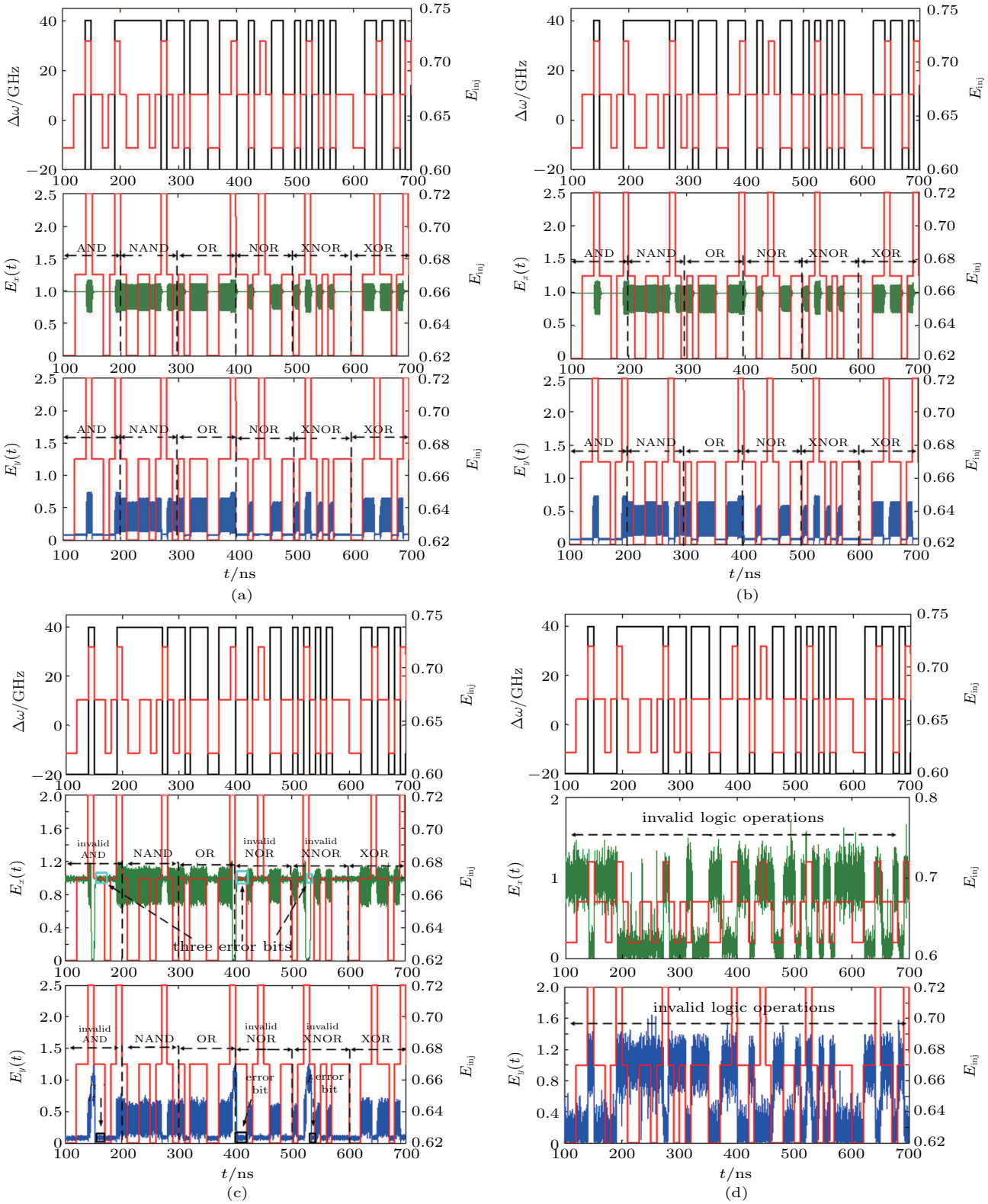


Fig. 10. (color online) For different values of noise strength D, the dynamic logic AND, NAND, OR, NOR, XOR, and XNOR operations, for $\mu = 2.0$, $K_x = 0\ \text{ns}^{-1}$, $K_y = 10\ \text{ns}^{-1}$, $T = 10\text{ns}$, and $D = 10^7$ (a), 10^8 (b), 10^9 (c), and 10^{10} (d). Black solid line represents the frequency detuning $\Delta\omega$ (control logic signal) blue line the y polarization bottle green line the x polarization red solid line the three-level signals.

4. Conclusions

According to the chaotic system in an optically injected VCSEL, we propose a novel implementation scheme for reconfigurable dynamic AOCLOs by using the threshold mechanism and the PB evolution. Here, the frequency detuning between the tunable SG-DBR laser and the VCSEL is considered as a control logic signal. For different key parameters such as the injection current, the injected strength and the frequency detuning, we discuss the dynamic evolutions of the PB with the optically injected amplitude when the output of the VCSEL is in chaotic state. According to the evolutions, we find out an appropriate value of the control logic signal, and further explore the implementation methods of AOCLOs. The different AOCLOs, such as logic AND, NAND, OR, NOR, XOR, and XNOR, can be implemented, owing to the fact that the control logic signal meets different logic operations between two logic inputs. It is noted that with the same control of logic and logic inputs, two logic outputs have the same logic operation. In addition, the conversion among different logic operations can be realized under relatively low noise strength of the spontaneous emission, controlling the logic operation between the control logic signal and two logic inputs in different time periods. These results can be generally used in all-optical digital chaotic combinational logic operations, such as all-optical chaotic adder, decoder, etc. Also it is possible that the logic operation system with high speed, security and low power cost can be implemented based on the results presented in this paper.

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