A phenomenological memristor model for synaptic memory and learning behaviors

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(Received 18 March 2017; revised manuscript received 4 July 2017; published online 30 September 2017)

Properties that are similar to the memory and learning functions in biological systems have been observed and reported in the experimental studies of memristors fabricated by different materials. These properties include the forgetting effect, the transition from short-term memory (STM) to long-term memory (LTM), learning-experience behavior, etc. The mathematical model of this kind of memristor would be very important for its theoretical analysis and application design. In our analysis of the existing memristor model with these properties, we find that some behaviors of the model are inconsistent with the reported experimental observations. A phenomenological memristor model is proposed for this kind of memristor. The model design is based on the forgetting effect and STM-to-LTM transition since these behaviors are two typical properties of these memristors. Further analyses of this model show that this model can also be used directly or modified to describe other experimentally observed behaviors. Simulations show that the proposed model can give a better description of the reported memory and learning behaviors of this kind of memristor than the existing model.

Keywords: memristor model, forgetting effect, transition from short-term memory (STM) to long-term memory (LTM), learning-experience behavior

PACS: 85.35.–p, 73.43.Cd, 87.19.lv **DOI:** 10.1088/1674-1056/26/11/118501

1. Introduction

The memristor has been treated as a promising candidate for building bio-inspired neuromorphic systems since its properties are similar to the memory and learning functions in biological systems which have been observed and reported in the experimental studies of memristors fabricated by different materials.[1–13] Table 1 gives some commonly reported properties with their experimental details in those experimental studies. The forgetting behavior and the transition from short-term memory (STM) to long-term memory (LTM) are two typical properties of this kind of memristor.

Table 1. Memory and learning behaviors observed in the experimental studies of different memristors.

Memristors	Forgetting effect		Transition from STM to LTM					Learning-experience behavior		P process + N process	
	Fitting function	Reading voltage	Report of this behavior (method)[a)]	Pulse's duration/ amplitude	Number of pulses	Forgetting time	Saturation of time constant	Report of this behavior	Number of pulses during first stimulating /restimulating	Report of this behavior	Existence of big gap
WO_x[1]	SEF	0.5 V	Yes (I)	0.4 ms/1.3 V	5–40	60 s	Yes	No	–	No	–
WO_{3-x}[4]	EF	∼0.5 V	Yes (II)	0.5 s/2.8 V	9	5 s	No	Yes[c)]	–	Yes	Yes
α-IGZO[5]	EF	3 V	Yes (I)	20 ms/5 V	10–150	70 s	Yes	Yes	100/4	Yes	Yes
Ag_2S[6]	$I = bt^{-m}$	∼13 mV	Yes (II)	0.5 s/80 mV	12	4 s	Yes	No	–	No	–
Ag/PEDOT:PSS/Ta[7]	EF	1.2 V	Yes (I)	–	5–50	60 s	No	Yes	50/6	Yes	Yes
PVA[8]	EF	–	Yes (I)	0.3 s/0.5 V	50–300	60 s	–	No	–	Yes	No
OTP[9][b)]	EF	–0.75 V	Yes (I)	0.2 s/−2 V	5–30	30 s	No	Yes[c)]	–	No	–
Ta/EV$(ClO_4)_2$/BTP-F/Pt[10]	EF	0.2 V	Yes (I)	10 ms/1 V	10–60	60 s	No	Yes	40/9	Yes	No
Ta/EV$(ClO_4)_2$/TPA-PI/Pt[11]	–	0.2 V	Yes (II)	10 ms/0.5 V	6	800 ms	–	Yes	80/11	Yes	No
Cu/Cu_2S/Pt[12]	EF	∼10 mV	Yes (II)	0. 5 s/0.1 V	4	10 s	No	No	–	No	–
Cu/PEDOT:PSS/Ta[13]	EF	–	Yes (I)	–	10–70	60 s	No	No	–	Yes	Yes

The notation "–" implies that in that paper the related experiment or analysis was not discussed, or related experimental details were not reported.

The notation "∼" before a figure implies that the exact figure was not reported, and the figure behind "∼" is estimated based on the reported experimental curves.

[a)] In this column, (I) and (II) give the experimental methods used in each study. The details of the two experimental methods are introduced in the Introduction.

[b)] Reference direction for voltage in Ref. [9] is different from that in other literatures. In Ref. [9], the applied negative voltage would lead to the increase of the memductance.

[c)] A behavior called "learning-experience behavior" was reported in Refs. [4] and [9], but the experimental details of such a behavior in these two literatures were different from those in Refs. [5], [7], [10], and [11].

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Similar to the memory in biological systems, the memory of this kind of memristor can be forgotten. In those reported experiments, the increase and decrease of the memductance (conductance of a memristor) would normally be regarded as the formation and loss of the memory of the device, and the voltage applied to the memristor is regarded as the input stimulation. When the memristor is stimulated by repeated positive pulses, its memductance would gradually increase, and the memory is gradually formed. After the stimulation is removed, its memductance would decrease, and the memory of the device is gradually forgotten. The memductance of the device at the end of the forgetting process would be larger than that at the beginning of the stimulating process. In those reported experiments, the decrease of the memductance during the forgetting process was reflected by the decrease of the current when a low positive voltage, called the reading voltage, was applied to the memristor, so those experimentally reported forgetting curves describe the variation of the current I with respect to time t during the forgetting process. The forgetting curves in those experiments can be well fitted by an exponential function (EF),[4–11,13] which is defined as

$$I = I_0 + A_{\mathrm{EF}} \exp(-t/\tau), \tag{1}$$

or a stretched exponential function (SEF),[1–3] which is defined as

$$I = A_{\mathrm{SEF}} \exp(-(t/\tau)^{\alpha}), \tag{2}$$

or some other functions with the curve shape that is similar to the curve shape of either EF or SEF.[12] In Eqs. (1) and (2), I_0, A_{EF}, and A_{SEF} are all not negative, and $\tau > 0$ is the time constant of the forgetting curve; in Eq. (2), $\alpha \in (0,1)$ is the stretch index.

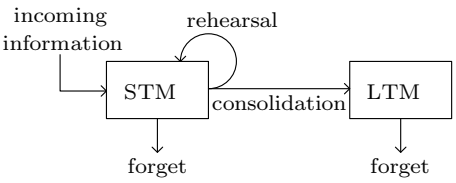


Fig. 1. Schematic illustration of the memory model in psychology.

The STM-to-LTM transition is another commonly observed behavior in the experimental studies of this kind of memristor. The concepts of STM and LTM come from the memory model in psychology proposed in 1968 by Atkinson and Shiffrin.[1,10,11] Figure 1 shows a simplified illustration of this memory model. The STM would be quickly forgotten, and the LTM would exist for a much longer time. Repeated rehearsals would lead to the transition from the STM to LTM. The forgetting behavior introduced above implies that the memory of this kind of memristor includes a quickly forgotten part, which is the STM of the device, and a long lasting part, which is the LTM of the device. Those reported experiments also show that more applied pulses would lead to a slower forgetting speed of STM and a higher level of LTM, which indicates that repeated stimulations would lead to the STM-to-LTM transition. Two experimental methods were used in those studies to observe this behavior: in some reported experiments, the STM-to-LTM transition was observed by comparing the forgetting curves after different numbers of pulses were applied; in the other experiments, this property was observed by comparing the memductance variations during the pulse-to-pulse interval as the intervals in those experiments were long enough for the observation of the forgetting behavior. In Table 1, the observation method is labeled (I) if the former method was used in the experiment. For those studies, the number of pulses gives the minimum and maximum number of the applied pulses, and the forgetting time gives the length of the forgetting period. The observation method is labeled (II) if the latter method was used. For those studies, the number of pulses gives the total number of the applied pulses, and the forgetting time gives the length of the pulse-to-pulse interval.

Besides the forgetting effect and the STM-to-LTM transition, some other properties have also been observed in those experimental studies. In biological systems, the relearning of a forgotten thing would be much faster and easier than the learning of the same thing for the first time. A similar learning-experience behavior has also been reported in some experimental studies of this kind of memristor. In this experiment, the memory of the device is first created by stimulating the memristor with repeated pulses, and then the pulses are removed for a period of time so that the memory is gradually forgotten. When the memristor is restimulated by pulses after the forgetting process, to make the memductance rise from the level at the end of the forgetting process to the highest level that has been reached during the former stimulating process, pulses used in the restimulating process are much fewer than those used in the former stimulating process. After the memory recovery, the memductance increase speed would be similar to that in the former stimulating process.

The variation of the memductance when the memristor is driven by a series of positive pulses (P process) followed by a series of negative pulses (N process) has also been reported in some of those studies. In this paper, this experiment is named as the "P process + N process" experiment. The memductance increases when positive pulses are applied and decreases when negative pulses are applied. There are two different kinds of results in those reported studies of such an experiment. In the results of some experiments, the memductance decreases rapidly when the first negative pulse arrives, and when the fol-

lowing negative pulses are applied, the memductance shows a continuous gradual decrease. So in those experiments, there is an obvious gap between the last state of the P process and the first state of the N process. In the results of the other experiments, there is no such an obvious gap, and the memductance just gradually decreases when the negative pulses are applied.

The mathematical model of this kind of memristor would be very important for their theoretical analysis and application design. The memristor models discussed in Refs. [14]–[19] can describe the forgetting effect, but those models cannot describe the other above-mentioned memory and learning behaviors. The forgetting term of the model proposed in Ref. [19] was modified by Chen *et al.* in Ref. [20] to describe the STM-to-LTM transition. This modification of the forgetting term also introduced a modeling method for the model design of the memristor with the behavior of STM-to-LTM transition. This modeling method was used in Ref. [21] to design a phenomenological model based on the HP memristor model.[22] Here we call a memristor model Chen's model if the design of such a model uses this modeling method. The analysis of Chen's model in Refs. [23] and [24] found that Chen's model could also describe the learning-experience behavior. In Ref. [25], Chen's model was modified to make sure that the state variables of the model could be restricted in their permissible intervals, and the mechanism analysis of this model was also discussed to explain how a model designed according to the STM-to-LTM transition can also describe the learning-experience behavior.

In our further analysis of Chen's model, we find that some behaviors of this model are different from the reported experimental observations. In this paper, a phenomenological memristor model with the above-mentioned experimentally observed memory and learning behaviors is proposed. The rest of this paper is arranged as follows. In Section 2, Chen's model is reviewed and analyzed to show that this model cannot describe some reported behaviors of this kind of memristor. In Section 3, a model is designed based on the forgetting effect. In Section 4, this model is further developed based on the behavior of the transition from STM to LTM. In Section 5, further discussion of the proposed model is given to show that this model can be used directly or modified to describe other reported experimental observations. Finally, this paper is summarized in Section 6.

2. Chen's model

Chen's model can be represented as

$$I = (1-w) f_{\text{off}}(V) + w f_{\text{on}}(V), \tag{3}$$

$$\dot{w} = \left(f(V) + \frac{\varepsilon - w}{\tau_{\text{c}}} \right) f_{\text{win}}(w, V), \tag{4}$$

$$\dot{\varepsilon} = k_{\varepsilon} f(V) f_{\text{win}}(\varepsilon, V), \tag{5}$$

$$\dot{\tau}_{\text{c}} = k_{\tau} f(V) f_{\text{win}}(\tau_{\text{c}}, V). \tag{6}$$

In Chen's model, equation (3) is the state-dependent current–voltage equation. V and I denote the voltage and the current, respectively. f_{off} and f_{on} describe the current–voltage relationships of the memristor's high-resistive state and low-resistive state, respectively. The relative weights of these two terms are determined by the state variable $w \in [0,1]$. The behavior of w is described by Eq. (4), in which f is a monotone increasing function, and $f(0) = 0$. $\varepsilon \in [0,1]$ describes the LTM of the memristor. $\tau_{\text{c}} > 0$ describes the forgetting speed. The behaviors of ε and τ_{c} are described by Eqs. (5) and (6), respectively, where k_{ε} and k_{τ} are positive coefficients. f_{win} in Eqs. (4)–(5) is the window function which limits the state variable into the interval on which the variable is defined, and this function would have little influence on the variation of a state variable if this state variable is not close to its upper or lower bound.

In our analysis of Chen's model, we find that some reported experimental observations cannot be described or explained by this model.

(i) In the reported experiments, the LTM of the memristive devices would be maintained for several days or even years, but not be forever memorized. In Chen's model, the LTM described by ε would never be forgotten since the derivative of ε is 0 when the input voltage stays at 0 V.

(ii) In the experimental studies, EF and SEF are the two most commonly used fitting functions of the forgetting curves. Figure 2 gives the curves of these two fitting functions. The forgetting curve of Chen's model would just decrease along an EF since the solution of the differential equation (4) is an EF when the input voltage is 0 V and the value of the window function is a constant, so this model cannot describe the forgetting behavior with the SEF-fitted forgetting curve.

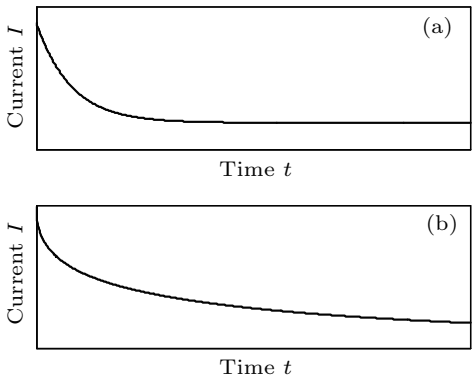


Fig. 2. Two kinds of forgetting curves: (a) EF-fitted forgetting curve, (b) SEF-fitted forgetting curve.

(iii) Chen's model was designed based on the behavior of the STM-to-LTM transition, and further analysis of Chen's model in Refs. [23]–[25] showed that this model could also describe the learning-experience behavior. Therefore, a conclusion which can be made from the analysis of Chen's model is that the learning-experience behavior is an inbuilt property

of all the memristive devices that have the property of STM-to-LTM transition. However, as shown in Table 1, not all the memristors that have the property of STM-to-LTM transition also showed the learning-experience behavior in their experimental studies, that is to say, the reported experimental results cannot provide the evidence for such a conclusion.

(iv) The learning-experience behavior described by Chen's model is not exactly the same as the experimental observations. In the reported experiments, as shown in Table 1, the number of applied pulses in the first stimulating process is several times or even tens of times higher than the number in the restimulating process. But in most reported simulations of Chen's model, as shown in Table 2, the former number is just a bit larger than the latter unless the value of τ_c remains small enough during this experiment. The simulation results in Ref. [24] seem to agree with the reported experiments, but the process of this simulation is not the same as that of those experiments: in this simulation, during the first stimulating process, 15 more pulses were applied after the memductance reached its upper bound, but in the reported experiments, the memductance just kept increasing during the first stimulating process, that is to say, the memductance in those experiments did not reach its upper bound before the end of this process. The behavior of Chen's model after the memory recovery during the restimulating process is also different from the reported experimental result. As discussed in Refs. [23] and [25], the faster memductance increase speed during the memory recovery in Chen's model is achieved by the increase of ε and τ_c, so in this model, after the memory recovery, the memductance increase speed would not slow down since ε and τ_c would not decrease.

Table 2. Reported simulation results of the learning-experience behavior of Chen's model.

Reference	[23]	[24]	[25]	
			$\tau_c(0) = 1$	$\tau_c(0) = 0.1$
Number of pulses during first stimulation	5	15	10	10
Number of pulses during memory recovery	4	3	9	5

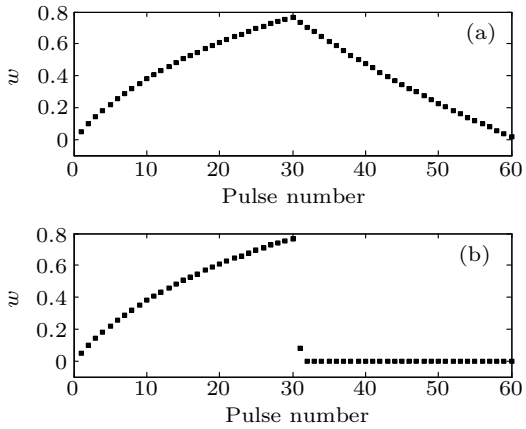


Fig. 3. The variation of w of Chen's model when the input voltage is a series of positive pulses followed by a series of negative pulses: (a) $f(V_-) = -6$, (b) $f(V_-) = -200$.

(v) As introduced in Section 1, there are two kinds of results in the reported P process + N process experiments. In our analysis of Chen's model, we find that this model can only describe the no gap case, but not the gap case. Let the amplitude of the negative pulses be $V_-(V_- < 0)$. The no gap case can be described by this model if the absolute value of $f(V_-)$ is not so large that the negative pulse induced memductance decrease is not too fast. Figure 3(a) gives the simulation of the no gap case of Chen's model when $f(V_-) = -6$. In this simulation, the input voltage consists of 30 positive pulses followed by 30 negative pulses, and the duration and interval of the applied pulses are 5 ms and 50 ms, respectively. As the variation trend of w in this model is the same as that of memductance, the variation of the memory level of the device in this simulation is reflected by the variation of w after each pulse is applied. w would just gradually decrease when each negative pulse arrives, and the first negative pulse would not lead to a rapid decrease of w. In the gap case, the memductance would decrease rapidly when the first negative pulse arrives, and then show a continuous gradual decrease when the following negative pulses are applied. In Chen's model, a large absolute value of $f(V_-)$ would lead to the rapid memductance decrease when the negative pulse arrives. Figure 3(b) gives the simulation results when $f(V_-) = -200$. The input voltage in this simulation is the same as that in the simulation of Fig. 3(a). There is an obvious gap as w shows a rapid decrease towards its lower bound when the first negative pulse arrives, but there is no continuous gradual decrease when the following negative pulses are applied since in this case w would quickly decrease to its lower bound.

The above analyses indicate that Chen's model can only describe the STM-to-LTM transition with the EF-fitted forgetting curve, and it is not general enough to describe other observed behaviors of this kind of memristor.

3. Forgetting effect

As the forgetting behavior is one typical characteristic of this kind of memristor, the design of our model will start from the analysis of the forgetting process. In this section, we would just consider the EF-fitted forgetting curve since the EF is a relatively simpler function and this function is more commonly used in the reported experiments. The SEF-fitted forgetting curve will be discussed in Section 5.

Generally a memristor model consists of a state-dependent current–voltage equation and at least one state equation. The state-dependent current–voltage equation used in our model is the same as Eq. (3) since it is a general form of the memristive current–voltage relationship.

In the experimental studies, the decrease of the memductance during the forgetting process is reflected by the decrease of the current when a constant low positive voltage $V_{\text{low}+}$ is applied to the memristor. Substituting $V = V_{\text{low}+}$ and Eq. (1) into Eq. (3), we can obtain

$$w = \frac{I_0 - f_{\text{off}}(V_{\text{low}+}) + A_{\text{EF}} \exp\left(-\dfrac{t}{\tau}\right)}{f_{\text{on}}(V_{\text{low}+}) - f_{\text{off}}(V_{\text{low}+})}. \tag{7}$$

The derivative of w with respect to time t is

$$\dot{w} = \frac{L - w}{\tau}, \tag{8}$$

where $L = [I_0 - f_{\text{off}}(V_{\text{low}+})]/[f_{\text{on}}(V_{\text{low}+}) - f_{\text{off}}\ (V_{\text{low}+})]$. We assume that the state equation of w has the same structure as Eq. (8), and this state equation is designed as

$$\dot{w} = \frac{F_w - w}{T_w}, \tag{9}$$

where $T_w > 0$ and $F_w \in [0, 1]$.

The structure of the state equation (9) and the limitation on the ranges of F_w and T_w would restrict w in [0,1]: since $T_w > 0$, $w < 0$ when $w > F_w$, and $w > 0$ when $w < F_w$, which means that the change of w is always towards F_w. So if the initial value of w is in [0,1], then w would forever be restricted in [0,1].

The current–voltage equation (3) shows that the variation of w can reflect the variation of the memductance. The above analysis of the state equation (9) shows that the variation of w follows the variation of F_w and the following speed is determined by T_w. So the designs of F_w and T_w could be based on the memductance variation observed in the experimental studies of this kind of memristor.

4. STM-to-LTM transition

The transition from STM to LTM is a commonly observed behavior of this kind of memristor. In this section, the model proposed in the previous section will be further developed to describe this behavior. The designs of F_w and T_w, which are based on the reported experimental observations of this behavior, are introduced in Subsections 4.1 and 4.2, respectively. These designs will introduce two new state variables, and the corresponding state equations are designed in Subsection 4.3. Simulations in Subsection 4.4 will show the ability of the proposed model to describe the STM-to-LTM transition. Note that in this section we still assume that the forgetting curve would decrease along an EF.

4.1. Design of F_w

The design of F_w is based on the variation trend of the memductance when different voltages are applied. The reported experimental results show that: (i) when positive pulses are applied to the memristor, the memductance increases; (ii) when the input voltage is 0 V or a low positive voltage (the reading voltage), the memductance decreases; (iii) when a negative voltage is applied to the memristor, the memductance would decrease.

These experimental results indicate that the value of F_w is not lower than w when a positive pulse arrives, and F_w is not larger than w when the applied voltage is 0 V, a low positive voltage, or a negative voltage.

Assume that the function, which describes the variation of F_w with respect to V, is a continuous function of V. Based on the above analyses, this function of V should have a "⎽⎾" shaped curve, and the obvious increase of this curve should start from a certain positive value of V. Such a function in this paper is designed as

$$F_w = f_F(V, w_{\min}, w_{\max}) = w_{\min}\,(1 - f_u(V)) + w_{\max} f_u(V), \tag{10}$$

where $0 \le w_{\min} \le w \le w_{\max} = 1$, and $f_u(V)$ is defined as

$$f_u(V) = \begin{cases} 1 - \left[1 + (a_+ V)^{b_+}\right]^{-1}, & V \ge 0, \\ 0, & V < 0, \end{cases} \tag{11}$$

where a_+ and b_+ are positive constants. Figure 4 gives the curves of F_w with respect to the applied voltage V when b_+ takes different values. In Eq. (11), a_+ determines the position where an obvious increase takes place, and b_+ determines how fast this obvious increase is.

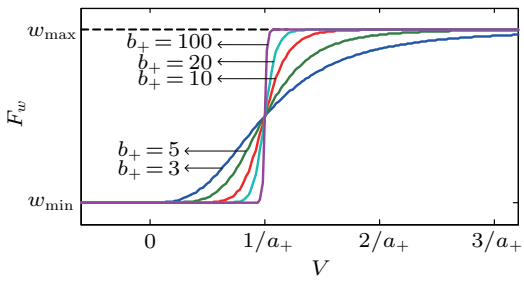


Fig. 4. (color online) Curves of F_w with respect to V.

In those experimental studies, as shown in Table 1, the forgetting curves were recorded by a reading voltage, which is lower than the amplitude of the stimulating pulses and has no obvious influence on the decrease of the memductance during the forgetting process. In our model, the reading voltage $V_{\text{low}+}$ can be defined as the positive voltage when F_w satisfies the condition

$$[F_w - w_{\min}]/[w_{\max} - w_{\min}] \le 0.0001. \tag{12}$$

Substituting Eq. (10) into Eq. (12), we can obtain

$$0 < V_{\text{low}+} \le a_+^{-1} \left[(0.9999)^{-1} - 1\right]^{b_+^{-1}}. \tag{13}$$

According to the definition of $V_{\text{low}+}$, $f_F(V_{\text{low}+}, w_{\min}, w_{\max}) \approx f_F(0, w_{\min}, w_{\max})$, which means that $F_w \approx w_{\min}$ when $V_{\text{low}+}$ is applied, so the variation trend of w when the reading voltage is applied is similar with that when the input voltage is 0 V.

During the forgetting process, w decreases towards $w_{\min}$, and at the end of this period, $w \approx w_{\min}$. In the experimental studies, more pulses in the stimulating process would lead to a larger memductance at the end of the forgetting process, so $w_{\min}$ should be a state variable which would increase when stimulating pulses are applied. As the EF-fitted forgetting curve would gradually converge to a constant value, the variation of $w_{\min}$ should be unobvious when the input voltage is 0 V or $V_{\text{low}+}$. The state equation of $w_{\min}$ will be designed in Subsection 4.3.

4.2. Design of T_w

The design of T_w is based on the rate of change of the memductance when different voltages are applied. The experimental observations show that: (i) the decrease of the memductance during the forgetting process, which takes several seconds or tens of seconds, is much slower than the memductance increase during the stimulating process, which takes only tens or hundreds of milliseconds; (ii) the memductance decrease when a negative pulse is applied is not slower than the memductance increase when a positive stimulating voltage is applied; (iii) the forgetting behavior is observed when the input voltage is 0 V or $V_{\text{low}+}$, and when the input voltage $V = 0$ V in those experiments, the actual voltage across the memristor would fluctuate around 0 V because of the low level random electrical noise.

These results imply that: (i) T_w could also be described as a function of V; (ii) the value of T_w when the positive stimulating voltage is applied should be lower than that when the low positive voltage is applied, and not lower than that when a large negative voltage is applied; (iii) the value of T_w when a relatively low negative voltage is applied is similar to that when a low positive voltage is applied.

To satisfy all these analyses, the function, which describes the variation of T_w with respect to V, should have a "⊔⊓⊔" shaped curve. Such a function of V in this paper is designed as

$$\begin{aligned} T_w &= f_T(V, \tau_{w0}, \tau_{w+}, \tau_{w-}) \\ &= \begin{cases} \tau_{w+} + (\tau_{w0} - \tau_{w+}) \left[1 + (a_+ V)^{b_+}\right]^{-1}, & V \geq 0, \\ \tau_{w-} + (\tau_{w0} - \tau_{w-}) \left[1 + (-a_- V)^{b_-}\right]^{-1}, & V < 0, \end{cases} \end{aligned} \tag{14}$$

where $0 < \tau_{w-} \leq \tau_{w+} \leq \tau_{w0}$; a_+ and b_+ are the same as those used in Eq. (11); a_-, b_-, τ_{w+}, and τ_{w-} are positive constants. Figure 5 gives the curves of T_w with respect to V when b_+ and b_- take different values. Obvious increase and decrease of T_w take place at certain negative and positive values of V, respectively. a_+ (a_-) determines the value of V at which the obvious decrease (increase) takes place, and b_+ (b_-) determines how fast the decrease (increase) is. According to the definition of $V_{\text{low}+}$, $T_w \approx \tau_{w0}$ when the input voltage is identical to $V_{\text{low}+}$.

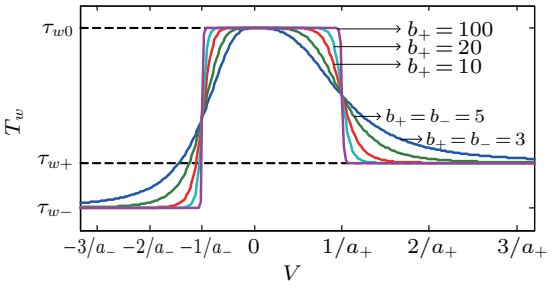


Fig. 5. (color online) Curves of T_w with respect to V.

The reported experimental results show that the time constant of the forgetting curve would be influenced by the history of the applied voltage: more stimulating pulses during the stimulating process would lead to a larger time constant of the forgetting curve. In our model, the time constant of the forgetting curve is described by T_w, and the above analysis shows that during the forgetting process $T_w \approx \tau_{w0}$. So τ_{w0} should also be a state variable, and its value depends on the history of the input voltage. The state equation of τ_{w0} will be designed in Subsection 4.3.

4.3. $w_{\min}$ and τ_{w0}

The designs of F_w and T_w in Subsections 4.1 and 4.2 introduced two new state variables, $w_{\min}$ and τ_{w0}. The corresponding state equations are designed here to describe their variations.

The analysis in Subsection 4.1 has shown that $w_{\min}$ increases when the stimulating pulses are applied and keeps almost unchanged during the forgetting process. When a negative voltage is applied, $w_{\min}$ would decrease to 0 since its upper bound w would decrease to 0. In the reported experiments, the LTM would also be forgotten, and its forgetting speed is much slower than that of the STM. In the proposed model, the LTM of the memristor is described by $w_{\min}$, so the almost unchanged variation of $w_{\min}$ during the forgetting process should be an unobvious slight decrease. The above analysis shows that the variation trend of $w_{\min}$ is similar to that of w when the same voltage is applied, so the variation of $w_{\min}$ could be described by a state equation that has the same form as Eq. (9). This state equation is designed as

$$\dot{w}_{\min} = \frac{F_{\min} - w_{\min}}{T_{\min}}, \tag{15}$$

where $F_{\min} = f_F(V, 0, w)$, $T_{\min} = f_T(V, \tau_{\min 0}, \tau_{\min +}, \tau_{\min -})$, $\tau_{\min 0}$, $\tau_{\min +}$, and $\tau_{\min -}$ are positive constants, $0 < \tau_{\min -} \leq \tau_{\min +} \leq \tau_{\min 0}$.

τ_{w0} in the proposed model can be understood as the time constant of the forgetting curve, and it describes the forgetting speed of the STM of the device. In some experiments, with the increase of the number of applied pulses, the time constant of the forgetting curve first increases, and then saturates at a certain value; in other experiments, the time constant of the forgetting curve just shows an increasing trend when the number of applied pulses increases. Those experimental studies have not reported the variation of the time constant of the forgetting curve when the negative voltage is applied. In Chen's model, it is assumed that the application of a negative voltage would lead to the decrease of this time constant. This assumption will also be used in our model. Based on the above analysis, the state equation of τ_{w0} is designed as

$$\dot{\tau}_{w0} = f_\tau(V) f_{\rm win}(\tau_{w0}, V). \tag{16}$$

In Eq. (16), f_τ describes the influence of the input voltage on the variation of τ_{w0}, and it is designed as

$$f_\tau(V) = \begin{cases} k_{\tau+}\left\{1-\left[1+(a_+V)^{b_+}\right]^{-1}\right\}, & V \geq 0, \\ -k_{\tau-}\left\{1-\left[1+(-a_-V)^{b_-}\right]^{-1}\right\}, & V < 0, \end{cases} \tag{17}$$

where a_+, b_+, a_-, and b_- are the same as those used in Eq. (14), $k_{\tau+}$ and $k_{\tau-}$ are positive constants. $f_{\rm win}$ is the window function which guarantees that the variation of τ_{w0} is in its permissible interval, and it is designed by modifying the window function proposed in Ref. [25] as

$$\begin{aligned} & f_{\rm win}(\tau_{w0}, V) \\ = \; & 0.25\{(f_{\rm s}(V)+1)[k(f_{\rm s}(\tau_{w0_\max}-\tau_{w0})+1)+2(1-k)] \\ & + (f_{\rm s}(-V)+1)(f_{\rm s}(\tau_{w0}-\tau_{w0_\min})+1)\}, \end{aligned} \tag{18}$$

where the first (second) term in curly braces determines the variation range of τ_{w0} when a positive (negative) voltage is applied; $\tau_{w0_\min}$ and $\tau_{w0_\max}$ are positive constants, $0 < \tau_{w0_\min} \leq \tau_{w0} \leq \tau_{w0_\max}$; and $f_{\rm s}$ is designed as

$$f_{\rm s}(x_{\rm s}) = \begin{cases} 1, & x_{\rm s} > 0, \\ -1, & x_{\rm s} \leq 0. \end{cases} \tag{19}$$

The value of k, which is equal to either 0 or 1, determines whether the saturation of τ_{w0} exists or not. If $k = 1$, then τ_{w0} has an upper bound $\tau_{w0_\max}$, and τ_{w0} would saturate at $\tau_{w0_\max}$ after τ_{w0} increases to $\tau_{w0_\max}$ when a positive voltage is applied. If $k = 0$, then τ_{w0} has no upper bound, and $\tau_{w0_\max}$ in this case is meaningless; the applied positive voltage would always lead to the increase of τ_{w0}.

4.4. Simulation

In the above discussion, we designed a memristor model to describe the experimentally observed behavior of the STM-to-LTM transition. This model consists of a state-dependent I–V equation (3) and three state equations (9), (15), and (16). Simulations of the proposed model are presented here to verify the ability of this model to describe such a behavior.

As discussed in Section 3, the value of the state variable w can reflect the memory level of the memristor. So in the following discussion, we will use the change of w to show the formation and loss of the memory of the device described by our model.

In the simulation, $a_+ = 2\ {\rm V}^{-1}$, $b_+ = 20$, $\tau_{w+} = 0.1$ s, $\tau_{\min+} = 0.15$ s, $\tau_{\min 0} = 10^4$ s, $k_{\tau+} = 50$, $\tau_{w0_\min} = 0.1$ s, $\tau_{w0_\max} = 20$ s. a_-, b_-, τ_{w-}, $\tau_{\min-}$, and $k_{\tau-}$ can take any value since no negative voltage will be applied in the following simulation.

The memory of the device would be gradually formed when positive pulses are applied, and the amount of memory formed in a cycle would be influenced by the duration, interval, and amplitude of the applied repeated pulses. Figure 6 gives the variation of w when the memristor is driven by 6 pulses with different duration, interval, and amplitude. The applied pulses of Fig. 6(a) are different from those of Figs. 6(b)–6(d) in the amplitude, duration, and interval, respectively. The results show that longer duration, shorter interval, and higher amplitude would lead to a larger amount of memory formed in a cycle. These results are consistent with the reported experiments.

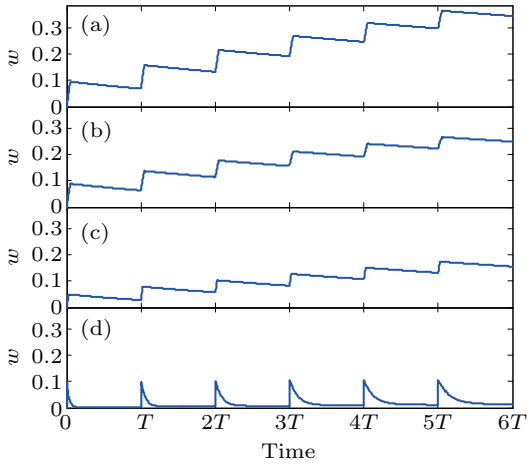


Fig. 6. (color online) The variation of w when the input voltage is 6 pulses with different duration, interval, and amplitude: (a) duration = 0.01 s, interval = 0.2 s, amplitude = 0.9 V; (b) duration = 0.01 s, interval = 0.2 s, amplitude = 0.6 V; (c) duration = 0.005 s, interval = 0.2 s, amplitude = 0.9 V; (d) duration = 0.01 s, interval = 20 s, amplitude = 0.9 V. T is the period of the applied pulse signal, T = duration+interval.

The simulation of the forgetting behavior is given in Fig. 7. In this simulation, as shown in Fig. 7(a), the memory of the device is first created by applying 30 positive pulses, the duration, interval, and amplitude of which are 5 ms, 50 ms, and 0.9 V, respectively. Figure 7(b) gives the variations of w and $w_{\rm min}$ during the first 100 s after the removal of the stimulation. During this period, w decreases at a relatively fast speed in the first 20 s, and then gradually saturates at $w_{\rm min}$; $w_{\rm min}$ shows no obvious change. The decrease of w indicates that part of the memory of the device, the STM, would be quickly forgotten, and the almost unchanged value of $w_{\rm min}$ indicates that the LTM would exist for a relatively long time.

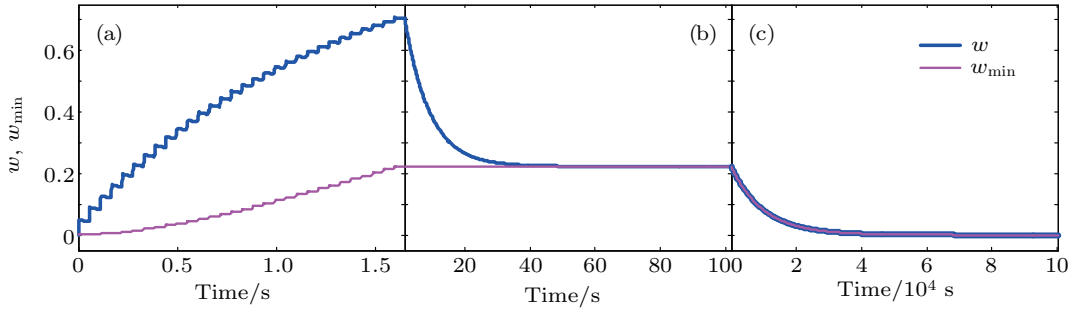


Fig. 7. (color online) Learning and forgetting behaviors. (a) The formation of memory. (b) Forgetting of STM. (c) Forgetting of LTM.

The meaning of the LTM in our model is different from that in Chen's model. As introduced in Section 2, the LTM of Chen's model would be forever memorized when $V = 0$ V, which is inconsistent with the reported experimental observations. The LTM of our model is described by $w_{\min}$, and it would also be forgotten. In our model, w and $w_{\min}$ would change towards F_w and $F_{\min}$, respectively. When $V = 0$ V, $F_{\min} = 0$ and $F_w = w_{\min}$. Figure 7(c) gives the variation of w and $w_{\min}$ after the forgetting process shown in Fig. 7(b). During this period, $w_{\min}$ decreases to 0 and w follows the variation of $w_{\min}$. The forgetting of LTM, which takes tens of kiloseconds, is much slower than the forgetting of STM, which just takes tens of seconds.

In the reported experimental studies, the forgetting curves were recorded when the memristor was applied with a reading voltage $V_{\text{low}+}$ or a series of pulses with the amplitude of such a low positive voltage. To analyze the difference between the forgetting curves of our model when the applied voltage is 0 V and $V_{\text{low}+}$, the maximum relative difference between these two forgetting curves is defined as

$$D_{\text{r}} = \frac{|w_{\text{f_low}+} - w_{\text{f_0}}|}{w_{\text{f_0}}} \times 100\%, \tag{20}$$

where $w_{\text{f_0}}$ and $w_{\text{f_low}+}$ are the values of w after the removal of the stimulation when the applied voltages are 0 V and the upper bound of $V_{\text{low}+}$, respectively. Figure 8 gives the variation of D_{r} during the forgetting process shown in Fig. 7(b). During this period, $D_{\text{r}} < 0.31\%$, so the behavior of the proposed model when $V = V_{\text{low}+}$ is almost the same as that when $V = 0$ V.

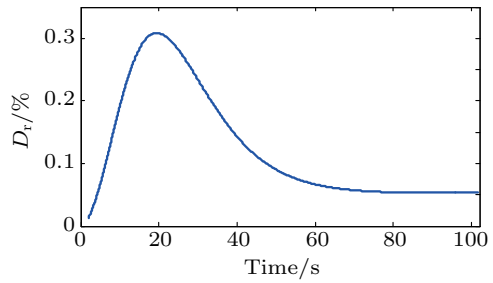


Fig. 8. (color online) The variation of D_{r} during the forgetting process.

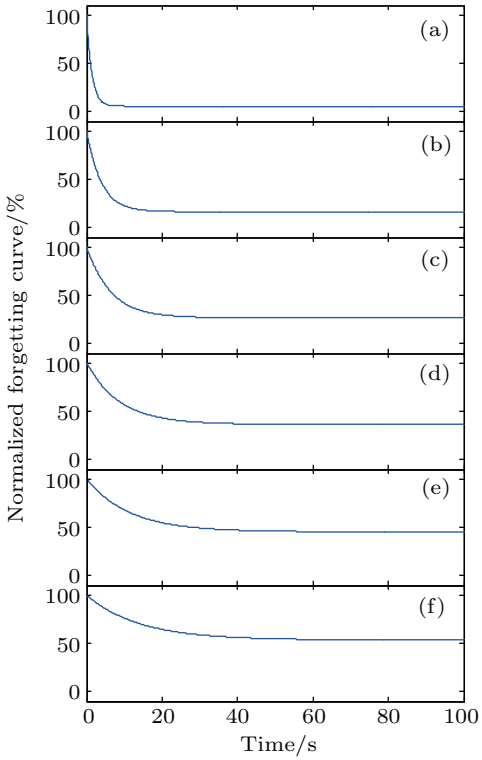


Fig. 9. (color online) The transition from STM to LTM observed by comparing the normalized forgetting curves after the memristor is stimulated by (a) 5 pulses, (b) 15 pulses, (c) 25 pulses, (d) 35 pulses, (e) 45 pulses, and (f) 55 pulses.

As introduced in Section 1, the transition from STM to LTM was observed in two different ways in those experimental studies. In most experiments, this behavior was observed by comparing the forgetting curves after the memristor was stimulated by different numbers of pulses. Simulation results of such an experiment are given in Fig. 9. The pulses used in this simulation are the same as those used in Fig. 7, and the number of the applied pulses increases from 5 to 55 in steps of 10. The normalized forgetting curves in Fig. 9 show that when more pulses are applied, the LTM accounts for a higher proportion of the memory formed during the stimulating process, and forgetting of the STM takes a longer time. The higher proportion of the LTM in our model is achieved by the increase of $w_{\min}$, and the longer forgetting time of the STM is achieved by the increase of τ_{w0}. In some other experiments, the forgetting curves were observed during the pulse-to-pulse

intervals as these intervals were long enough for the observation of the forgetting behavior. The simulation in Fig. 6(d) can be regarded as the simulation of such an experiment, and the ability of the proposed model to describe the behavior of STM-to-LTM transition could also be verified by analyzing the variation of w during each pulse-to-pulse interval in Fig. 6(d).

In our model, the variation of the time constant of the forgetting curves is described by the change of τ_{w0}, and the parameter k in the window function (18) determines whether the saturation of this time constant exists or not. Figure 10 gives the variation of τ_{w0} when k takes different values. In this simulation, the input voltage is a constant voltage $V = 0.9$ V. If $k = 0$, then τ_{w0} does not have an upper bound, and the value of τ_{w0} just continuously increases. If $k = 1$, τ_{w0} has an upper bound τ_{w0_max}; the value of τ_{w0} keeps increasing until reaching its upper bound, and then saturates at its upper bound value.

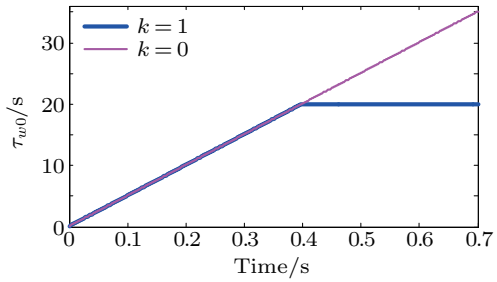


Fig. 10. (color online) The variation of τ_{w0} when k is equal to 0 or 1.

5. Other behaviors

As introduced in Table 1, besides the EF-fitted forgetting curves and the STM-to-LTM transition, the SEF-fitted forgetting curves and some other behaviors have also been observed in those experimental studies of this kind of memristor. In this section, we will show that the model proposed in the previous section can be used directly or modified to describe other experimentally observed behaviors.

5.1. SEF-fitted forgetting curve

The model design in Section 4 is based on the assumption that the fitting function of the forgetting curve is an EF. Here, we will show that this model can be modified to describe the SEF-fitted forgetting curve.

The main difference between the forgetting curves fitted by EF and SEF is that after the rapid decrease of the memductance at the beginning of the forgetting process, the EF-fitted forgetting curve would gradually converge to a constant value, while the SEF-fitted forgetting curve would still decrease at a much slower speed. The forgetting behavior of the model discussed in Section 4 could be better fitted by an EF, because during the forgetting process w would change towards $w_{\min}$, and the decrease of $w_{\min}$ is much slower than that of w, which makes $w_{\min}$ seemingly unchanged during this process. If the decrease of $w_{\min}$ is not that much slower than that of w so that the decrease of $w_{\min}$ could be observed during the forgetting process, w would first quickly decrease to $w_{\min}$ and then follow the decrease of $w_{\min}$. In this case, the SEF would be the better fitting function for the forgetting behavior.

In our model, the variation speed of $w_{\min}$ during the forgetting process is determined by $\tau_{\min 0}$. Figure 11 gives the variations of w and $w_{\min}$ during a 100-s forgetting process when $\tau_{\min 0} = 100$ s. In this simulation, the initial values of w, $w_{\min,}$ and τ_{w0} are 0.6, 0.3, and 8, respectively, and the values of the other parameters are the same as those used in the simulations in Subsection 4.4. During this period, $w_{\min}$ decreases gradually from 0.3 to 0.11; w decreases at a relatively fast speed at the beginning, and after w decreases to the value that is just a bit larger than $w_{\min}$, w follows the variation of $w_{\min}$. The SEF-fitted curve of this forgetting behavior is also given in Fig. 11, which shows that the forgetting curve (the variation curve of w) in this simulation can be well fitted by an SEF.

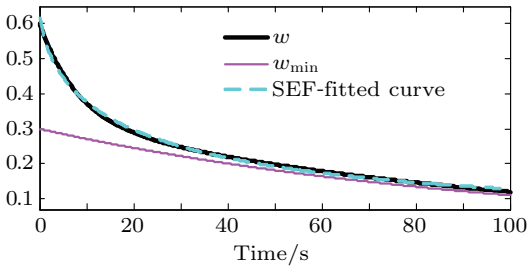


Fig. 11. (color online) SEF-fitted forgetting curve.

5.2. Learning-experience behavior

The learning-experience behavior is another behavior that has been observed in some of those experimental studies of this kind of memristor. The main character of this behavior is that the stimulation induced memristance increase during the relearning process is much faster than that during the first learning process. The model designed in Section 4 can be modified to describe this behavior.

The modification is to redesign $w_{\max}$ in Eq. (10) as a state variable. Our idea is to assume that the different speeds of increase of the memory level in the first stimulating and the restimulating processes are caused by the different values of w's upper bound $w_{\max}$: the value of $w_{\max}$ would also be influenced by the input voltage like w and $w_{\min}$; the increase speed of $w_{\max}$ when positive pulses are applied is faster than that of $w_{\min}$ and much slower than that of w; during the forgetting process, $w_{\max}$ keeps almost unchanged like $w_{\min}$ in the model with an EF-fitted forgetting curve. During the first stimulating process, w increases at a relatively slow speed, because duirng this period $w_{\max}$ is just a bit larger than w and the increase

speed of w is restricted by that of $w_{\max}$. During the forgetting process, w deceases to $w_{\min}$ and $w_{\max}$ shows no obvious change. So when the memristor is restimulated by pulses after the forgetting process, w would increase at a fast speed since $w_{\max}$ is obviously larger than w and would not restrict the increase of w. After w increases to the value that is just a bit lower than $w_{\max}$, w would follow the increase of $w_{\max}$ again like in the first stimulating process. Note that this modification would not influence the ability of the original model to describe the behavior of STM-to-LTM transition.

The above discussion shows that the variation of $w_{\max}$ is similar to the variations of w and $w_{\min}$, so the state equation of $w_{\max}$ is designed in the same form as Eq. (9):

$$\dot{w}_{\max} = \frac{F_{\max} - w_{\max}}{T_{\max}}, \tag{21}$$

where $F_{\max} = f_F(V, w, 1)$, $T_{\max} = f_T(V, \tau_{\max 0}, \tau_{\max +}, \tau_{\max -})$, $\tau_{\max 0}$, $\tau_{\max +}$, and $\tau_{\max -}$ are all positive constants, $0 < \tau_{\max -} \leq \tau_{\max +} \leq \tau_{\max 0}$.

Besides the state-dependent I–V equation (3) and three state equations (9), (15), and (16) in the original model, one more state equation (21) is introduced in the modified model with the learning-experience behavior. Figure 12 gives the simulation of this behavior. In the simulation, $\tau_{w+} = 0.005$ s, $\tau_{\max +} = 0.1$ s, $\tau_{\max 0} = 10^4$ s, and $\tau_{\max -}$ can take any value since no negative voltage is applied in this simulation; the values of the other parameters are the same as those used in Subsection 4.4; the pulses used in this simulation are the same as those used in the simulation in Fig. 7. When 30 pulses are applied to the memristor during the first stimulating process, as shown in Fig. 12(a), both w and $w_{\max}$ increase when each pulse arrives, and the increase speed of w is similar to that of $w_{\max}$. During this period, the increase of w, which can reflect the memory formation of the device, is restricted by the increase of its upper bound $w_{\max}$. When the applied pulses are removed during the 100-s forgetting process, as shown in Fig. 12(b), $w_{\max}$ keeps almost unchanged and w decreases obviously. So at the end of the forgetting process, $w_{\max}$ is obviously larger than w. When the pulses are applied again to the memristor after the forgetting process, as shown in Fig. 12(c), it only takes 3 pulses for w to rise back to the maximum value that has been reached during the former stimulating process. After w increases to the value that is just a bit lower than $w_{\max}$, the increase speed of w become slow again.

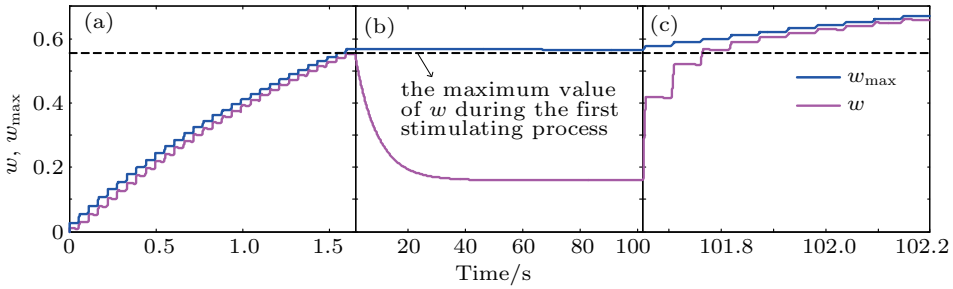


Fig. 12. (color online) Simulation of the modified model with the learning-experience behavior. (a) The first stimulating process. (b) The forgetting process. (c) The restimulating process.

Compared with Chen's model, our model can give a better description of the experimentally observed learning-experience behavior. As discussed in Section 2, in Chen's model, the learning-experience behavior has to be an inbuilt property of the memristor with the behavior of STM-to-LTM transition, but the reported experiments cannot provide the evidence for such a conclusion; the simulation results of the learning-experience behavior of Chen's model are not exactly the same as the reported experimental observations. The learning-experience behavior of our model is more consistent with the reported experimental results.

(i) In our model, the learning-experience behavior does not have to be an inbuilt property of the memristor with the behavior of the STM-to-LTM transition. The meaning of $w_{\max}$ determines whether a memristor model with the behavior of the STM-to-LTM transition also has the learning-experience behavior or not. If $w_{\max} = 1$ as discussed in Section 4, the memristor does not have the learning-experience behavior; if $w_{\max}$ is a state variable as discussed in this section, then the historical applied voltage would have an influence on the upper bound of w, and in this case, the memristor has the learning-experience behavior.

(ii) The simulation of our model shows that the number of the applied pulses in the first stimulating process is much larger than the number in the memory recovery, which is similar to those reported experimental results. In our model with the learning-experience behavior, the value of τ_{w+} determines how much faster the memory recovery is than the first memory formation. A lower value of τ_{w+} would lead to a lower number of pulses used in the memory recovery. After the memory recovery, w is just a bit lower than $w_{\max}$, so when more pulses are applied, w would again follow the increase of $w_{\max}$, which means that the variation of w at this time would be similar to that during the first stimulating process.

5.3. P process + N process experiment

In the existing studies of this kind of memristor, there are two kinds of results in the reported P process + N process experiments. The discussion in Section 2 shows that Chen's model can only describe the no gap case, but not the gap case. In this section, we will show that the model designed in Section 4 can describe both observed behaviors of this experiment.

The difference between these two kinds of results is caused by the different memductance decrease speeds in the experiments of different memristors when negative pulses are applied. In our model, this speed is determined by τ_{w-}: a larger value of τ_{w-} would lead to a slower decrease speed when the negative pulse arrives. Figure 13 gives the simulation results of such an experiment when τ_{w-} takes different values. In the simulation, $a_- = 5\ \mathrm{V}^{-1}$, $b_- = 20$, $\tau_{\min -} = 0.05$ s, $k_{\tau -} = 50$, the values of the other parameters are the same as those used in Subsection 4.4. As shown in Fig. 13(a), when the value of τ_{w-} is relatively large ($\tau_{w-} = 0.05$ s), w would decrease at a relatively slower speed when negative pulses are applied, and there is no obvious gap in the result of this experiment. When the value of τ_{w-} is not too large ($\tau_{w-} = 0.0003$ s), as shown in Fig. 13(b), w would rapidly decrease to its lower bound $w_{\min}$ when the first negative pulse arrives, and then follow the decrease of $w_{\min}$ when the following pulses are applied. So in this simulation, the first negative pulse would lead to an obvious gap between the last state of the P process and the first state of the N process, and when the following negative pulses are applied, w shows a continuous gradual decrease.

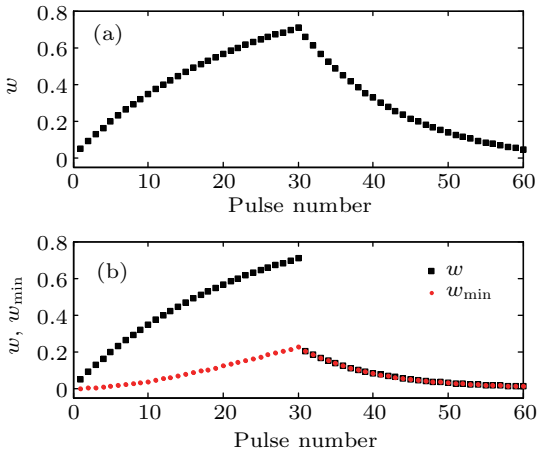


Fig. 13. (color online) Simulation results of the P process + N process experiment when τ_{w-} takes different values: (a) $\tau_{w-} = 0.05$ s, (b) $\tau_{w-} = 0.0003$ s.

6. Conclusion

A phenomenological memristor model is proposed in this paper for the memristors with memory and learning behaviors. The design of this model is based on the typical properties of this kind of memristor, i.e., the forgetting effect and the STM-to-LTM transition. Compared with Chen's model, the proposed model can give a better description of the reported memory and learning behaviors: (i) the learning-experience behavior and the meaning of LTM of our model are more consistent with the reported experimental observations; (ii) this model can be used to describe both EF and SEF fitted forgetting curves; (iii) both kinds of results observed in the reported P process + N process experiments can be described by our model.

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