Sampled-data modeling and dynamical effect of output-capacitor time-constant for valley voltage-mode controlled buck-boost converter*

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By analyzing the output voltage ripple of a buck-boost converter with large equivalent series resistance (ESR) of output capacitor, one valley voltage-mode controller for buck-boost converter is proposed. Considering the fact that the increasing and decreasing slopes of the inductor current are assumed to be constant during each switching cycle, an especial sampled-data model of valley voltage-mode controlled buck-boost converter is established. Based on this model, the dynamical effect of an output-capacitor time-constant on the valley voltage-mode controlled buck-boost converter is revealed and analyzed via the bifurcation diagrams, the movements of eigenvalues, the Lyapunov exponent spectra, the boundary equations, and the operating-state regions. It is found that with gradual reduction of output-capacitor time-constant, the buck-boost converter in continuous conduction mode (CCM) shows the evolutive dynamic behavior from period-1 to period-2, period-4, period-8, chaos, and invalid state. The stability boundary and the invalidated boundary are derived theoretically by stability analysis, where the stable state of valley voltage-mode controlled buck-boost converter can enter into an unstable state, and the converter can shift from the operation region to a forbidden region. These results verified by time-domain waveforms and phase portraits of both simulation and experiment indicate that the sampled-data model is correct and the time constant of the output capacitor is a critical factor for valley voltage-mode controlled buck-boost converter, which has a significant effect on the dynamics as well as control stability.

Keywords: buck-boost converter, valley voltage-mode control, sampled-data modeling, dynamics

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1. Introduction

Voltage ripple-based control technique, using the output ripple voltage as the pulse width modulation (PWM) ramp, is commonly used to improve the transient response of the dc–dc converter,[1] such as hysteretic control,[2] constant-on-time control,[3] V^2 control,[1,4] and so on.

The conventional V^2 control is essentially a peak V^2 control technique,[4] where an error amplifier exists between the reference voltage and the PWM comparator as shown in Fig. 1. When the output voltage of the error amplifier is varied very slowly, the output part can be represented by a fixed reference voltage. Under this assumption, the peak V^2 control can be simplified into the peak voltage-mode control. The simple control architecture, which does not require an error amplifier but still contains the advantages of the ripple-based control technique, makes the peak voltage-mode control technique popular, especially in computer or portable electronic devices.[1] According to the duality, there would exist a valley voltage-mode control technique for switching converter. The output voltage is positive for the buck converter and boost converter. However, the output voltage of the buck-boost converter is negative. Thus, this leads to meaningfully investigating whether the peak voltage-mode control or valley voltage-mode control can be applied to the buck-boost converter.

The ripple controllers, however, suffer some serious stability problems. All the voltage ripple-based controlled switching converter will become unstable and operate in a subharmonic oscillation state or chaos if the time constant (ESR times capacitance) of the output capacitor is smaller than a certain value.[3–7] Therefore, it is necessary to investigate the dynamical effect of the output-capacitor time-constant for the ripple-based controlled switching converter.

In recent years, the complex dynamical behavior of the switching converter has become a hot research topic.[5,6,8–17] By establishing a one-dimensional or two-dimensional discrete iterative map model, various nonlinear phenomena and dynamical behaviors of switching converters, with the circuit parameters varied, are extensively investigated, such as period-doubling bifurcation,[5,6] multi-periodic behaviors,[8] border collision,[6,9] subharmonic oscillation,[10] Hopf bifurcation,[11,12] time bifurcation,[13] and chaos.[14–17]

Assuming the output voltage is constant, a one-dimensional discrete iterative map model of the ripple-based

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controlled buck converter is obtained, which is simple but fails to be used to discuss the influence of output-capacitor time-constant.[5] The precise two-dimensional discrete iterative map models are obtained through solving the state equations of ripple-based controlled buck and boost converters with different operation modes.[6,18] However, the modeling process and the discrete iterative map models are rather complicated. Moreover, the corresponding eigenvalues of Jacobian and the maximal Lyapunov exponent are difficult to deduce.

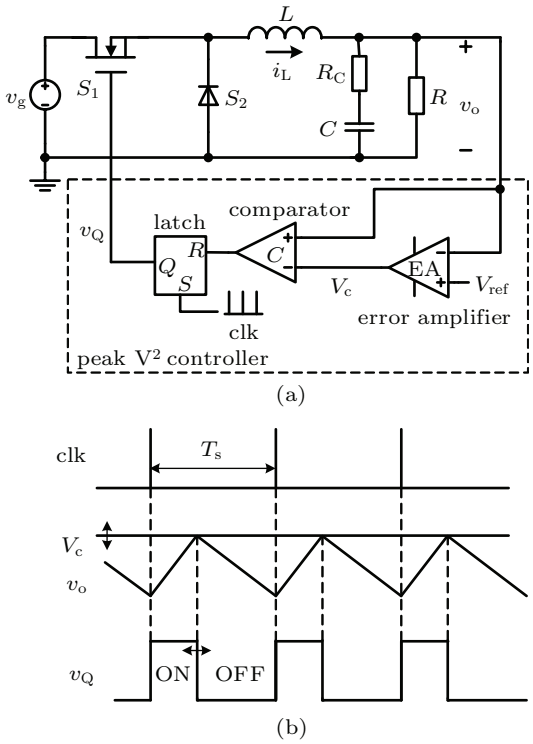


Fig. 1. (a) Peak V^2 controlled buck converter and (b) corresponding operation waveforms.

The sampled-data modeling technique combines both the continuous form of the state-space averaged model and the high-frequency accuracy of the discrete-time model, which is usually applied to stability analysis and small-signal analysis.[1,7,19] Especially in describing the responses of inductor current(s) and capacitor voltage(s) at the switching instants, the sampled-data model fits naturally with the operation of the switching regulator. Since the output ripple voltage is much smaller than output voltage in almost all practical design, which has nothing to do with the slope of the inductor current, the rising and falling slopes of the inductor current can be assumed to be constant during every switching cycle.[1] Under this assumption, various transfer functions, including control-to-output voltage transfer function, control-to-inductor current transfer function, audio-susceptibility, and output impedance, can be easily obtained through performing a small-signal analysis by sampled-data modeling.[19] Using the sampled-data modeling, the critical ESR for the stability of the valley V^2 controlled boost converter is investigated efficiently.[7] However, most of the studies focus on the small-signal analysis and stability analysis, no attention is paid to the dynamical modeling and bifurcation analysis of switching power converters.

In this paper, we will firstly investigate the possibility of a peak voltage-mode or valley voltage-mode controlled buck-boost converter and then propose its valley voltage-mode controller. In addition, a simple sampled-data modeling is performed, in which the bifurcation diagrams, the movements of eigenvalues, the Lyapunov exponent spectra, the boundary equations and the operating-state regions are used for revealing and analyzing the effect of the output-capacitor time-constant on the dynamics of the valley voltage-mode controlled buck-boost converter. Finally, circuit simulation and experimental results are provided to verify the correctness of the theoretical analysis and sampled-data model.

2. Sampled-data modeling of valley voltage-mode controlled buck-boost converter

2.1. Valley voltage-mode controlled buck-boost converter

Figure 2(a) shows a buck-boost converter, where v_g is the input voltage, v_o is the output voltage, R_C is the equivalent series resistance (ESR) of output capacitor C, v_C is the capacitor voltage, v_{ESR} is the voltage across the ESR, i_o, i_C, and i_L are load current, capacitor current, and inductor current, respectively. When the buck-boost converter operates in continuous conduction mode (CCM), its main steady-state waveforms are shown in Fig. 2(b) if the large ESR R_C is used.

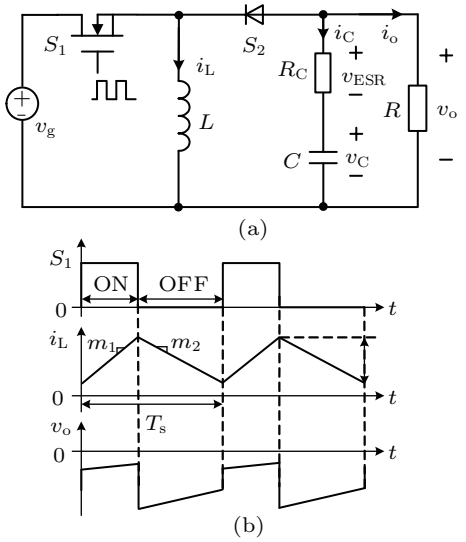


Fig. 2. (a) Buck-boost converter and (b) its steady-state waveforms with large ESR.

In Fig. 2(a), the output voltage is the sum of v_C and v_{ESR}. If large ESR R_C is used, the output voltage ripple is dominated by the ripple voltage across the ESR and thus looks piece-wise linearly. As shown in Fig. 2(b), when the switch S_1 is ON, i_L

increases with the slope of m_1 and C is discharged to supply the power to the load, which makes output voltage decrease. Due to the negative polarity of output voltage, output voltage in Fig. 2(b) exhibits negatively increasing. When the switch S_1 is OFF, i_L decreases linearly with increasing time t, C is charged, L and C supply the power to the load. In this duration, the output voltage also exhibits a negative increase due to a large ESR and the negative polarity of the output voltage. There exist two jump voltages in each switching cycle T_s because of the existence of ESR.

In the buck converter with peak voltage-mode control, the switch S_1 is turned on at the beginning of each switching cycle and turned off after the positive output voltage is increased to a control signal. For the buck-boost converter, however, after the switch S_1 is turned on, the negative output voltage increases, which means that the positive output voltage does not increase but decreases if the polarity of output voltage is inverted. Therefore, the peak voltage-mode control cannot be used for controlling the buck-boost converter. For the valley voltage-mode control, the switch S_1 is turned off at the beginning of each switching cycle and turned on after the positive output voltage decreases to a control signal. It is just the case for the buck-boost converter during the switch S_1 being in the OFF state (Fig. 2(b)) if the polarity of output voltage is inverted. Therefore, valley voltage-mode control can be applied to the buck-boost converter.

According to the polarity of the reference voltage, one valley voltage-mode controller for the buck-boost converter can be proposed. Figure 3(a) shows a valley voltage-mode controller with negative reference voltage, where the controller consists of an error amplifier, a comparator, a latch and a clock clk, K_v is the output voltage sensing coefficient ($K_v > 0$), and $-V_{ref}$ is the reference voltage ($V_{ref} > 0$). It is noted that if the reference voltage is positive, i.e., $V_{ref} < 0$, the output voltage sensing coefficient must be negative, i.e., $K_v < 0$, and the two inputs of the comparator should be interchanged. The corresponding operation waveforms are shown in Fig. 3(b). It can be seen from Figs. 3(a) and 3(b) that the output voltage is used to generate the ramp signal v_s. The control objective of the valley voltage-mode controlled buck-boost converter is to make the negative peak value of v_s follow V_{ref}.

At the beginning of every switching cycle, the clock resets the latch and makes the driver signal v_Q be low level, the switch S_1 is turned off, which causes i_L to decrease linearly from the initial value. The inductor current ripple Δi_L will flow through C when S_1 is OFF. Under the condition of large ESR, the voltage ripple of v_s is approximately equal to $K_v \Delta i_L R_C$. When v_s with negative polarity increases to V_{ref}, the output of the comparator sets the latch and makes the driver signal v_Q be high level, S_1 is turned on, which makes i_L increase and v_s (with negative polarity) increase till the end of the present switching cycle.

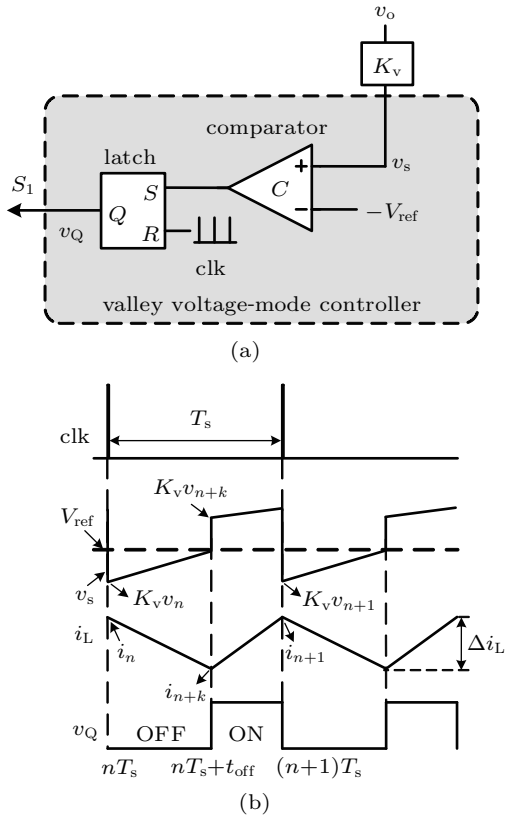


Fig. 3. (a) Valley voltage-mode controller for buck-boost converter and (b) corresponding operation waveforms.

2.2. Sampled-data modeling

To investigate the dynamics of a valley voltage-mode controlled buck-boost converter, an especial sampled-data modeling is performed by assuming that the increasing and decreasing slopes of the inductor current are constant during each switching cycle. This condition is reasonable in almost all practical designs because the output voltage ripple has a trivial influence on the slope of the inductor current. The capacitor voltage v_C and inductor current i_L at the beginning of the nth switching cycle are denoted as v_n and i_n. When the switch S_1 is turned on, inductor current i_{n+k} can be obtained easily from Fig. 3(b) as follows:

$$i_{n+k} = i_n - m_2 t_{off}, \tag{1}$$

where t_{off} is the off time duration of switch S_1 in the nth switching cycle and $m_2 = -v_o/L$ is the decreasing slope of i_L. From Fig. 2, during the off time duration of switch S_1, the capacitor current i_C is equal to $-(i_L + i_o)$. Therefore, the capacitor voltage v_{n+k} can be derived as

$$\begin{aligned} v_{n+k} &= v_n + \frac{1}{C}\int_0^{t_{off}} [-(i_n - m_2 t) - i_o]\mathrm{d}t \\ &= v_n - \frac{i_n + i_o}{C} t_{off} + \frac{m_2}{2C} t_{off}^2. \end{aligned} \tag{2}$$

Similarly, i_L and v_C at the end of the nth switching cycle can

be expressed as

$$i_{n+1} = i_{n+k} + m_1(T_s - t_{off}), \tag{3}$$

$$v_{n+1} = v_{n+k} - \frac{i_o}{C}(T_s - t_{off}), \tag{4}$$

where $m_1 = v_g/L$ is the increasing slope of i_L.

From Fig. 3(b), the sensed output voltage $v_o(n+k)$ at the turn-on instant of the switch S_1 is equal to the reference voltage V_{ref}, i.e., $K_v v_o(n+k) = V_{ref}$. Therefore, the control constraint can be expressed as follows:

$$K_v[(-i_{n+k} - i_o)R_C + v_{n+k}] = V_{ref}. \tag{5}$$

3. Dynamical analysis

3.1. Bifurcation behaviors

Significantly, it is found that instability exists in the valley voltage-mode controlled buck-boost converter when duty ratio D is less than 0.5 ($D < 0.5$), which is the same as that in the valley V^2 controlled boost converter.[6] Therefore, the dynamical analysis in this paper mainly focuses on the case of $D > 0.5$. Equations (1)–(5) constitute a complete two-dimensional sampled-data model of the valley voltage-mode controlled buck-boost converter, based on which, when input voltage $v_g = 4$ V, $V_{ref} = 0.602$ V, $K_v = 0.1$, $V_c = -0.6$ V, $T_s = 20$ μs, $L = 20$ μH, $C = 940$ μF, and $R = 3$ Ω keep constant while R_C is varied from 20 mΩ to 10 mΩ, bifurcation diagrams of inductor current and output voltage of the valley voltage-mode controlled buck-boost converter are obtained, as shown in Fig. 4.

From Fig. 4, it is shown that the valley voltage-mode controlled buck-boost converter has complex dynamical behaviors. With the decrease of R_C, the orbit of the converter is transformed from steady period-1 state to subharmonic oscillation (period-2 state), owing to the first period-doubling bifurcation at point A where $R_C = 19.2$ mΩ. As R_C gradually decreases, the converter goes from the period-2 state to the period-4 state due to the second period-doubling bifurcation at point B where $R_C = 12.25$ mΩ. From Fig. 4, it can also be known that a period-8 state region exists in the bifurcation diagram during $R_C = 11.69$ mΩ ~ 11.6 mΩ, owing to the third period-doubling bifurcation taking place at point C where $R_C = 11.69$ mΩ. As R_C decreases further, the period-8 state disappears and a chaotic orbit appears at $R_C = 11.6$ mΩ. When R_C decreases to 10.65 mΩ finally, the converter with valley voltage-mode control is invalid.

The following is analyzed in a similar way when C is taken as a bifurcation parameter. By fixing $R_C = 19$ mΩ, the inductor current bifurcation diagram can be obtained and shown in Fig. 5(a) with C changing from 500 μF to 1000 μF, as well as its output voltage bifurcation diagram drawn in Fig. 5(b).

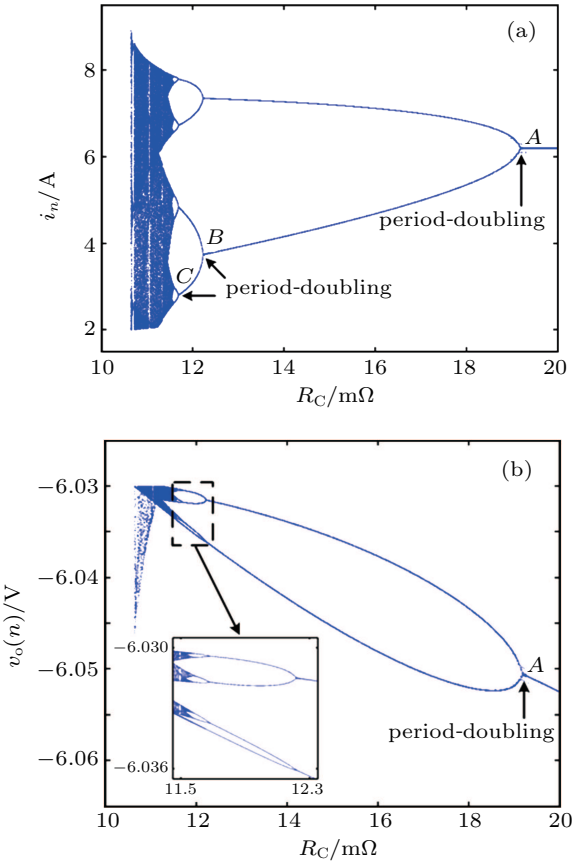


Fig. 4. (color online) Bifurcation diagrams of (a) i_L versus R_C and (b) v_o versus R_C.

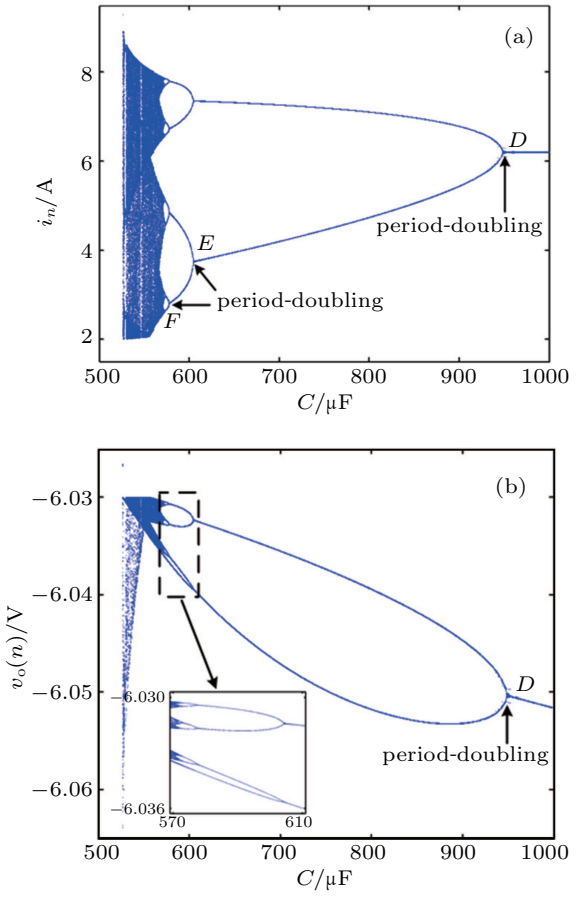


Fig. 5. (color online) Bifurcation diagrams with the variation of C: (a) i_L versus C; (b) v_o versus C.

It is found from Fig. 5 that as the output capacitor C decreases from 1000 μF to 573.9 μF, the orbit of the converter has a transition from steady period-1 state to multi-period state due to period-doubling bifurcation. With C decreasing to 573.9 μF, the orbit enters into a chaotic state. When $C \leq 526.7$ μF, the chaotic state disappears, and the voltage-mode controlled buck-boost converter is invalid. In the ranges of $C = 950.2$ μF–605.2 μF, 605.2 μF–578.3 μF, and 578.3 μF–573.9 μF, the system operates in period-2, period-4, and period-8 due to the first, the second, and the third period-doubling bifurcation, respectively, at the points D, E, and F shown in Fig. 5, where $C = 950.2$ μF, 605.2 μF, and 578.3 μF.

From the analysis above, it is shown that the valley voltage-mode controlled buck-boost converter with the variations of output-capacitor time-constant R_C and C has the same routes from stable period-1 to period-2, period-4, and period-8 via the first, the second, and the third period-doubling bifurcation, entering into chaos and ultimately being an invalid state.

3.2. Jacobian and eigenvalues

By investigating the eigenvalues of the Jacobian around the fixed point, the stability of the equilibrium state can be determined. Furthermore, by studying the movements of the eigenvalues of the Jacobian under circuit parameter variations, the stability status such as the occurrence of bifurcations and boundaries of operating regimes can be identified.

The Newton–Raphson method or other numerical algorithms[20,21] can be used to obtain the eigenvalues of Jacobian at the fixed point $\boldsymbol{X}_Q = [i_L\ v_o]^T$ by putting $x_{n+1} = x_n = \boldsymbol{X}_Q$. The Jacobian of the sampled-data model around the fixed point $\boldsymbol{X}_Q$ can be derived as

$$\boldsymbol{J}_n(\boldsymbol{X}_Q) = \left[\begin{matrix} J_{11} & J_{12} \\ J_{21} & J_{22} \end{matrix}\right]\Bigg|_{x_n = X_Q}, \tag{6}$$

where $J_{11} = \partial i_{n+1}/\partial i_n$, $J_{12} = \partial i_{n+1}/\partial v_n$, $J_{21} = \partial v_{n+1}/\partial i_n$, and $J_{22} = \partial v_{n+1}/\partial v_n$.

From Eqs. (1)–(5), J_{ij} in Eq. (6) are given as

$$\begin{aligned} J_{11} &= 1 + \frac{(m_1 + m_2)(CR_C + t_{off})}{\Delta}, \\ J_{12} &= -\frac{(m_1 + m_2)C}{\Delta}, \\ J_{21} &= -\frac{t_{off}}{C} + \frac{(i_n - m_2 t_{off})(CR_C + t_{off})}{C\Delta}, \\ J_{22} &= 1 - \frac{i_n - m_2 t_{off}}{\Delta}, \end{aligned}$$

where $\Delta = i_n + i_o - m_2(CR_C + t_{off})$.

The eigenvalues can be obtained by solving the characteristic equation in λ

$$\det[\lambda \boldsymbol{I} - \boldsymbol{J}(\boldsymbol{X}_Q)] = 0. \tag{7}$$

Based on the sampled-data model described by Eqs. (1)–(5) and the Jacobian given by Eq. (6), the bifurcation and stability characteristics of the valley voltage-mode controlled buck-boost converter can be obtained by examining the movements of the eigenvalues under the variations of the specific parameters. The movements of the eigenvalues reveal the bifurcation phenomena and the way parameter variations affect the operation of the buck-boost converter with valley voltage-mode control. If all eigenvalues of the Jacobian evaluated at

Table 1. Eigenvalues for different ESRs.

R_C/mΩ	Eigenvalues	Remarks
19.17	–0.9971, 0.4483	CCM period-1
19.18	–0.9979, 0.4480	CCM period-1
19.19	–0.9989, 0.4478	CCM period-1
19.20	**–1.0001, 0.4476**	**period-doubling bifurcation**
19.21	–1.0015, 0.4474	CCM period-2
19.22	–1.0034, 0.4473	CCM period-2

Table 2. Eigenvalues for different output capacitors.

C/μF	Eigenvalues	Remarks
950.95	–0.9986, 0.4480	CCM period-1
950.70	–0.9992, 0.4479	CCM period-1
950.45	–0.9998, 0.4477	CCM period-1
950.20	**–1.0005, 0.4476**	**period-doubling bifurcation**
949.50	–1.0012, 0.4475	CCM period-2
947.00	–1.0021, 0.4474	CCM period-2

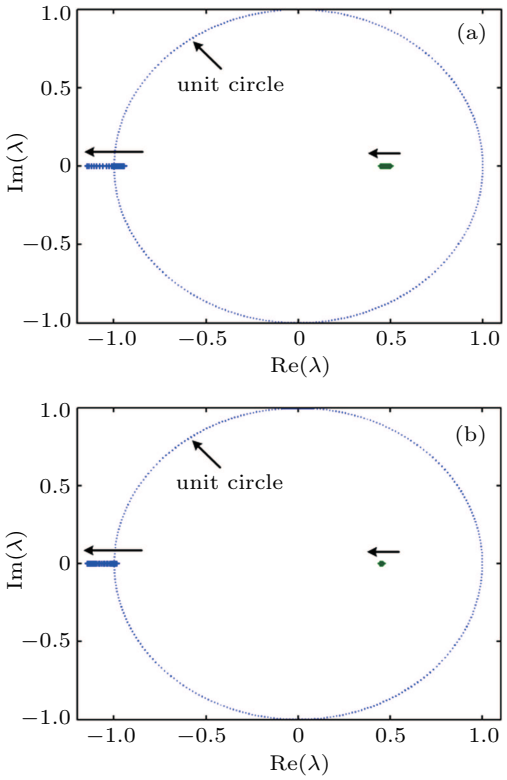


Fig. 6. (color online) Movements of eigenvalues for valley voltage-mode controlled buck-boost converter: (a) loci of eigenvalues when $C = 940$ μF and R_C varies from 19.5 mΩ to 18.9 mΩ; (b) loci of eigenvalues when $R_C = 19$ mΩ and C varies from 960 μF to 930 μF. Arrows indicate the directions of movements of the eigenvalues with decreasing R_C and C.

the fixed point are inside a unit circle, the buck-boost converter is stable. Any movements of the eigenvalues crossing from the interior of the unit circle to the exterior indicate a loss of stability of the crossing point.

Here, special attention should be paid to the loci under R_C and C variation. Listed in Tables 1 and 2 are the eigenvalues for different values of R_C and C respectively. Figure 6 illustrates the loci movements of the eigenvalues when (a) $C = 940$ μF and R_C varies from 19.5 mΩ to 18.9 mΩ and (b) $R_C = 19$ mΩ, and C varies from 960 μF to 930 μF. The arrows of the locus movements indicate the directions of movements of the eigenvalues with decreasing R_C and C.

3.3. Maximal Lyapunov exponent

The two Lyapunov exponents of the two-dimensional system are represented as[22,23]

$$\begin{bmatrix} \lambda_{m1} \\ \lambda_{m2} \end{bmatrix} = \lim_{n\to\infty} \frac{1}{n} |\mathrm{eig}(\boldsymbol{J}_n \, \boldsymbol{J}_{n-1} \, \cdots \, \boldsymbol{J}_1)| \tag{8}$$

and the maximal Lyapunov exponent is given by

$$\lambda_m = \max(\lambda_{m1}, \lambda_{m2}). \tag{9}$$

Here, $\mathrm{eig}(\boldsymbol{J}_n \, \boldsymbol{J}_{n-1} \, \cdots \, \boldsymbol{J}_1)$ is the function to obtain the eigenvalues of $(\boldsymbol{J}_n \, \boldsymbol{J}_{n-1} \, \cdots \, \boldsymbol{J}_1)$ and $\max(\lambda_{m1}, \lambda_{m2})$ is the function to acquire the maximal value between λ_{m1} and λ_{m2}.

By using Eqs. (6), (8), and (9), the maximal Lyapunov exponents corresponding to Figs. 4 and 5 are shown in Figs. 7(a) and 7(b), respectively. From Fig. 7(a), the maximal Lyapunov exponent vanishes as $R_C \leq 10.65$ mΩ, the valley voltage-mode controlled buck-boost converter is invalid. As R_C increases, the maximal Lyapunov exponent becomes positive from zero when $10.65\ \mathrm{m\Omega} < R_C \leq 11.6\ \mathrm{m\Omega}$, the converter is in a chaotic state. Compared with the scenario in the bifurcation diagram, the maximal Lyapunov exponent has dramatic changes at some points where chaotic orbits jump to the periodic orbits, which indicates that multiple periodic windows exist in the chaotic region. At the points A, B, and C shown in Fig. 7(a), where $R_C = 19.2$ mΩ, 12.25 mΩ, and 11.69 mΩ, respectively, the maximal Lyapunov exponent reaches zero from the negative, which means that the converter undergoes the period-doubling bifurcation, corresponding to the points A, B, and C of the bifurcation diagram shown in Fig. 4.

Similarly, in Fig. 7(b), when $C > 950.2$ μF, 605.2 μF$< C \leq 950.2$ μF and 578.3 μF$< C \leq 605.2$ μF, the converter is in a periodic state with CCM operation, the maximal Lyapunov exponent becomes negative. When $C = 950.2$ μF, $C = 605.2$ μF, and $C = 578.3$ μF, the maximal Lyapunov exponent equals zero, which means that the converter exhibits a period-doubling bifurcation, corresponding to the points D, E, and F of the bifurcation diagram shown in Fig. 5. In the range of 526.7 μF–573.9 μF, the maximal Lyapunov exponent changes from negative to positive, which indicates the converter is in a chaotic state. When $C \leq 526.7$ μF, the maximal Lyapunov exponent equals zero, the corresponding dynamical behavior of the buck-boost converter with valley voltage-mode control is invalid as shown in Fig. 4.

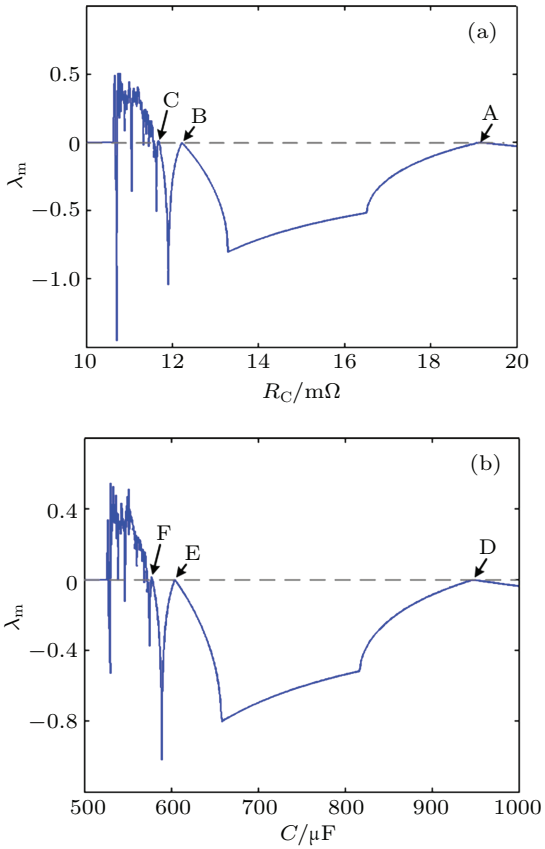


Fig. 7. (color online) Maximal Lyapunov exponents for valley voltage-mode controlled buck-boost converter when (a) R_C varies from 10 mΩ to 20 mΩ and (b) C varies from 500 μF to 1000 μF.

4. Boundary equations and operating-state regions

4.1. Boundary equations

According to the above discussion of bifurcation behavior in Subsection 3.1, it is found that the valley voltage-mode controlled buck-boost converter with the variations of R_C and C presents the same dynamical behavior, including the transition from period-doubling bifurcation to chaos, and to invalid control finally.

In Subsection 3.2, it is mentioned that the variations of eigenvalues can evaluate the parameter range of the converter working in a stable state. When the eigenvalue of first iteration map $x_{n+1} = f(x_n)$ is equal to -1, the first period-doubling bifurcation occurs and drives the system entering into period-2 from period-1.

From Eq. (7), the eigenvalues $\lambda_{1,2}$ of the characteristic equation for the sampled-data modeling can be expressed as

$$\lambda_{1,2} = 0.5(J_{11}+J_{22}) \pm 0.5\sqrt{(J_{11}-J_{22})^2+4J_{12}J_{21}}. \quad (10)$$

Hence, by putting $\min(\lambda_1,\lambda_2) = -1$ and substituting Eq. (6) into Eq. (10), the first period-doubling bifurcation boundary as well as the stability boundary τ_1 can be yielded as

$$\tau_1 : CR_C = \frac{T_s v_g^2}{2(v_o^2 - v_g^2)} - \frac{Lv_o}{Rv_g}. \quad (11)$$

Equation (11) indicates that the first period-doubling bifurcation of valley voltage-mode controlled buck-boost converter is influenced by output-capacitor time-constant (the product of R_C and C), input voltage v_g, output voltage v_o, inductance L, load resistance R, and the switching period T_s. The system will operate in the stable period-1 region when the left part of Eq. (11) is greater than the right one, i.e., the stable region is located above the boundary τ_1.

While the converter is transferred from steady period-1 state to period-2 state, the second iteration map $x_{n+2} = f(f(x_n)) = f^{(2)}(x_n)$ is existent. Similarly, making $x_{n+2} = x_n = \boldsymbol{X}_{Q2}$, the corresponding fixed point $\boldsymbol{X}_{Q2}$, the Jacobian and the eigenvalues $\lambda_{1,2}^{(2)}$ are obtained. The second period-doubling bifurcation boundary τ_2 can be obtained by letting $\min(\lambda_1^{(2)}, \lambda_2^{(2)})$ equal -1. Using the same method can obtain the third period-doubling bifurcation boundary τ_3.

As shown in Fig. 3(b), when the valley voltage-mode controlled buck-boost converter operates in OFF state, the variation of v_s is positive for the duration of $nT_s \sim (nT_s + t_{off})$. If the variation of v_s is negative for the duration of $nT_s \sim (nT_s + t_{off})$, the comparator cannot set the latch and the driver signal v_Q is always at a low level, S_1 is turned off in the whole switching period. In this condition, the convertor cannot work and the control technology is invalid. According to $v_s = K_v v_o = K_v(v_C + v_{ESR})$, we have

$$\Delta v_s = K_v(\Delta v_C + \Delta v_{ESR}) > 0. \quad (12)$$

Supposing that the peak inductor current is I_{max} during the n-th switching cycle, the inductor current at t_1 can be found to be

$$i_L = I_{max} - \frac{-v_o}{L}t_1, \quad nT_s \le t_1 + nT_s \le t_{off} + nT_s. \quad (13)$$

The output capacitor current $i_C = -(i_L + i_o)$ when S_1 is turned off, therefore the variations of v_C and v_{ESR} during $nT_s \sim (nT_s + t_1)$ are

$$\Delta v_C = \frac{1}{C}\int_0^{t_1} -(i_L + i_o)\mathrm{d}t = -\frac{t_1}{C}\left[I_{max} + i_o + \frac{v_o}{2L}t_1\right], \quad (14)$$

$$\Delta v_{ESR} = R_C \Delta i_C = -R_C\left(I_{max} + i_o + \frac{v_o}{L}t_1\right) - [-R_C(I_{max} + i_o)]$$
$$= -R_C\frac{v_o}{L}t_1. \quad (15)$$

For the buck-boost converter in CCM, the peak inductor current can be expressed as

$$I_{max} = -i_o\left(\frac{T_s}{t_{off}} + \frac{R}{2L}t_{off}\right). \quad (16)$$

Combining Eqs. (12) and (14)–(16), equation (12) can be rewritten as

$$\Delta v_s = K_v(\Delta v_C + \Delta v_{ESR})$$
$$= K_v\left[-\frac{t_1}{C}\left(-\frac{i_o T_s}{t_{off}} - \frac{i_o R}{2L}t_{off} + i_o + \frac{v_o}{2L}t_1\right) - \frac{v_o R_C}{L}t_1\right] > 0. \quad (17)$$

Because K_v is positive and v_o is negative, by considering $t_1 = t_{off}$ in the whole OFF state, equation (17) can be simplified into

$$CR_C > -\frac{v_o L}{v_g R}. \quad (18)$$

From Eq. (18), we know if the valley voltage-mode controlled buck-boost converter can work normally during one switching cycle, the output-capacitor time-constant must satisfy Eq. (18). Otherwise, the valley voltage-mode control of the buck-boost converter will be invalid. Thus, we can obtain the invalidated boundary τ_4

$$\tau_4 : CR_C = -\frac{v_o L}{v_g R}. \quad (19)$$

The valley voltage-mode control for the buck-boost converter is invalid when the left part of Eq. (19) is less than the right one. The region located below the boundary τ_4 which should be avoided in practical design, is called a forbidden region.

4.2. Operating-state regions

Considering the output-capacitor time-constant parameters with R_C = 10–20 mΩ and C = 500–1000 μF, and the other circuit parameters are chosen to be the same as those in Fig. 4, the operating-state regions of R_C and C can be obtained from Fig. 8. Figure 8(a) shows the operation spaces divided by boundary equations. The two-parameter dynamic behavior distribution divided by the sampled-data model as shown in Fig. 8(b), where the higher periodicities are depicted in grey color, the white area means low period, and the darkest shade refers to chaos.

Comparing Fig. 8(a) with Fig. 8(b), it is easily noted that the operation spaces divided by boundary equations are consistent with the regions divided by the sample data model.

There exist five operation state regions, i.e., CCM period-1, CCM period-2, CCM period-4, CCM period-8 and chaos, and the forbidden region, of the valley voltage-mode controlled buck-boost converter over the parameter space which can be divided by four stability boundaries τ_1–τ_4. The CCM period-8 and chaotic region contains a CCM period-8 region which is so weak that the change of grey level is obscure.

By choosing a horizontal line with $C = 940$ μF in Fig. 8(b), the bifurcation process will be obtained when the R_C varies among 10 mΩ–20 mΩ, which is shown in Fig. 4. In the same way, the bifurcation process while the C varies among 500 μF–1000 μF will be obtained via a vertical line with $R_C = 19$ mΩ in Fig. 8(b), the corresponding bifurcation diagrams are observed from Fig. 5. The period bifurcation points A–C in Fig. 4 and D–F in Fig. 5 are in complete agreement with the results in Fig. 8, which verifies the correctness and feasibility of operating spaces.

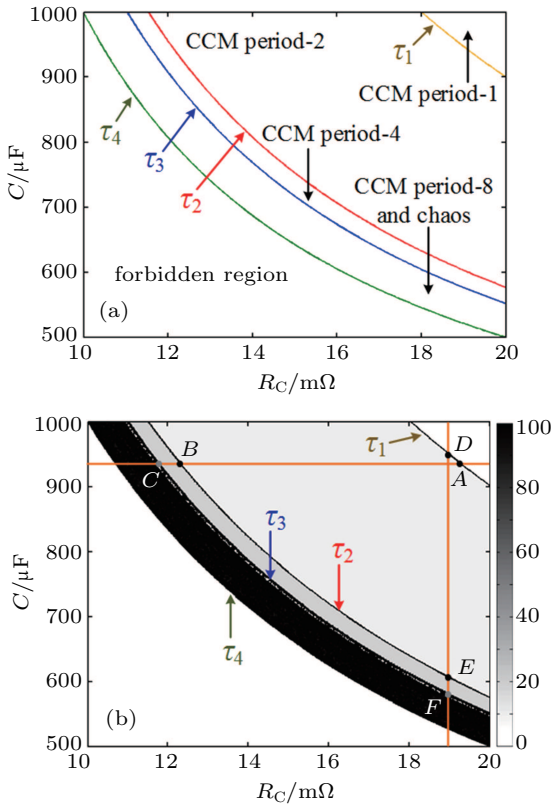


Fig. 8. (color online) Operation spaces varying with output-capacitor time-constant CR_C: (a) regions divided by boundary equations; (b) regions divided by sampled-data model.

As shown in Fig. 8, the different operation state regions of the converter can be demonstrated clearly. It is found that the system is stable when the output-capacitor time-constant CR_C is relatively large, unstable and even invalid when CR_C is small. Using such operation spaces the designer can place the nominal operating point away from behaviour boundaries, especially from the forbidden region.

5. Simulation and experimental results

5.1. Simulation waveforms

Time-domain waveforms and phase portraits are usually used to visualize nonlinear phenomena, which can also be used to validate the correctness of the sampled-data model. According to Figs. 2 and 3(a), a circuit simulation model is built by using PSIM software. The circuit parameters are chosen to be the same as those in Fig. 4. Figure 9 shows simulation results of the time-domain waveforms (steady-state output voltage, sensed output voltage, and inductor current) and the phase portraits (inductor current versus output voltage) of the valley voltage-mode controlled buck-boost converter with different ESRs.

By substituting the circuit simulation parameters into Eqs. (11) and (19), two critical output capacitor time-constants of the converter state transiting can be gained. The converter will move from steady period-1 state to period-2 state at R_C = 19.15 mΩ calculated from Eq. (11). The valley voltage-mode controlled buck-boost converter is invalid at $R_C = 10.64$ mΩ calculated from Eq. (19). When $R_C = 20$ mΩ > 19.15 mΩ, which means that the output capacitor time constant is greater than the right part of Eq. (11), the valley voltage-mode controlled buck-boost converter operates in CCM and stable period-1 state as shown in Fig. 9(a1), the output voltage of the buck-boost converter is negative and looks piece-wise linear. From Figs. 9(b1) and 9(c1), it can be seen clearly that the converter is in period-2 state with $R_C = 16$ mΩ, and in chaos with $R_C = 11$ mΩ separately. Their corresponding phase portraits are shown in Figs. 9(a2), 9(b2), and 9(c2). It can be seen that the stable state is transformed into an unstable state by using a relatively small output capacitor ESR, which is consistent with the bifurcation diagram in Fig. 4 and the operation space distribution in Fig. 8.

To validate the invalid region mentioned in bifurcation diagrams, valley voltage-mode controlled buck-boost converters with different ESRs, which operate in CCM period-1 and invalid state, are further investigated. The time-domain simulation waveforms of output voltage and inductor current under ESR variation are shown in Fig. 10. The system operates in CCM period-1 with $R_C = 20$ mΩ for the durations of 20 ms–30 ms. At time $t = 30$ ms, through changing $R_C = 10.5$ mΩ (which is smaller than 10.65 mΩ in Fig. 4, and also located in the forbidden region in Fig. 8(a)), the inductor current descends to zero quickly while the output voltage is gradually raised to zero, which means that the valley voltage-mode controlled buck-boost converter is invalid and thus the converter does not work.

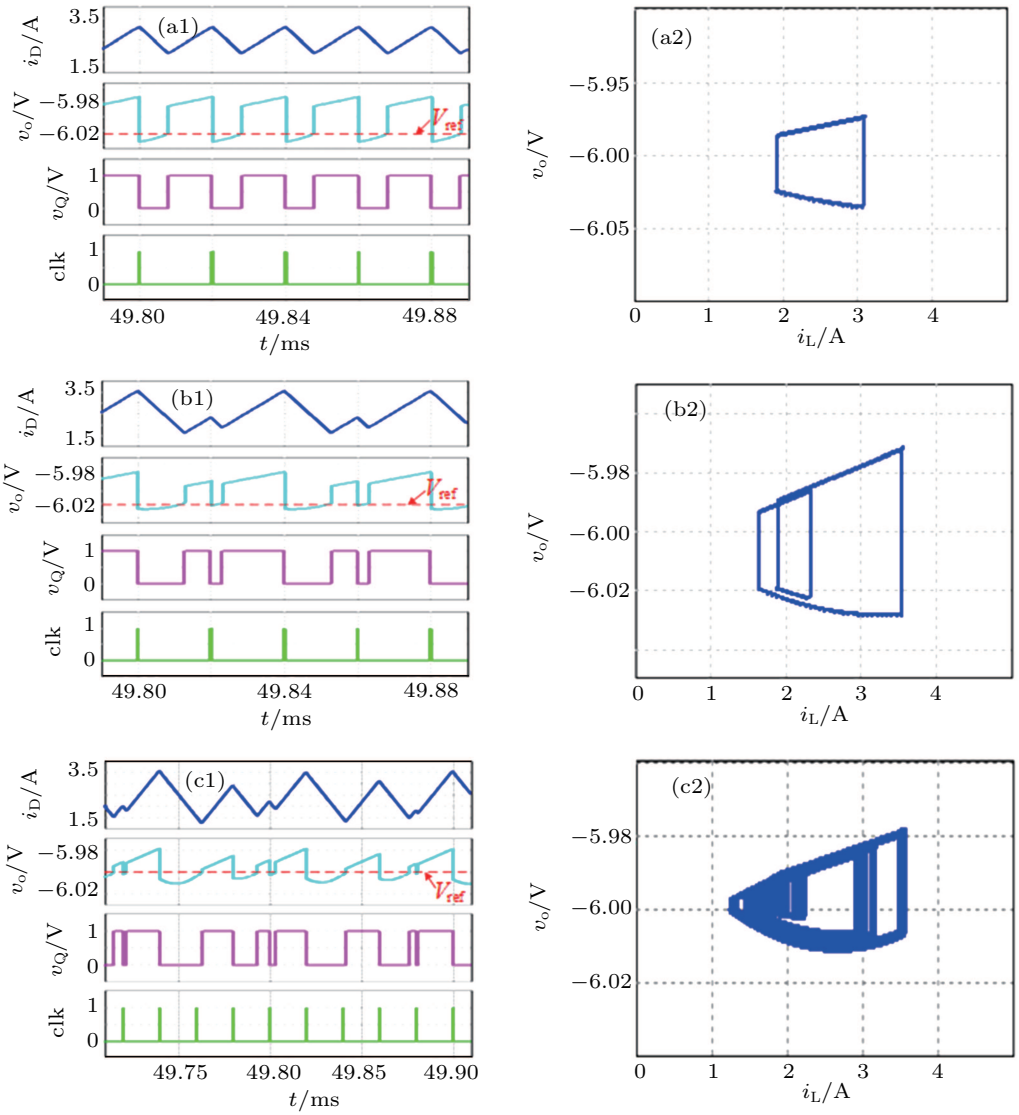


Fig. 9. (color online) Simulation results of valley voltage-mode controlled buck-boost converter with different ESRs: (a) $R_C = 20$ mΩ; (b) $R_C = 16$ mΩ; (c) $R_C = 11$ mΩ.

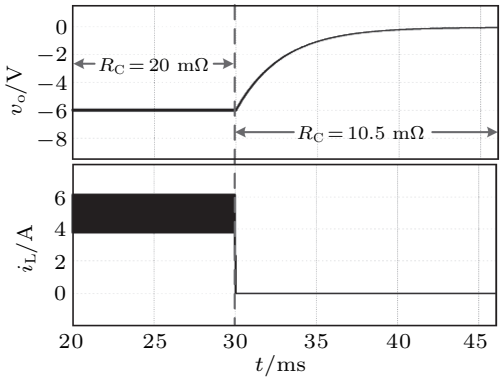


Fig. 10. Simulation waveforms of output voltage and inductor current under ESR variation.

5.2. Experimental verification

To verify the theoretical analysis and simulation results given earlier and to illustrate the effect of output capacitor time-constant, the experimental studies of the voltage-mode controlled buck-boost converter are performed with the same circuit parameters: $v_g = 4$ V, $V_{ref} = 0.602$ V, $K_v = 0.1$, $L =$ 40 μH, $C = 940$ μF, $R = 6$ Ω, and $T_s = 20$ μs. A photograph of the experimental set-up is shown in Fig. 11, where switch S_1 is the N-channel power MOSFET (IRF740), switch S_2 is the diode (ES4J), the comparator is high-speed LM319, the flip-flop latch consists of 74LS02, and the control signals are generated by the driver A3120, respectively.

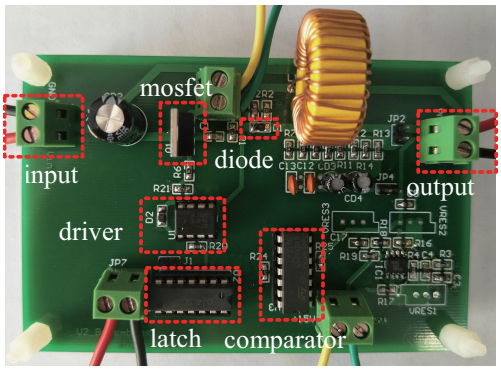


Fig. 11. (color online) Photograph of the experimental set-up.

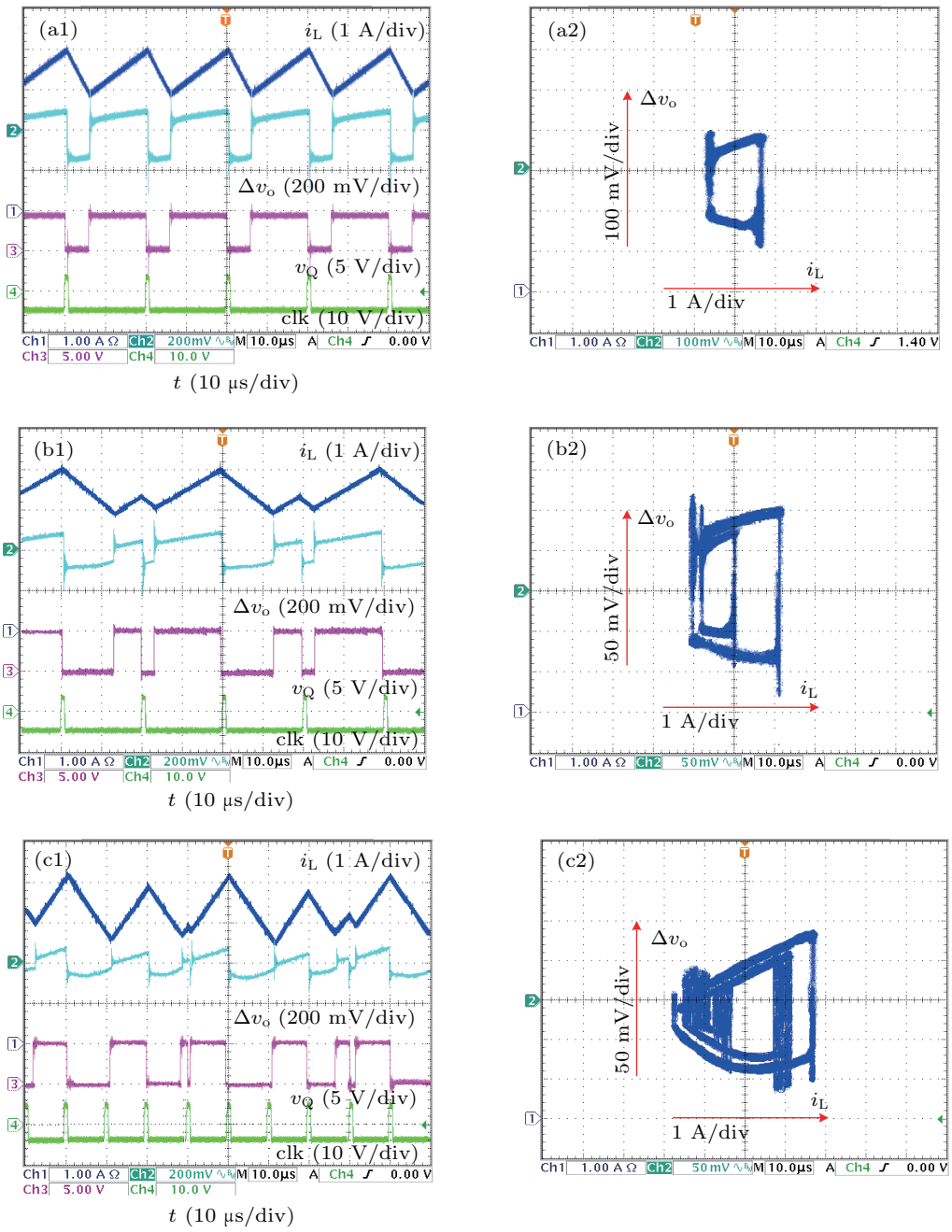


Fig. 12. (color online) Experimental results of valley voltage-mode controlled buck-boost converter with different ESRs: (a) $R_C = 20$ mΩ; (b) $R_C = 16$ mΩ; (c) $R_C = 11$ mΩ.

Figure 12(a) shows that for $R_C = 20$ mΩ, the converter operates in the period-1 state. For $R_C = 16$ mΩ and $R_C = 11$ mΩ, the converter operates in the period-2 state and chaos, as shown in Figs. 12(b) and 12(c). These experimental results are consistent with the theoretical analysis and simulation results. In hardware experiment, at the moment when the switch turns on or off, there are some spikes existing in the output voltage due to many parasitic parameters in circuit components.

6. Conclusions

The valley voltage-mode controller for the buck-boost converter is proposed in this paper. A simple sampled-data model is established to investigate the effect of output-capacitor time-constant on its dynamics through dynamical analysis. Based on the sampled-data model and eigenvalue of the corresponding characteristic equation, the bifurcation diagrams, the movement of eigenvalues, the Lyapunov exponent spectrum, the boundary equations, and the operating-state regions of output-capacitor time-constant CR_C are obtained. With the R_C and C gradually decreasing, the buck-boost converter in CCM has the same route from stable period-1 to period-2, period-4, and period-8 via the first, the second, and the third period-doubling bifurcation, respectively, entering into chaotic state and ultimately being an invalid state. The stability boundary and the invalidated boundary are derived

theoretically through stability analysis, where the stable state of valley voltage-mode controlled buck-boost converter can transit to an unstable state, and the converter can shift from operation region to forbidden region. Research results show that the time constant of the output capacitor is a critical factor for the voltage-mode controlled buck-boost converter, which has an important influence on the dynamics as well as control stability of voltage-mode controlled buck-boost converter. These results verified by time-domain waveforms and phase portraits from both simulation and experiment indicate that the sampled-data model is correct. The results in this paper can provide useful guidance for designing the buck-boost converter with valley voltage-mode control.

References

[1] Redl R and Sun J 2009 *IEEE Trans. Power Electron.* **24** 2669

[2] Schweitzer B P and Rosenstein A B 1964 *IEEE Trans. Aerospace and Electron. Syst.* **2** 1171

[3] Wang J P, Bao B C, Xu J P, Zhou G H and Wen H 2013 *IEEE Trans. Ind. Electron.* **60** 1759

[4] Zhou G H, Xu J P and Wang J P 2014 *IEEE Trans. Ind. Electron.* **61** 1280

[5] He S Z, Zhou G H, Xu J P, Bao B C and Yang P 2013 *Acta Phys. Sin.* **62** 110503 (in Chinese)

[6] He S Z, Zhou G H, Xu J P, Wu S R and Chen L 2014 *Acta Phys. Sin.* **63** 130501 (in Chinese)

[7] Zhou G H, He S Z, Chen X and Cui H F 2014 *Electron. Lett.* **50** 627

[8] Shi G D, Zhang H M, Bao B C, Feng F and Dong W 2015 *Acta Phys. Sin.* **64** 010501 (in Chinese)

[9] Xie F, Yang R and Zhang B 2011 *IEEE Trans. Circuits Syst. I, Reg. Papers* **58** 2269

[10] Bao B C, Zhou G H, Xu J P and Liu Z 2011 *IEEE Trans. Power Electron* **26** 1968

[11] Deivasundari P S, Uma G and Poovizhi R 2013 *IET Power Electron.* **6** 763

[12] Wang F Q and Ma X K 2013 *Chin. Phys. B* **22** 120504

[13] Zhou Y F, Chen J N, Iu H H C and Tse C K 2008 *Int. J. Bifurc. Chaos* **18** 121

[14] Zhao Y B, Zhang D Y and Zhang C J 2007 *Acta Chin. Phys.* **16** 933

[15] Wang F Q, Zhang H and Ma X K 2012 *Chin. Phys. B* **21** 020505

[16] Zhou G H, Xu J P, Bao B C, Zhang F and Liu X S 2010 *Chin. Phys. Lett.* **27** 090504

[17] Banerjee S, Parui S and Gupta A 2004 *IEEE Trans. Circuits Syst. II* **51** 649

[18] He S Z, Zhou G H, Xu J P, Wu S R, Yan T S and Zhang X 2014 *Acta Phys. Sin.* **63** 170503 (in Chinese)

[19] Fang C C 2001 *IEEE Trans. Power Electron.* **16** 345

[20] Banerjee S and Chakrabarty K 1998 *IEEE Trans. Power Electron.* **13** 252

[21] Xie F, Yang R and Zhang B 2010 *Acta Phys. Sin.* **59** 8393 (in Chinese)

[22] Chen Y F, Tse C K, Qiu S S, Lindenmuller L and Schwarz W 2008 *IEEE Trans. Circuits Syst. I, Reg. Papers* **55** 3335

[23] Bao B C 2013 *An Introduction to Chaotic Circuits* (Beijing: Science Press) (in Chinese) p. 164