Comparative study of electrical characteristics for n-type 4H–SiC planar and trench MOS capacitors annealed in ambient NO*

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The interface properties and electrical characteristics of the n-type 4H–SiC planar and trench metal–oxide–semiconductor (MOS) capacitors are investigated by measuring the capacitance voltage and current voltage. The flat-band voltage and interface state density are evaluated by the quasi-static method. It is not effective on further improving the interface properties annealing at 1250 °C in NO ambient for above 1 h due to the increasing interface shallow and fast states. These shallow states reduce the effective positive fixed charge density in the oxide. For the vertical MOS capacitors on the $(11\bar{2}0)$ and $(1\bar{1}00)$ faces, the interface state density can be reduced by approximately one order of magnitude, in comparison to the result of the planar MOS capacitors on the (0001) face under the same NO annealing condition. In addition, it is found that Fowler–Nordheim tunneling current occurs at an oxide electric field of 7 MV/cm for the planar MOS device. However, Poole–Frenkel conduction current occurs at a lower electric field of 4 MV/cm for the trench MOS capacitor. This is due to the local field crowded at the trench corner severely causing the electrons to be early captured at or emitted from the SiO_2/SiC interface. These results provide a reference for an in-depth understanding of the mobility-limiting factors and long term reliability of the trench and planar SiO_2/SiC interfaces.

Keywords: 4H–SiC metal–oxide–semiconductor capacitors, trench, interface states, nitric oxide annealing

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1. Introduction

Silicon carbide is a promising candidate for advanced power switching devices, owing to the superior material properties such as high thermal conductivity, high critical electric field, and the larger carrier saturation velocity.[1–4] The full potential of SiC metal–oxide–semiconductor field-effect transistor (MOSFET) is still far from being reached because of the relatively high interface state density (D_{it}) at the SiO_2/SiC interface.[5–10] The improvement of the channel mobility can be achieved via the post-oxidation annealing (POA) in NH_3,[11] N_2O,[12] Ar, $POCl_3$,[8,13] and sodium[14] atmosphere. Among them, nitridation by nitric oxide (NO) is considered to be an effective industrial technique to improve the interface properties. The interface state density can be reduced to a low value for the MOS capacitors annealed in NO at 1250 °C. Nonetheless, the conventional high-frequency method cannot detect the fast states responding to higher than 100 MHz. It is believed that NO annealing at a temperature above 1250 °C is not recommended due to the generation of very fast states.[15,16] The variation of fast interface state with NO annealing time at 1250 °C or below has not been investigated in detail. Meanwhile, the effects of fast and shallow states on the flat-band voltage shift and channel mobility of the MOSFETs are still ambiguous.

On the other hand, fundamental studies of SiC planar MOS capacitors formed on $(11\bar{2}0)$ and $(1\bar{1}00)$ faces have been performed in the past few years. It is proved that MOSFETs fabricated on these nonpolar faces with NO annealing exhibit higher channel mobilities than those fabricated on (0001) face.[17–19] Nevertheless, the channels are formed on a sidewall of the trench for the trench MOSFET. The capacitance–voltage measurement is therefore difficult to use for directly evaluating the interface quality of the sidewall (we call it vertical MOS capacitor in this paper). Anisotropic channel properties on the trench sidewall were mostly evaluated through the value of field effective mobility of the fabricated trench MOSFET.[19–21] In addition, the most commonly cited intrinsic oxide degradation mechanism is the Fowler–Nordheim tunneling for the SiC planar MOSFETs.[22,23] Different mechanisms of charge transports at the SiO_2/SiC interface have not

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been well understood. Therefore, comparisons of electrical characteristic and interface property between the trench and planar MOS capacitors are required in order to obtain a comprehensive understanding of the anisotropic channel mobility and reliability issues for the 4H–SiC MOSFETs.

In this study, the interface properties of planar MOS capacitors for different nitridation times are presented. We also propose a simple method to estimate the density of interface states of the vertical MOS capacitor by using the quasi-static capacitance voltage measurement. Comparison of electrical characteristic between the planar MOS and trench MOS capacitor is discussed in detail.

2. Experiments

Figure 1(a) shows the schematics of one unit cell 4H–SiC planar and trench MOS capacitors, which were fabricated on the n-type 4° off-angle silicon face (0001) epitaxial substrates. The wafers were purchased from TYSiC, with a bulk doping concentration of approximately 8×10^{15} cm^{-3}. For samples A, B, and C, the wafers were prepared for planar MOS capacitors. For sample D, 2-μm deep and 3-μm wide trenches were obtained by inductively coupled plasma (ICP) etching using mixed gases of SF_6, O_2, HBr. Stripe-shaped unit cell trenches were patterned on the wafer with the SiO_2 mask. The directions of the trenches are perpendicular and parallel to the primary flat of the wafer to form the vertical MOS capacitors on the $(1\bar{2}00)$ and $(11\bar{1}0)$ faces respectively, as shown in Figs. 1(a) and 1(b). All the samples were dipped in buffered HF (BOE) after solvent and standard RCA cleaning process. Subsequently, samples A, B, and C were subjected to dry oxidation at 1250 °C for 2.5 h. Post-oxidation annealing (POA) was subsequently performed in NO ambient at 1250 °C for 1 h, 2.5 h, and 5 h, separately. These samples are marked as NO_xh as listed in Table 1 (where x means that the sample is annealed in NO for x hours after dry oxidation). In addition, sample D was annealed in NO at 1250 °C for 2.5 h after dry oxidation of 75 min. A flat reference capacitor was also fabricated on the substrate of sample D. Aluminum of 300-nm-thick was subsequently evaporated and patterned using standard photolithographic procedures to form the gate electrode for each of the samples. BOE was used to remove the oxide grown on the back side, followed by the formation of back contact using nickel.

The high frequency (10 kHz) capacitance voltage (HFCV) and the quasi-static capacitance voltage (QSCV) measurements were done using Agilent B1500A. Some useful information can be obtained by the DC and HFCV measurement to set the various QSCV parameters such as the integration time, current range, leakage current and the capacitance value appropriately. For most of the cases, the integration time needs to be longer than the time constant of the QSCV response. To obtain an accurate value of the quasi-static capacitance, it may be necessary to adjust the parameters and measure them by trial and error through comparing the data. The QSCV measurement was performed in steps of 0.2 V for the gate voltage sweep and in an integration time of 1 s for the charge calculation. The interface state density was extracted by the proposed method i.e., the "C–ψ_S method".[15] Meanwhile, we used the "Terman method"[24] to evaluate the interface state density in the planar MOS capacitor. Current–voltage (I–V) measurements have also been performed to confirm the process quality and the extrinsic failures of oxide. All measurements were done at room temperature.

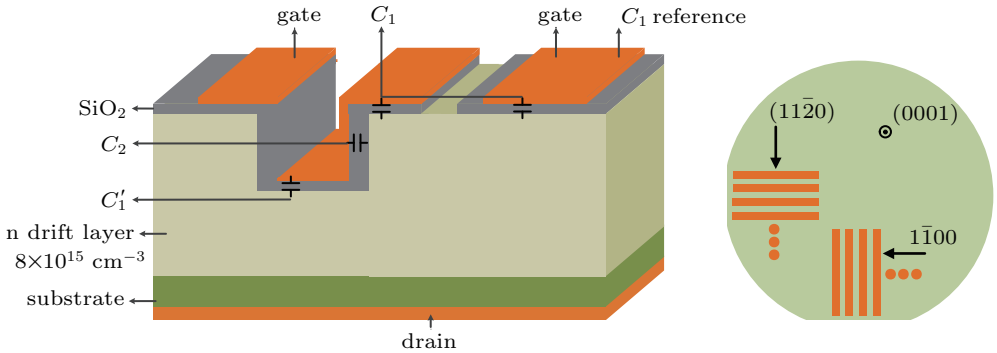


Fig. 1. (color online) (a) Schematics of one unit cell trench and planar MOS capacitors and (b) definitions of the wafer plane orientation and the trench MOS direction.

Table 1. Oxide thickness of all the samples obtained by accumulation capacitance (C–V) and SE (trench sidewall by SEM).

The t_{OX} obtained by	Planar MOS			Trench MOS	
	Sample A	Sample B	Sample C	Sample D: NO_2.5 h	
	NO_1 h	NO_2.5 h	NO_5 h	flat face	sidewall
C–V/nm	86.5	86.8	97.5	55.4	156.9
SE/nm	85.5	87.1	95.9	55.6	154 (by SEM)

3. Results and discussion

Table 1 summarizes the oxide thickness determined by C–V accumulation capacitance. The t_{OX} of the vertical MOS capacitor was achieved by using scanning electron microscopy (SEM). These values are in good agreement with the results obtained by spectroscopic ellipsometry (SE) for all the samples. The thickness of SiO_2 increases slightly with the increasing nitridation time as can be seen by comparing samples A, B, and C. However, due to the anisotropic behavior of oxidation, the t_{OX} of the trench sidewall is almost three times larger than that of the horizontal face for sample D. The t_{OX} determined by SE for all the samples is used to extract the flat-band voltage (V_{FB}), effective oxide charge density (Q_{eff}), and the interface states density (D_{it}) as discussed below.

3.1. Planar MOS devices

The normalized CV curves for the planar MOS devices are extracted from QSCV and HFCV measurements by sweeping the gate voltage from depletion to accumulation. The flat-band voltage (V_{FB}) shift as shown in Fig. 2(a), results from the effective oxide charge density (Q_{eff}) at the SiO_2/SiC interface. The Q_{eff} is the sum of the interface states density (D_{it}), fixed oxide charge density, oxide trapped charge density and mobile charges density.[25,26] The expression for the Q_{eff} can be written as

$$Q_{eff} = (q\varphi_{ms} - V_{FB})C_{OX}/q, \quad (1)$$

where $q\phi_{ms}$ is the work function difference between SiC (3.81 eV) and Al metal (4 3 eV), C_{OX} is the oxide capacitance per unit area. Listed in Table 2 are the V_{FB} and Q_{eff} obtained by the two methods. The V_{FB} obtained by the QSCV method is left shifted in comparison to that obtained by the HFCV method as shown in Fig. 2(a). Furthermore, the curves of semiconductor capacitance (C_D) versus gate voltage for sample C obtained by the two methods are shown in Fig. 2(b). It is found that there is a large difference between C_D and the theoretical semiconductor capacitance $C_{D,theory}$ at a given gate voltage by using the QSCV method. Therefore, the V_{FB} is underestimated by the conventional HFCV method, because the fast and shallow states also contribute to interface trap capacitance (C_{it}).[16,27] These interface trap capacitances are not measured accurately, leading to a wrong value of the flat capacitance.

The values of Q_{eff} determined by the QSCV method ($Q_{eff,QSCV}$) are 2.35×10^{11}, 2.82×10^{11}, and 1.30×10^{11} cm^{-2} respectively for the planar MOS capacitors annealed in NO atmosphere for 1 h, 2.5 h, and 5 h. In the previous reports, it was demonstrated that the NO annealed oxides possess N-induced hole traps, which are positively trapped charges and scaled with the NO annealing time.[28,29] Nevertheless, in this experiment, $Q_{eff,QSCV}$ for the sample NO_5 h is smaller than that for the sample NO_2.5 h, and $Q_{eff,HFCV}$ even switches from positive to negative values. We speculate that the shallow state density should increase with the increase of NO annealing time. These shallow states (donor-type traps) exist near the SiO_2/SiC interface in the oxide and trap more electrons, leading to a decrease of effective positive fixed charge density. The density of shallow states probably increases with a slow rate when NO annealing time ranges from 1 h to 2.5 h. Thus, it has almost no effect on the total Q_{eff}. A sharp increase in the density of shallow states occurs when NO annealing time ranges from 2.5 h to 5 h, which results in reductions of $Q_{eff,QSCV}$ and $Q_{eff,HFCV}$. As shown in the last row of Table 2, the values of effective interface fast state density ($Q_{it,eff}$) are estimated by subtracting $Q_{eff,HFCV}$ from $Q_{eff,QSCV}$. Note that $Q_{it,eff}$ increases in proportion to the NO annealing time, which may be related to very fast states existing near the SiO_2/SiC interface in SiC (the fast states will be discussed later). Therefore, the channel mobility is still below 50 cm^2/V·s, which is probably caused by a reduction of the free carrier density at the SiO_2/SiC interface and by the scattering of the trapped electrons.[30,31]

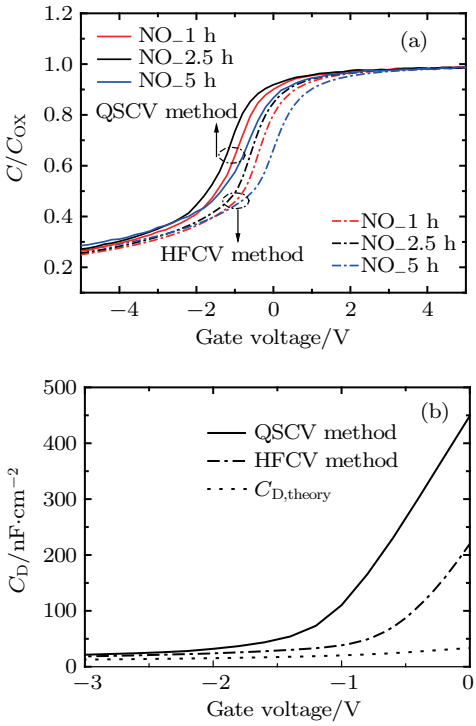


Fig. 2. (color online) C–V curves of (a) planar MOS capacitors for different NO annealing times, and (b) semiconductor capacitance C_D versus gate voltage for sample NO_2.5 h obtained by QSCV and HFCV method. The $C_{D,theory}$ versus gate voltage is also plotted.

Table 2. Flat-band voltages and effective oxide charge densities determined by the QSCV and HFCV method for the planar MOS capacitors for different NO annealing times.

Planar MOS	NO_1 h	NO_2.5 h	NO_5 h
Ideal C_{FB}/C_{OX}	0.836	0.839	0.851
$V_{FB,QSCV}$/V	–0.44	–0.65	–0.09
$Q_{eff,QSCV}$/cm^{-2}	2.35×10^{11}	2.82×10^{11}	1.30×10^{11}
$V_{FB,HFCV}$/V	0.14	–0.04	0.61
$Q_{eff,HFCV}$/cm^{-2}	0.88×10^{11}	1.31×10^{11}	-0.27×10^{11}
$Q_{it,eff}$/cm^{-2}	1.47×10^{11}	1.51×10^{11}	1.57×10^{11}

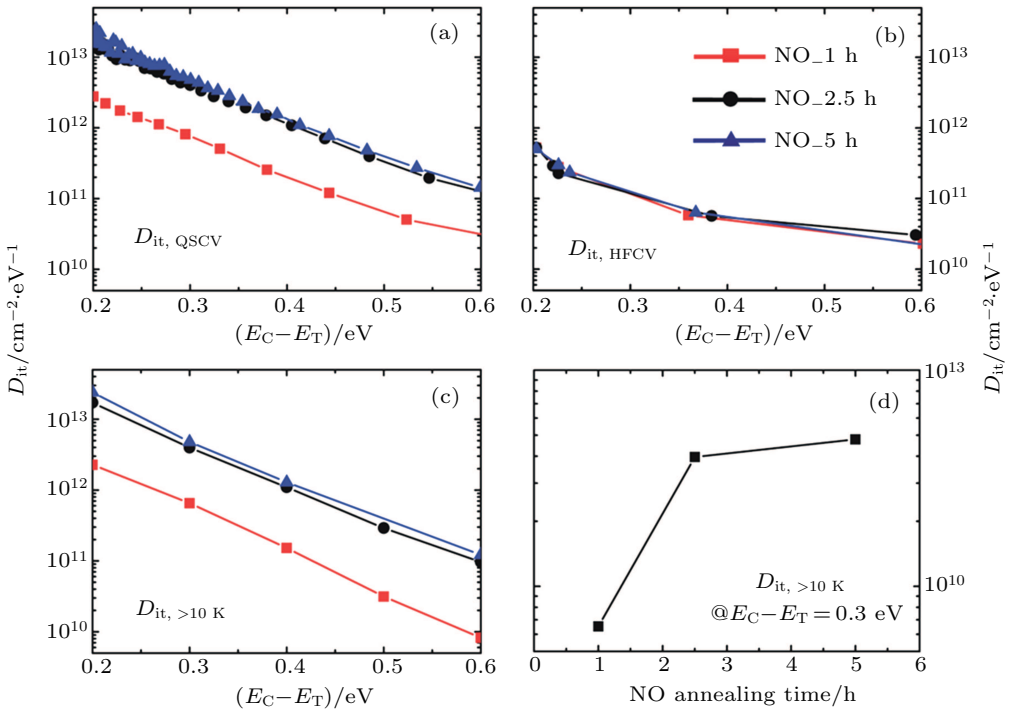


Fig. 3. (color online) Distributions of (a) $D_{it,QSCV}$, (b) $D_{it,HFCV}$, (c) $D_{it,>10\ K}$ and (d) fast states density at E_C–$E_T = 0.3$ eV.

The interface state density is evaluated by using the QSCV ($D_{it,QSCV}$) and HFCV ($D_{it,HFCV}$) method. The former method was presented in detail in Section 3, together with being used for calculating the vertical MOS capacitors. Figures 3(a)–3(d) show $D_{it,QSCV}$, $D_{it,HFCV}$, and $D_{it,>10\ K}$ for the planar MOS capacitors annealed in NO for 1 h, 2.5 h and 5 h, respectively. Here, $D_{it,>10\ K}$ is for the fast state capacitor responding to higher than 10 kHz, and is achieved by subtracting $D_{it,HFCV}$ from $D_{it,QSCV}$. Sample NO_1 h possesses the smallest $D_{it,QSCV}$ as shown in Fig. 3(a). Meanwhile, the interface state density is beyond a value of 10^{13} cm^2·eV^{-1} near the conduction band edge for 5 h NO annealing time. As shown in Fig. 3(b), there is no obvious difference in $D_{it,HFCV}$ with increasing NO annealing time due to the underestimation of the fast state. It is noted that $D_{it,>10\ K}$ does not scale linearly with nitrogen incorporation as indicated in Figs. 3(c) and 3(d). Figure 3(d) also shows that $D_{it,10\ K}$ at $E_C - E_T = 0.3$ eV is reduced by approximately 86% for the sample annealed in NO for less than 2.5 hours.

Based on the above-mentioned evaluation results, it is concluded that NO annealing at 1250 °C for above 1 h is not effective in further improving the interface properties due to the increasing fast and shallow state density at the SiO_2/SiC interface. These fast states can respond to the frequencies higher than the measurement frequency of 10 kHz in this study and are almost saturated for a longer NO annealing time. However, the interfacial electron trapping in the shallow state will occur at the SiO_2/SiC interface. These shallow states are donor-like, thus being neutralized after capturing the electrons. The density of shallow states is rapidly increased when NO annealing time is increased beyond 2.5 h, which causes a reduction of Q_{eff}. The fast and shallow states both determine the flat-band voltage of the MOS capacitor and restrict the improvement of the channel mobility of SiC MOSFET.

3.2. Trench MOS devices

We investigate the crystallographic orientation dependence of the interface state density of the trench MOS capacitor annealed in NO at 1250 °C, especially for $(11\bar{2}0)$ and $(1\bar{1}00)$ faces devices. An appropriate thickness of SiO_2 serves as the dry etching mask, which is annealed in O_2 at 1000 °C for the densification. Therefore, the surface roughness of the trench sidewall may be reduced. Subsequently, the etched substrate is thermally oxidized to form a sacrificial oxide with a thickness of approximately 20 nm. The sacrificial oxide layer is removed by diluted HF. Thus, the defect density on the SiC surface introduced by the previous etching process may be reduced. Some parts of the sample are patterned by photoresist, to produce a planar MOS capacitor at the same substrate without any vertical edge as shown in Fig. 1(a). The quasi-static capacitance for the trench MOS structure ($C_{QS,trench}$) is given by the sum of three MOS capacitors as follows:

$$C_{QS,trench} = C_2S_2 + C_1S_1 + C_1'S_1' = C_2S_2 + C_1(S_1 + S_1'), \quad (2)$$

where C_2 is the vertical MOS quasi-static capacitance per unit area for the $(11\bar{2}0)$ or $(1\bar{1}00)$; C_1 and C_1' are the planar MOS quasi-static capacitances per unit area for the (0001) faces; S_1,

S_1', and S_2 are the areas of gate electrode for the three MOS capacitors respectively. Here, C_1 can be approximated as C_1', because the C–V curves for the two capacitors show a similar appearance.

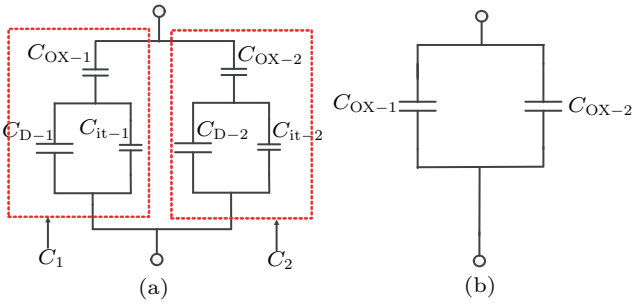


Fig. 4. (color online) Equivalent circuits for the trench MOS capacitor in (a) depletion using QSCV method and (b) in strong accumulation using HFCV method, where C_1, C_{D-1}, C_{OX-1}, and C_{it-1} are the quasi-static, semiconductor, oxide and interface trap capacitances per unit area for the planar MOS capacitors, respectively. C_2, C_{D-2}, C_{OX-2}, and C_{it-2} are those for the vertical MOS capacitors, respectively.

Based on the quasi-static equivalent circuit shown in Fig. 4(a), the relationship between the quasi-static capacitances and interface trap capacitances is given by:

$$C_1 = \frac{C_{OX-1}(C_{D-1}+C_{it-1})}{C_{OX-1}+C_{D-1}+C_{it-1}}, \tag{3}$$

$$C_2 = \frac{C_{OX-2}(C_{D-2}+C_{it-2})}{C_{OX-2}+C_{D-2}+C_{it-2}}. \tag{4}$$

Combining Eqs. (2) and (4) yields

$$C_2 = \frac{C_{QS,trench}-C_1(S_1+S_1')}{S_2} = \frac{C_{OX-2}(C_{D-2}+C_{it-2})}{C_{OX-2}+C_{D-2}+C_{it-2}}, \tag{5}$$

where C_{D-1}, C_{OX-1}, and C_{it-1} are the semiconductor, oxide and interface trap capacitances per unit area for the planar MOS capacitor, respectively. Likewise, C_{D-2}, C_{OX-2}, and C_{it-2} are those for the vertical MOS capacitors, respectively. The oxide capacitance of the vertical MOS capacitor can be determined by the accumulation, which is based on the equivalent circuit shown in Fig. 4(b). The interface state densities for the planar and vertical MOS capacitors can be calculated from

$$D_{it-1} = \frac{C_{D-1}+C_{it-1}-C_{D,theory}}{q^2}, \tag{6}$$

$$D_{it-2} = \frac{C_{D-2}+C_{it-2}-C_{D,theory}}{q^2}. \tag{7}$$

The flat-band voltage of the fabricated MOS capacitor is roughly estimated from the surface potential (ψ_S) and gate voltage curve as shown in Fig. 5(a). For the vertical MOS capacitors fabricated on the $(11\bar{2}0)$ and $(1\bar{1}00)$ faces, the values of V_{FB} are -4.4 V and -4.2 V, and the values of Q_{eff} calculated from Eq. (1) are 6.85×10^{11} and 6.60×10^{11} cm^{-2}, respectively. As we can see, the vertical MOS capacitor has a large negative flat-band voltage shift. This is because the surface roughness of the trench sidewall causes the generation of positive fixed charge after thermal oxidation and NO annealing. Meanwhile, due to the metal ion contamination of the substrate surface in the ICP process, the calculated Q_{eff} of 7.33×10^{11} cm^{-2} is larger than the previous results for the planar MOS capacitors under the same NO annealing condition.

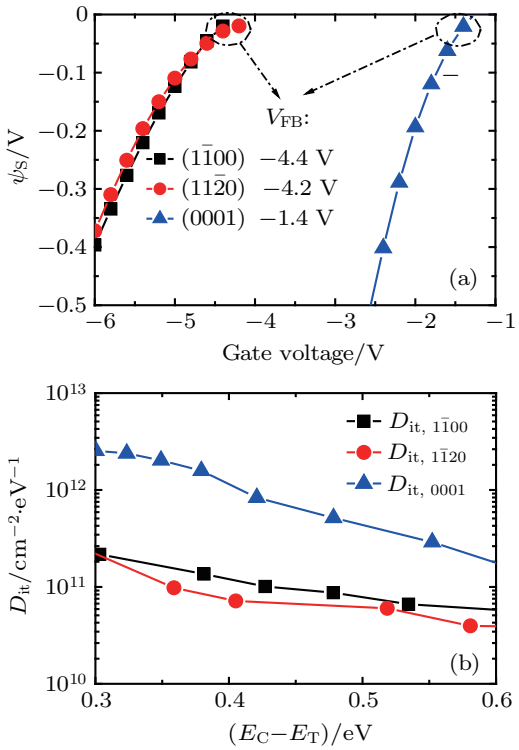


Fig. 5. (color online) (a) Comparison among the curves of surface potential versus gate voltage curves of 4H–SiC MOS capacitors on $(1\bar{2}00)$, $(11\bar{1}0)$, and (0001) faces, and (b) distributions of D_{it} extracted from high-frequency QSCV method for those MOS capacitors, with $D_{it,11-20}$, $D_{it,1-100}$, and $D_{it,0001}$ corresponding to the MOS capacitors on $(1\bar{2}00)$, $(11\bar{1}0)$, and (0001) faces, respectively.

Figure 5(b) shows the interface state densities $D_{it,11\bar{2}0}$, $D_{it,1\bar{1}00}$, and $D_{it,0001}$ for the MOS capacitors on $(11\bar{2}0)$, $(1\bar{1}00)$, and (0001) faces on the same substrate, respectively. The slight difference between $D_{it,11\bar{2}0}$ and $D_{it,1\bar{1}00}$ is caused by the locally nonuniform oxide thickness due to the oxidation anisotropy,[32] which further increases the interface state density at the SiO_2/SiC interface. It has been found that the value of D_{it} at the edge of the conduction band increases as a function of oxide thickness due to the existence of deep acceptor-type surface states.[33] Even though the t_{OX} of the vertical MOS capacitor is larger than that of the planar MOS capacitor, nitridation is carried out under the same NO condition after oxidizing both of the MOS devices. By using the aforesaid method of calculation, it is directly demonstrated that $D_{it,11\bar{2}0}$ and $D_{it,1\bar{1}00}$ are smaller than $D_{it,0001}$ due to the more superior MOS interface quality of the $(11\bar{2}0)$ and $(1\bar{1}00)$ faces.[30] In spite of the thicker oxide, the interface trap density for the $(11\bar{2}0)$ face at $E_C - E_T = 0.3$ eV can be reduced by approximately one order of magnitude in comparison to that for the (0001) face.

3.3. Comparisons of current–voltage characteristic between planar and trench MOS capacitors

Figure 6(a) shows FN plots for the fabricated planar MOS capacitor, which can be expressed as follows:[34]

$$J_{\mathrm{FN}} = AE^2 \exp\left(-\frac{B}{E}\right), \tag{8}$$

$$A = \frac{q^3 m_{\mathrm{e}}}{8\pi h m_{\mathrm{ox}} \phi_{\mathrm{B}}}, \quad B = \frac{4(2m_{\mathrm{ox}})^{1/2}\phi_{\mathrm{B}}^{3/2}}{3qh/2\pi}, \tag{9}$$

where m_{e} is the free electron mass, q is the electronic charge, h is the Planck's constant, and ϕ_{B} is the barrier height between oxide and semiconductor. Using the slope of the curve of $\ln(I/E^2)$ versus $1/E$ as shown in Fig. 6(a), ϕ_{B} can be calculated with a known electron effective mass m_{ox} in oxide ($0.5m_{\mathrm{e}}$). The barrier height is 2.7 eV, which is close to the value of the band offset between 4H–SiC and SiO_2 in a previous study.[35]

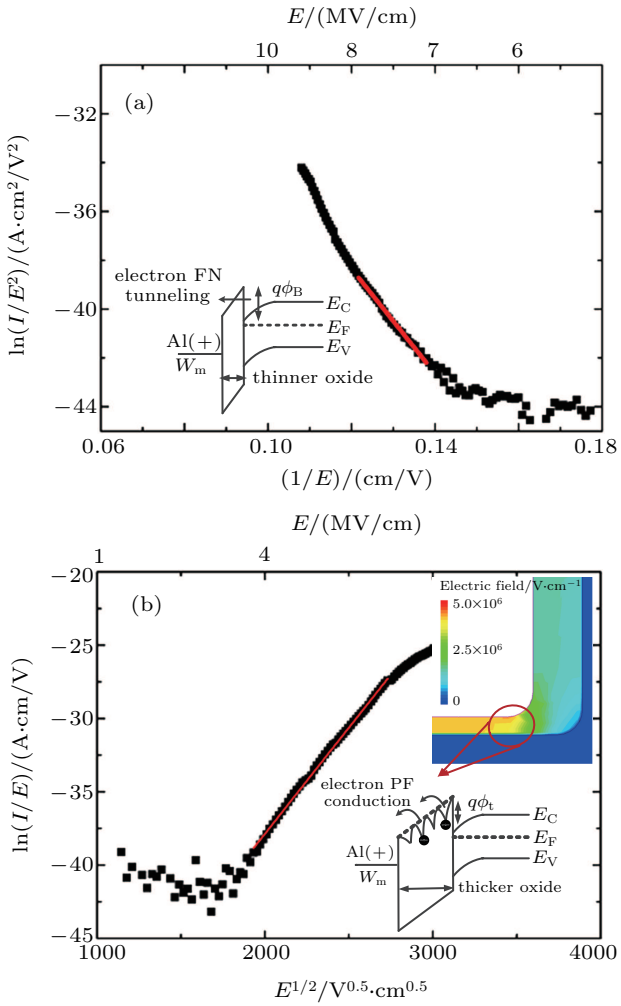


Fig. 6. (color online) (a) Electric-field-dependent Fowler–Nordheim (FN) I–E characteristics and (b) Poole–Frenkel (PF) I–E characteristics for the planar MOS and trench MOS capacitors respectively, with insets showing the energy-band diagrams for electron emission in both of the SiC MOS capacitors. Simulated two-dimensional (2D) electric field distribution when oxide breakdown occurs for the trench MOS capacitors is plotted.

In contrast, a different current–voltage characteristic is obtained for the trench MOS capacitor. A linear function between $\ln(I/E)$ and $E^{1/2}$ is achieved as shown in Fig. 6(b). The current density associated with Poole–Frenkel emission is determined by[36,37]

$$J_{\mathrm{PF}} = (qN_{\mathrm{c}}\mu)E \exp\left[\frac{-q(\phi_{\mathrm{t}} - \sqrt{qE/\pi\varepsilon_0\varepsilon_{\mathrm{r}}})}{kT}\right], \tag{10}$$

where ε_{r} is the relative dielectric permittivity, $k$is the Boltzmann's constant, ε_0 is the permittivity of free space, T is the temperature, q is the electronic charge, N_{c} is the conduction-band effective density of states, μ is the electron mobility, and ϕ_{t} is the potential barrier height for electron emission from the trapped state in oxide. In Eq. (10), the slope of $\ln(J/E)$ versus $E^{1/2}$ can be written as

$$k_{\mathrm{slope}} = \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_{\mathrm{r}}}}. \tag{11}$$

The relative dielectric permittivity of SiO_2 can be obtained from Eq. (11) as follows:

$$\varepsilon_{\mathrm{r}} = \frac{q^3}{\pi\varepsilon_0 k_{\mathrm{slope}}^2 k^2 T^2} k_{\mathrm{slope}}. \tag{12}$$

The value of k_{slope} is calculated to be 0.01448 from a linear fitting curve as shown in Fig. 6(b). Thus, the relative dielectric permittivity $\varepsilon_{\mathrm{r}} = 4.0$ can be extracted from Eq. (12), which is in good agreement with the value for SiO_2.

As indicated in the energy-band diagram in the insert of Fig. 6(b), the field emission of electrons will dominate the current transport for the trench MOS capacitor. This is due to the trapped positive charge existing in the thick oxide corner of the trench. Furthermore, as shown by the simulation result of 2D electric field distribution in Fig. 6(b), the local field crowding will severely cause the local electrons to be captured in or emitted from the interface traps. Thus, the PF conduction current can take place at a critical electric field of $E_{\mathrm{C}} = 4$ MV/cm for the trench MOS device. This value is lower than that of planar MOS device (FN tunneling current occurs at $E_{\mathrm{C}} = 7$ MV/cm), probably because more uniform thickness of oxide is formed in the planar MOS capacitor. It is thus concluded that the peak value of the electric field in the gate oxide of trench MOSFET should be reduced to below 4 MV/cm, for the long term reliability and threshold voltage stability.

4. Conclusions

The capacitance voltage and current voltage are measured to evaluate the flat-band voltages, effective oxide charge densities, the interface state densities and oxide breakdown characteristics of the trench and planar MOS capacitors. We report for the first time in this paper the achievement of D_{it} by measuring the quasi-static capacitance voltage, for the trench MOS capacitor in which only two mask layers are used.

The flat-band voltage is severely underestimated by the conventional HFCV method. Meanwhile, the interface state

density does not decrease significantly with the NO annealing at 1250 °C for above 1 h, due to the increasing shallow and fast states generated by the nitrogen incorporation. These shallow states result in a decrease of effective positive fixed charge density because more electrons are trapped into the states near the SiO_2/SiC interface in the oxide. On the other hand, it is found that D_{it} at $E_C - E_T = 0.3$ eV for vertical MOS capacitor on the $(11\bar{2}0)$ face can be reduced to below 10^{12} $cm^2 \cdot eV^{-1}$, which is smaller than that for planar MOS capacitors on the (0001) face. However, the electric field in the gate oxide of trench MOS capacitor should be reduced to below 4MV/cm due to local field crowded at the corner of the trench gate. It is concluded that the trapped positive charges at the trench oxide result in the electrons captured or emitted early. Therefore the PF conduction current occurs at the lower electric field, in comparison to the FN tunneling current for the planar MOS capacitor. The present results will provide a better understanding of the interface properties and reliability of oxynitrided 4H–SiC MOSFETs.

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