Impact of neutron-induced displacement damage on the single event latchup sensitivity of bulk CMOS SRAM

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Since the displacement damage induced by the neutron irradiation prior has negligible impact on the performance of the bulk CMOS SRAM, we use the neutron irradiation to degrade the minority carrier lifetime in the regions responsible for latchup. With the experimental results, we discuss the impact of the neutron-induced displacement damage on the SEL sensitivity and qualitative analyze the effectiveness of this suppression approach with TCAD simulation.

Keywords: displacement damage, neutron irradiation, single event latchup, TCAD simulation

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1. Introduction

Single event latchup (SEL) in space and at the ground is one of the most well-known hard errors, which is inherent to the CMOS ICs. The charge induced by the ion can modify the electrical field and possibly trigger the parasitic four-layer P–N–P–N structure.[1–3] Under this circumstance, the reverse-biased junctions become conductive, resulting in the loss of functionality or device destruction. To suppress this phenomenon, many hardening methods have been developed to mitigate the SEL, such as epitaxial layer, guard rings, shallow trench isolation, and silicon on insulator (SOI) technology. However, these methods will change the inherent structure and technological process of the SRAM chips, which are difficult to achieve for many commercial ICs. So it is meaningful to find a post-processing strategy to suppress the latchup sensitivity of commercial SRAM chips.

Using displacement damage to suppress SEL is an old concept. In 1979, Adams[4] characterized the long-term annealing of neutron irradiation induced changes in the suppression of MOS/LSI ICs' latchup. Since then, various researchers have explored this method. Spratt[5] studied the heavy ion induced displacement damage to suppress the SEL for CMOS ICs in 2003. Moreover, protons have also been studied as a means of producing damage by Eddy *et al.*[6] in 1981. Unfortunately, heavy ion and proton can lead to ionizing dose damage which is not desirable. Neutrons are uncharged particles which are more acceptable to produce the displacement damage. However, no data focused on the neutron induced displacement damage in the suppression of SEL in the state-of-the-art CMOS SRAM technology have been published.

Neutron-induced displacement damage can change several semiconductor parameters that can affect charge collection mechanisms from a single event strike.[7] The most sensitive one is the minority carrier lifetime. A decrease in the minority carrier lifetime leads to a decrease in the parasitic bipolar transistor gain and reduces the latchup sensitivity of bulk CMOS SRAM.

The aim of this paper is to verify the effectiveness of the neutron irradiation hardening strategy. The broad beam heavy ion experiment and the pulsed laser experiment were performed to support our conclusion. Furthermore, the technology assisted computer aided design (TCAD) simulation tool was utilized to explore the underlying mechanism of this hardening strategy.

2. Basic theory

When fabricating CMOS SRAM chips in a bulk technology, one cannot avoid creating the parasitic four-layer P–N–P–N structures, which are also known as thyristors or silicon controlled rectifiers. Figure 1 shows one of these parasitic structures that is introduced by placing NMOS and PMOS transistors side-by-side in a CMOS inverter. Latchup can occur because the parasitic vertical pnp transistor and the lateral npn transistor form a feedback loop which will amplify the current induced by the particle strike and cause it to sustain itself.

Latchup is possible only if (i) the transistors become biased into the forward active mode, (ii) the transistors current gain product ($\beta_{\rm npn} \cdot \beta_{\rm pnp}$) exceeds unity, and (iii) the bias supply is capable of sourcing a current greater than the holding current.[2] Preventing any of these requirements will avoid latchup.

In this work, a post-processing hardening strategy based on requirement (ii) is proposed. As we all know, the neutron-induced displacement damage can alter several semiconductor parameters and the most sensitive parameter is the minority

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carrier lifetime. A decrease in the minority carrier lifetime leads to a decrease in the parasitic bipolar transistor's gain and latchup will not occur if the parasitic transistors current gain product is below unity. Using fast neutrons to reduce the parasitic bipolar gain is a meaningful study because the ionizing dose effect can be ignored if the n/γ of the neutron fluence is high enough.

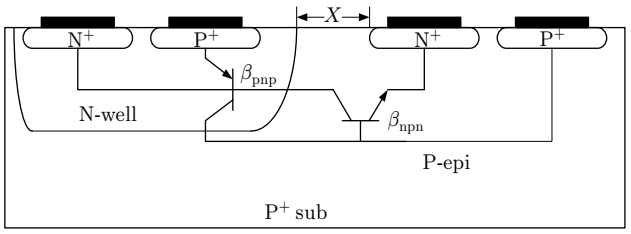


Fig. 1. Typical cross-section of an N-well CMOS technology showing parasitic bipolar transistors and the simplified P–N–P–N structure.

3. Neutron exposure

In this paper, two kinds of commercial-off-the-shelf (COTS) SRAM chips include the 800-nm bulk CMOS process from the IDT Semiconductor (chip #:IDT6116SA45P, 2K×8-Bit) and the 150-nm bulk CMOS process from the Cypress Semiconductor (chip #:CY7C1021CV33-10ZXI, 64K×16-Bit) were exposed to fast neutron radiation with fluence up to 2×10^{14} 1-MeV(Si)-n/cm^2.

The neutron irradiation experiment was carried out with the fast burst reactor facility of the Xi'an Pulsed Reactor (XAPR). The 1# shielding device which held a high n/γ value around 6.1×10^9 cm^{-2}·rad(Si)$^{-1}$ provided the experiment environment. After the neutron irradiation, the chips were stored at room temperature until the radioactivity level had fallen to the safe range. Subsequently, the chips' parameters from the SRAMs' datasheet were measured on the VLSI test system J750EX of the Northwest Institute of Nuclear Technology (NINT). The electrical measurements of IDT6116SA45P were performed 60 days after the neutron irradiation and the test results are shown in Table 1, and the same of CY7C1021CV33 in Table 2. As we can see, no parameter's variation between the pre- and post-neutron-irradiation chips exceeds 10%.

Table 1. Electrical parameters measurements of IDT6116SA45P taken on the chips without neutron irradiation (1# and 2#) and after the neutron irradiation (3# and 4#).

Chip	Read-write test	$I_{CC}(f=0)$/mA	$I_{CC}(f=f_{MAX})$/mA	I_{SB}/nA	T_{AA}/ns	T_{OE}/ns	T_{AW}/ns	T_{WP}/ns
1#	pass	62.0871	98.9569	939.8937	12.0000	6.2000	4.6000	6.8000
2#	pass	58.8913	94.4585	987.9155	12.6000	6.6000	4.6000	7.2000
3#	pass	63.1745	97.8093	601.4207	12.6000	6.4000	5.0000	7.0000
4#	pass	63.6672	98.5234	788.4326	12.4000	6.2000	5.0000	6.8000

Table 2. Electrical parameters measurements of CY7C1021CV33 taken on the chips without neutron irradiation (1# and 2#) and after the neutron irradiation (3#, 4#, and 5#).

Chip	Read-write test	I_{CC}/mA	I_{SB}/mA	T_{AA}/ns	T_{ACE}/ns	T_{AW}/ns	T_{PWE}/ns
1#	pass	16.7076	1.9753	51.0000	50.0000	65.0000	116.0000
2#	pass	16.7076	1.9815	51.0000	50.0000	64.0000	116.0000
3#	pass	16.7076	2.0122	51.0000	50.0000	64.0000	117.0000
4#	pass	16.7076	2.2071	51.0000	50.0000	64.0000	117.0000
5#	pass	16.7076	2.0237	51.0000	50.0000	65.0000	116.0000

4. Experiment results

To verify the effectiveness of the neutron irradiation prior to the hardening strategy, the heavy ion experiment and the pulsed laser experiment were carried out. The pre- and post-neutron-irradiation chips' SEL cross sections were calculated and are shown below. What is more, a typical 2-D CMOS inverter simulation model was built to analyze the underlying mechanism of this post-processing hardening strategy.

4.1. Heavy ion experiment

Heavy ion SEL tests were carried out with the tandem accelerator facility of the China Institute of Atomic Energy (CIAE). The ions used in the test are tabulated in Table 3.

The device under test (DUT, IDT6116SA45P) was decapsulated and written with the initial data "0x0055". The SRAM was tested statically, which means that the chip was exposed to normal ion beams, and then the memory was read back and checked for upsets and latchups. We chose the ^{48}Ti and ^{79}Br ions to test our chips with neutron irradiation and without neutron irradiation.

Table 3. Ions used in heavy ion accelerator experiment.

Ion	Energy/MeV	LET/MeV·cm^2·mg^{-1}
^{48}Ti	169	21.8
^{79}Br	218	42.0

As shown in Fig. 2, the SEL cross sections of the chips in the heavy ion environment were calculated. For ^{48}Ti and ^{79}Br ions irradiation, the chip without neutron irradiation has an almost 2 or 3 times higher SEL cross section than the chip with neutron irradiation fluence 2×10^{14} 1-MeV(Si)-n/cm^2. However, the SEL was still observed at this neutron fluence level.

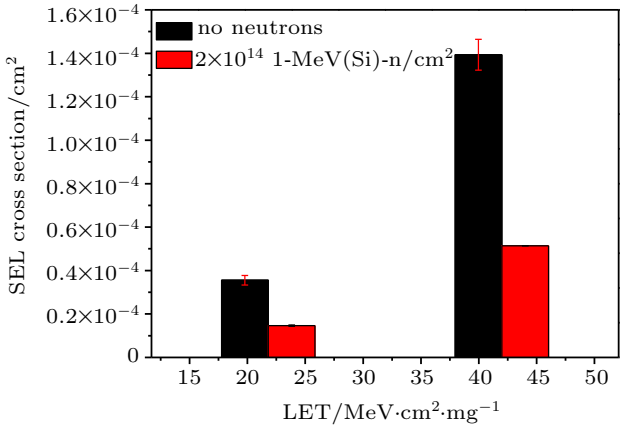


Fig. 2. (color online) Heavy ion SEL cross section versus ions' LET plotted on a log-linear scale to illustrate the difference between the pre- and post-neutron-irradiation chips.

From the heavy ion experiment, we can obtain the conclusion that the neutron irradiation fluence 2×10^{14} 1-MeV(Si)-n/cm^2 is not high enough to decrease the product of parasitic bipolar transistors' current gains below unity. The nonuniform nature of the neutron irradiation fluence also let the current gains' reduction become uncertain.

Another explanation of this phenomenon is the carrier removal induced by the neutron irradiation.[8] Many researchers have found that carrier removal as a result of neutron-induced displacement damage leads to an increase in the resistivity of doped silicon, which allows the well potential modulation from an ion strike to be larger in both time and spatial extent. After the neutron irradiation, the inherent resistivity will increase so that the well potential collapse becomes easier and possibly results in the parasitic transistors to be conductive. So the change in resistivity of the well and substrate is a restraining factor to this SEL hardening strategy.

4.2. Pulsed laser experiment

Pulsed laser is a powerful tool for studying SEEs in ICs, it is an important supplement for the heavy ion experiment. Although the charge generation profiles of pulsed lasers are different from those of heavy ions, the pulsed laser experiment allows the observed SEEs to be correlated with the time and location of the strike. When access to the top side is blocked by the metal layers just like the situation in Fig. 3, the laser light should be directed through the wafer from the back side.[9]

In this work, the pulsed laser experiment was carried out with the Nd: YAG laser of NINT. Because the IDT6116SA45P is packaged in a double in-line package (DIP), which is difficult for back thinning, the SRAM chip CY7C1021CV33 packaged in a thin small outline package (TSOP) from a Cypress Semiconductor was chosen as the DUT. The SRAM chips were written with the initial data "0x5555". Before the pulsed laser experiment, the chips were thinned to the silicon substrate by the four-axis polishing platform. The wavelength of the laser we used is 1064 nm, for which the light has a sufficiently long penetration depth to reach sensitive volumes.

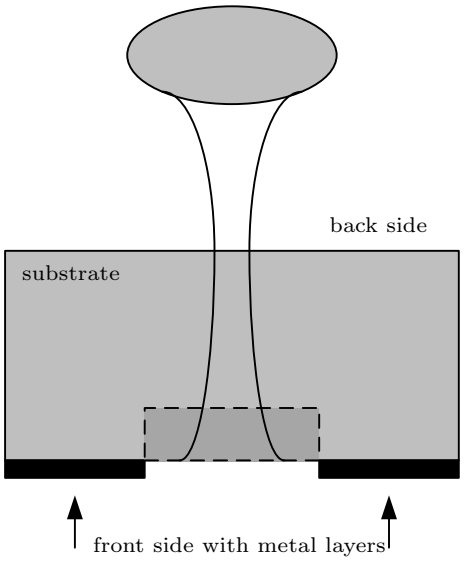


Fig. 3. Backside laser irradiation with laser focused on the back surface of the chip.

In Fig. 4, the SEL thresholds of the chips are almost the same for the pre- and post-neutron-irradiation chips. The pulsed laser SEL threshold is around 4 nJ if the silicon substrate is thinned 100 μm. The pulsed laser SEL cross section of the chip without neutron irradiation is nearly 2 or 3 times of that of the chip with neutron irradiation fluence 2×10^{14} 1-MeV(Si)-n/cm^2. The result of the pulsed laser experiment is the same as that of the heavy ion experiment.

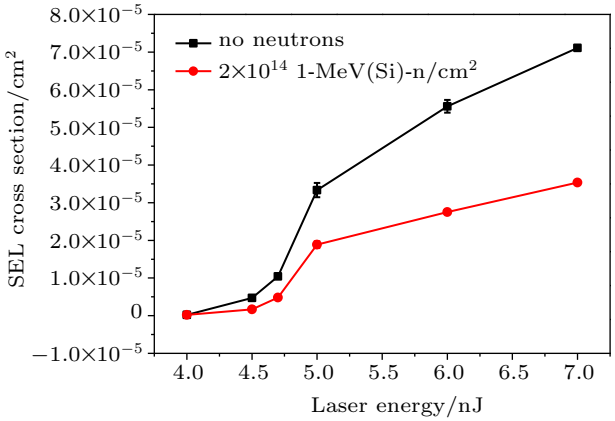


Fig. 4. (color online) Pulsed laser SEL cross section versus laser energy plotted on a log-linear scale to illustrate the difference between the responses of the pre- and post-neutron-irradiation chips.

5. TCAD simulation

For further study of the impact of the neutron-induced displacement damage on the SEL sensitivity of bulk CMOS SRAM, one 2D CMOS inverter model was built after model calibration by the Sentaurus TCAD simulation tool. Using this

model, we can simulate the heavy ion injection process and obtain the current waveforms of the critical points.

To verify the validity of the model, the heavy ions' strike was simulated at the junction of the N-well and P-substrate with different LET values, and the total currents of the PMOS source region were recorded as shown in Fig. 5. As we can see, the heavy ions whose LET is below 0.155 pC/μm will not cause latchup; it is just a current disturbance induced by the ion strike as time goes on. When the LET of the heavy ion exceeds 0.155 pC/μm, the SEL phenomenon can be easily observed and the SEL current is nearly 4 mA.

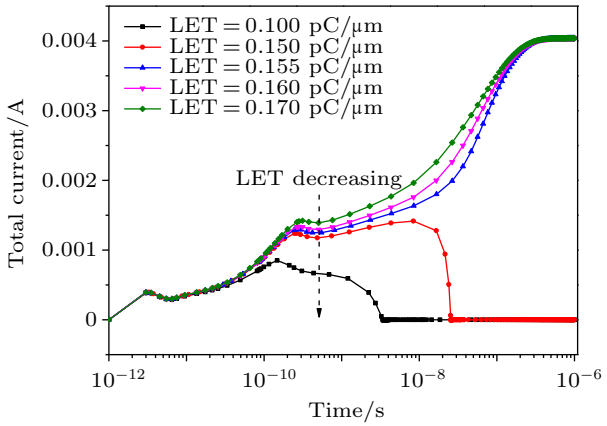


Fig. 5. (color online) Simulated total current of the PMOS source region versus time. Note that the unit of LET used in TCAD simulation is pC/μm, and the conversion of units is 1 pC/μm= 96.608 MeV·cm^2·mg^{-1}.

From Srour's study in 1979,[10] the relationship between the minority carrier lifetime and the neutron irradiation fluence is

$$\frac{1}{\tau_{\rm r}} = \frac{1}{\tau_{\rm r0}} + \frac{\Phi}{K_{\rm r}}, \tag{1}$$

where $\tau_{\rm r0}$ is the minority carrier lifetime before the neutron irradiation, $\tau_{\rm r}$ is the minority carrier lifetime after the neutron irradiation, Φ is the neutron fluence, and $K_{\rm r}$ is the minority carrier lifetime damage coefficient. According to the study result of Srour, $K_{\rm r}$ can be 7×10^6 n·s/cm^2 when the energy of the neutron fluence exceeds 10 keV. Moreover, the lifetimes of electrons and holes are set as 1×10^{-6} s (the typical carrier lifetime in TCAD specification) in our CMOS inverter model. When these parameters are put into formula (1), the lifetimes of electrons and holes after the neutron irradiation can be calculated.

As shown in Fig. 6, the lifetimes of electrons and holes change in the TCAD simulation model's parameter file with the increase of the neutron fluence. The LET of the heavy ion is constant 0.78 pC/μm (75 MeV·cm^2·mg^{-1}), which is meaningful for the SEL hardening in space. Similarly, we obtained the total current of the PMOS source region.

With the neutron irradiation fluence increasing, latchup becomes difficult. From these curves, we can obviously see that latchup will not occur if the neutron fluence exceeds 2×10^{13} 1-MeV(Si)-n/cm^2, beyond which the current gains' product of our simulation model is below unity.

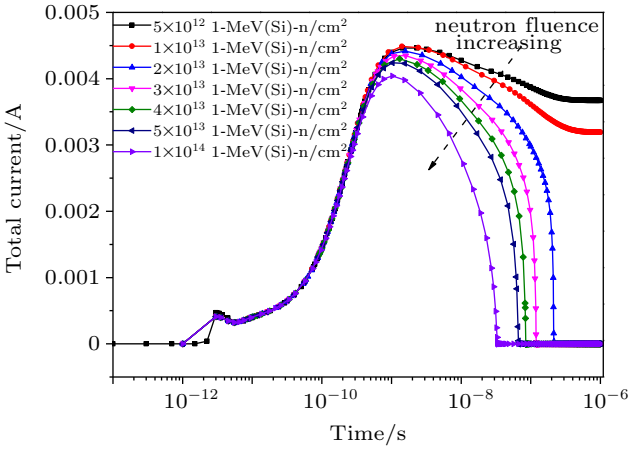


Fig. 6. (color online) Simulated total current of the PMOS source region versus time. Note that the LET of the heavy ion is constant 0.78 pC/μm= 75 MeV·cm^2·mg^{-1}, which is meaningful for the SEL hardening in space.

The simulation results above tell us that it is feasible to use neutron irradiation prior as a SEL hardening strategy. It is important to note that the carrier lifetime of the commercial SRAM chip is related to the chip's material and process, which are difficult to obtain, so the result of TCAD simulation can only be a reference for qualitative analysis.

For further study, we should know more details about the technological parameters of the COTS SRAMs to make the CMOS inverter model more accurate. More experiments are necessary to find the best neutron irradiation fluence for the COTS SRAM chips of different feature sizes.

6. Summary and conclusion

The impact of the neutron-induced displacement damage on the SEL sensitivity of bulk CMOS SRAM has been studied. Firstly, the test results of J750EX establish that neutron irradiation prior has negligible impact on the performance of SRAM chips. Then, both the results of heavy ion experiment and pulsed laser experiment show a decrease in the SEL cross section of the bulk CMOS SRAM after neutron irradiation. The chip without neutron irradiation has an almost 2 or 3 times higher SEL cross section than the chip with neutron irradiation fluence 2×10^{14} 1-MeV(Si)-n/cm^2. However, not only the heavy ion experiment but also the pulsed laser experiment tells us that the neutron fluence 2×10^{14} 1-MeV(Si)-n/cm^2 is not high enough to avoid the SEL. More experiments are necessary. What is more, a typical 2D CMOS inverter simulation model was built. The simulation results demonstrate the effectiveness of this hardening strategy.

In conclusion, neutron irradiation prior is a post-processing method which is suitable for the COTS SRAM chips because the neutron fluence from the fast burst reactor facility will not impact the function of the chips even if the fluence is very high. More experiments should be carried out to find the optimum neutron irradiation fluences for the COTS SRAMs of different feature sizes, which will provide strong and firm support for the use of COTS SRAM in space.

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