A novel P-channel SOI LDMOS structure with non-depletion potential-clamped layer*

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A novel structure is proposed for doubling the vertical breakdown voltage of silicon-on-insulator (SOI) devices. In this new structure, the conventional buried oxide (BOX) in an SOI device is split into two sections: the source-section BOX and the drain-section BOX. A highly-doped Si layer, referred to as a non-depletion potential-clamped layer (NPCL), is positioned under and close to the two BOX sections. In the split BOXes and the Si region above the BOXes, the blocking voltage (BV) is divided into two parts by the NPCL. The voltage in the NPCL is clamped to be nearly half of the drain voltage. When the drain voltage approaches a breakdown value, the voltage sustained by the source-section BOX and the Si region under the source are nearly the same as the voltage sustained by the drain-section BOX and the Si region under the drain. The vertical BV is therefore almost doubled. The effectiveness of this new structure was verified for a P-channel SOI lateral double-diffused metal-oxide semiconductor (LDMOS) and can be applied to other high-voltage SOI devices. The simulation results show that the BV in an NPCL P-channel SOI LDMOS is improved by 55% and the specific on-resistance ($R_{on,sp}$) is reduced by 69% in comparison to the conventional structure.

Keywords: breakdown voltage (BV), silicon-on-insulator (SOI), buried oxide (BOX), P channel

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1. Introduction

Silicon-on-insulator (SOI) technology[1,2] is competitive in comparison to bulk Si technology because of its small isolation area, immunity to latch-up,[3] and radiation hardening[4,5] characteristics. The breakdown voltage (BV), a key parameter, is mainly limited by the vertical BV in the SOI device.[6] Increasing the electrical field in a buried oxide (BOX) is an effective way to improve the vertical BV.[7] The membrane SOI device etching the Si substrate below the BOX eliminates the vertical BV limit and boosts the BV in the SOI device.[8,9]

In this paper, a novel structure is proposed to improve the vertical BV limit in an SOI device. In this new structure, one BOX is split into two sections: the source-section BOX and the drain-section BOX. A highly-doped Si layer, referred to as a non-depletion potential-clamped layer (NPCL), is positioned under and close to the two BOX sections. When the new structure is in a blocking state, the blocking voltage is divided into two parts with the assistance of the NPCL. When the device is approaching the BV, the voltage in the NPCL is nearly half of the BV. The voltage sustained by the source-section BOX and the Si region under the source is almost equal to the voltage sustained by the drain-section BOX and the Si region under the drain. Therefore, the vertical BV is doubled. This new structure was verified for a P-channel SOI lateral double-diffused metal-oxide semiconductor (LDMOS) and achieved good results in this study because the vertical BV of a P-channel SOI LDMOS is low as a result of the connection method used for the circuit.[10]

2. Mechanism and device structure

The novel structure proposed in this paper was verified for an NPCL P-channel SOI LDMOS. The NPCL P-channel SOI LDMOS and the conventional P-channel SOI LDMOS are also referred to as the proposed structure and conventional structure, respectively. In the proposed structure, the NPCL is made up of highly-doped N-type Si. The conventional BOX is split into two sections, with an Si window in the middle. The NPCL is positioned under and close to the two BOX sections. One is the source-section BOX, and the other is the drain-section BOX. A schematic cross-sectional view of the proposed structure is shown in Fig. 1. In this figure, L_d and N_d are the length and concentration of the P drift region, respectively; L_w is the silicon window length; T_d is the thickness of the P drift region; T_I is the thickness of the BOX; and T_{NPCL} is the thickness of the NPCL. The connection method in the circuit of a P-channel SOI LDMOS can be simplified so that the

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gate and source are connected to a ground while the drain and substrate are connected to the negative voltage terminal.[10]

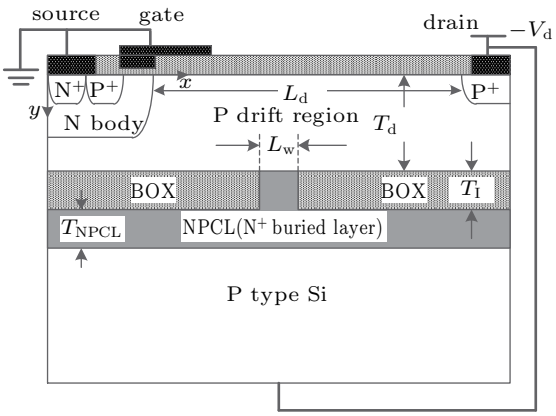


Fig. 1. Schematic cross section view of NPCL P channel SOI LDMOS.

Reduced surface field (RESURF) technology and field plates are used to improve the lateral BV. Therefore, the vertical BV becomes the limiting factor in the device's BV. In a conventional P-channel SOI LDMOS, the N body region and P drift region form a diode D1, shown in Fig. 2(a). When a high negative voltage is applied to the drain and substrate,[10] the voltage drop is mainly sustained by the diode D1. This means that the source-side BOX and the Si region under the source mainly sustain the voltage drop, and this limits the vertical BV.

In the proposed structure, when the applied voltage increases, the depletion region expands to the right. Because the NPCL is made up of a highly-doped N type layer, its potential is boosted and remains uniform after the depletion region is reached. As a result of the boosted potential of the NPCL, the drain-section BOX and the Si region under the drain also sustain a voltage drop. When the proposed structure approaches the BV, the voltage sustained by the drain-section BOX and Si region under the drain is nearly equal to the voltage sustained by the source-section BOX and the Si region under the source, and the voltage in the NPCL is almost half of the BV. Therefore, the BV is almost doubled.

To further illustrate the functioning of the proposed structure, a line labelled $AA'BB'C'CD$ is drawn around the BOX and Si regions in Figs. 2(a) and 2(b). Figure 2(a) shows a conventional P-channel SOI LDMOS, also referred to as a conventional structure. Figure 2(b) shows the proposed structure. The voltage drop along line $AA'BB'C'CD$ is equal to the BV sustained by the device.

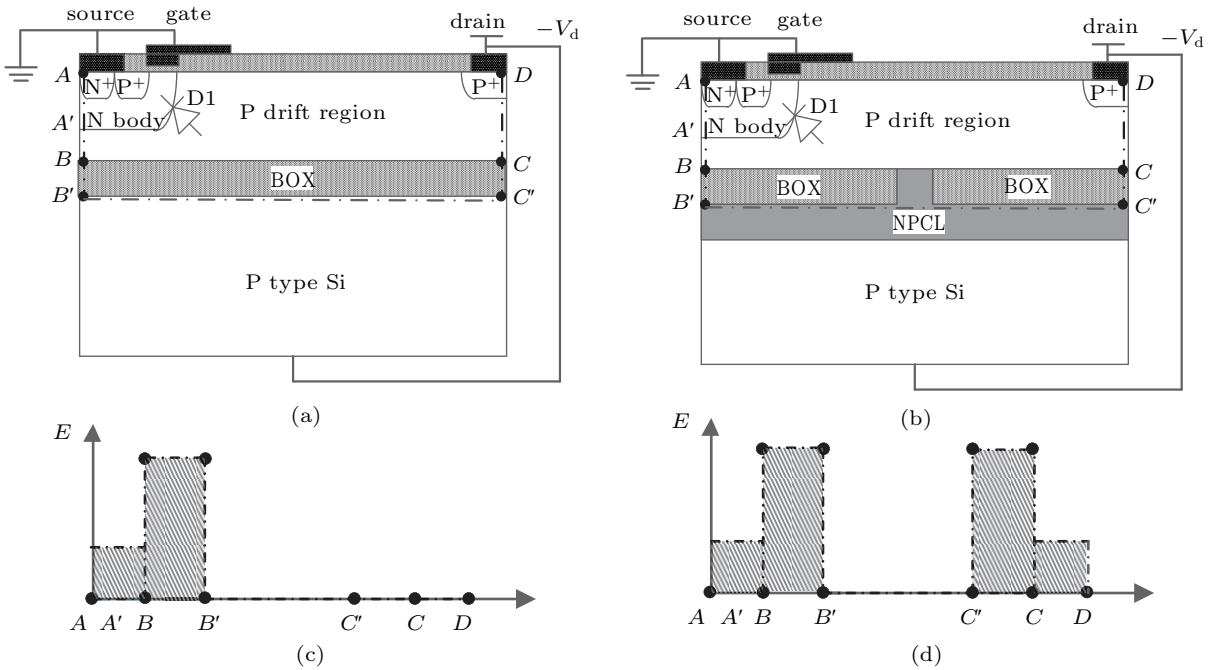


Fig. 2. (a) Line $AA'BB'C'CD$ around conventional P channel SOI LDMOS, (b) line $AA'BB'C'CD$ around NPCL P channel SOI LDMOS, (c) electric field around line $ABB'C'CD$ in panel (a), and (d) electric field around line $AA'BB'C'CD$ in panel (b).

The schematic diagrams of the electrical field along line $AA'BB'C'CD$ in the conventional structure and the proposed structure are shown in Figs. 2(c) and 2(d), respectively. In Fig. 2(c), the high electrical field along line ABB' shows that the source-side BOX and the Si region under the source sustain the voltage, whereas the electrical field along line C'CD is low. The drain-side BOX and the Si region under the drain hardly sustain any voltage. The following formula describes the situation: $\mathrm{BV}' = E_I \times T_I + E_{Si} \times T_d = V_{BOX} + V_{Si} = \mathrm{BV}$. In Fig. 2(d), in which the conventional BOX is split into two sections with the NPCL, the high electrical field along line $AA'BB'$ shows that the source-section BOX and the Si region under the source sustain voltage, whereas the high electrical field along line $C'CD$ shows that the drain-section BOX and

the Si region under the drain also sustain voltage in the proposed structure. The following formula describes this situation: $\mathrm{BV}' = 2E_{\mathrm{I}} \times T_{\mathrm{I}} + 2E_{\mathrm{Si}} \times T_{\mathrm{d}} = 2V_{\mathrm{BOX}} + 2V_{\mathrm{Si}} = 2\mathrm{BV}$. The proposed structure can sustain a nearly doubled BV. It should be noted that in the above discussion, it is assumed that the electrical fields around the source region and the drain region are equal for brief periods of time. Differences between the N body region, the source region, and the drain region cause the real situation to be slightly different.

3. Results and discussion

The simulation results for the electrical field distribution are shown in Fig. 3. The one-dimensional (1-D) electrical field distribution along line $AA'BB'C'CD$ in Figs. 2(a) and 2(b) are plotted in Fig. 3(a). CS denotes the conventional structure. The hollow symbols represent the electrical field along line $AA'BB'C'CD$ in the conventional structure at the BV. The points A, A',…,D in Fig. 3(a) indicate the electrical field at those locations in Fig. 2(a). The peak value of A', located at the edge of the N body and P drift regions, is 2.7×10^5 V·cm^{-1}. The peak value of B on the Si side is 2.4×10^5 V·cm^{-1}, and the peak value of B on the BOX side is 7.1×10^5 V·cm^{-1}. This is consistent with the electrical displacement continuity equation for the edge between the Si and the BOX: $E_{\mathrm{I}} = E_{\mathrm{sc}}\varepsilon_{\mathrm{s}}/\varepsilon_{\mathrm{I}} + q\sigma_{\mathrm{in}}/\varepsilon_{\mathrm{I}}$.[11] The electrical fields of the peak C', C, and D are extremely low and hardly contribute to sustaining the BV. The BV is −202 V in the conventional structure. PS in Fig. 3(a) denotes the proposed structure. The solid symbols represent the electrical field along line $AA'BB'C'CD$ in the NPCL P-channel SOI LDMOS at the BV. The electrical field of peak A' is 2.5×10^5 V·cm^{-1}. The peak B on the Si side is 1.3×10^5 V·cm^{-1}, and the peak B on the BOX side is 3.7×10^5 V·cm^{-1}. The electrical field along line $B'C'$ is small. The boosted equipotential of the NPCL makes the drain-section BOX and the Si region under the drain sustain a high electrical field. The electrical field of the peak C' is 6.9×10^5 V·cm^{-1}. The peak C on the BOX side is 7.0×10^5 V·cm^{-1}, and the peak C on the Si side is 2.3×10^5 V·cm^{-1}. The BV of the proposed structure is −313 V, a 55% improvement over that of the conventional structure. The electrical fields along lines BB' and $C'C$ are not symmetric because of the asymmetry between the source and drain regions in the real device.

The three-dimensional (3-D) electrical field distributions within the devices can be seen clearly in Figs. 3(b) and 3(c). As figure 3(b) shows, in the conventional structure, only the source-side BOX and the Si region under the source sustain an electrical field. As figure 3(c) shows, in the proposed structure, the source-section BOX, the Si region under the source, the drain-section BOX, and the Si region under the drain all sustain an electrical field. This boosts the BV of the device.

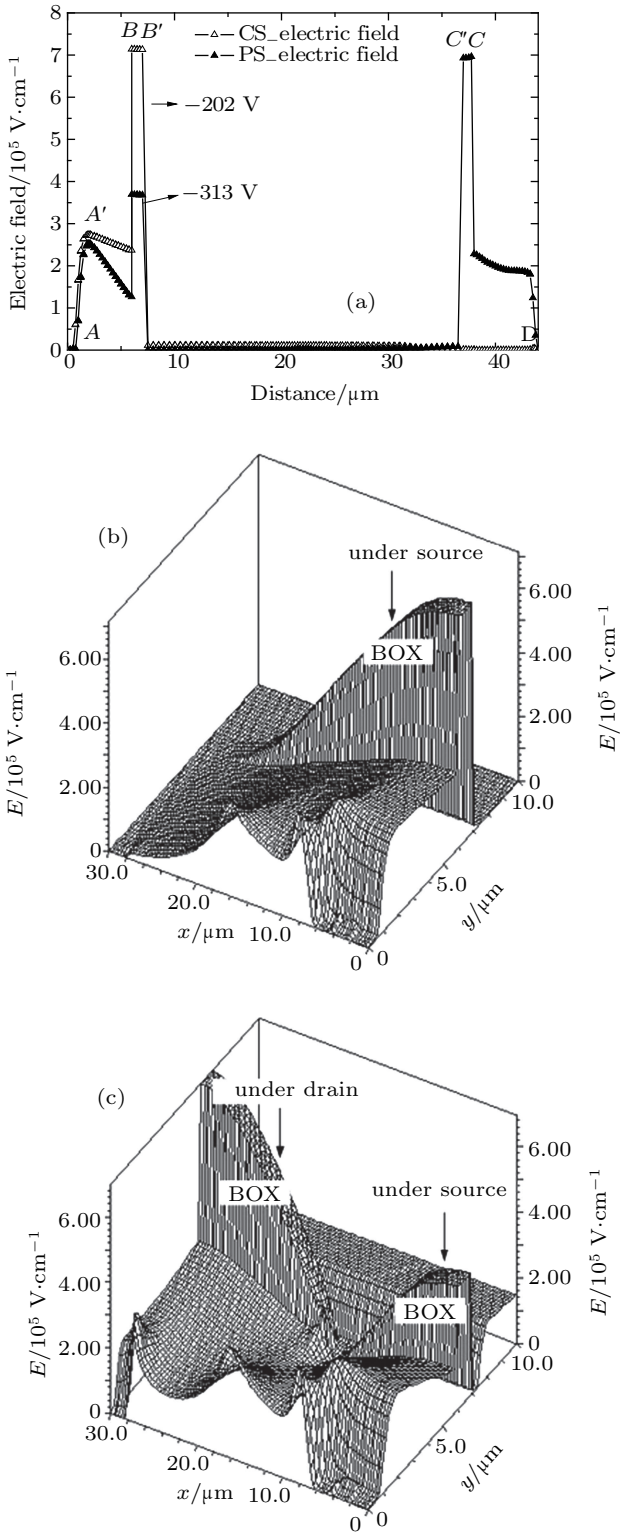


Fig. 3. (a) 1-D electric field distributions along line $ABB'C'CD$ of conventional P channel SOI LDMOS and NPCL P channel SOI LDMOS, (b) 3-D electric field distributions in conventional P channel SOI LDMOS, and (c) 3-D electric field distributions in NPCL P channel SOI LDMOS. ($T_{\mathrm{d}} = 6$ μm, $T_{\mathrm{I}} = 1$ μm, $L_{\mathrm{d}} = 20$ μm, $L_{\mathrm{w}} = 1$ μm.)

The surface electrical field distributions associated with different V_{ds} for the conventional structure and proposed structure are plotted in Fig. 4. The device parameters are identical to those in Fig. 3. The locations of the points I, II, and III are shown in the inset diagram in Fig. 4. V_{ds} was

gradually increased to investigate the difference in the surface electrical field between the conventional structure and the proposed structure. When V_{ds} was increased to -100 V, the electrical field at point *I* was 1.9×10^5 V·cm^{-1}, the electrical field at point *II* was 1.6×10^5 V·cm^{-1}, and the electrical field at point *III* was nearly 0. V_{ds} was gradually increased until a BV of -202 V was reached. The electrical field at point *I* was then 3.8×10^5 V·cm^{-1}, the electrical field at point *II* was 3.0×10^5 V·cm^{-1}, and the electrical field at point *III* was only 0.2×10^5 V·cm^{-1}. These results indicate that the conventional structure mainly sustains the BV by diode D1 (shown in Fig. 2(b)). In contrast, in the proposed structure, when a V_{ds} of -202 V was applied, the electrical field at point *I* was 3.7×10^5 V·cm^{-1}, the electrical field at point *II* was 3.0×10^5 V·cm^{-1}, and the electrical field at point *III* was nearly 0. This situation is similar to that in the conventional structure. However, when V_{ds} was increased steadily, the potential of the NPCL was boosted and contributed to making the drain-section BOX and the Si region under the drain sustain the BV. The proposed structure thus achieved a much higher BV of -313 V. The electrical field at point *I* was 3.8×10^5 V·cm^{-1}, the electrical field at point *II* was 3.0×10^5 V·cm^{-1}, and the electrical field at point *III* was nearly 2.8×10^5 V·cm^{-1}. The enhanced electrical field at point *III* contributes to the higher BV.

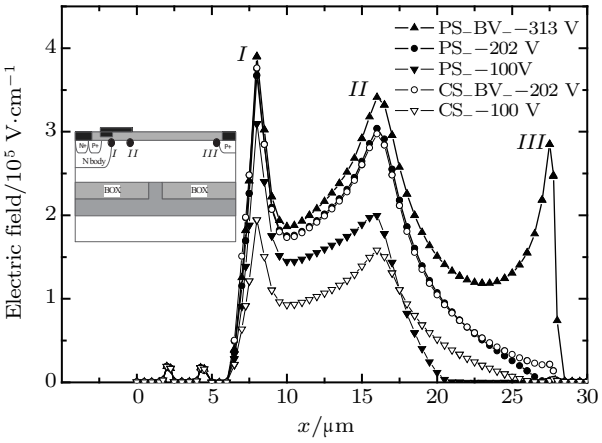


Fig. 4. Surface electric field of conventional and NPCL P channel SOI LDMOS at various drain voltage.

To illustrate the effect of the Si window length on the BV in the proposed structure, the BVs are plotted as a function of L_w in Fig. 5. The functions of L_w were simulated with different T_I values. The BV achieved by the proposed structure increases with the BOX thickness. For a BOX thickness of 1 μm, the BV is -313 V for $L_w = 1$ μm, 241V for $L_w = 8$ μm, and -167 V for $L_w = 16$ μm. The BV decreases as L_w increases. The reason for this is that the permittivity of SiO_2 is much lower than that of Si, and hence the BOX can sustain a higher electric field when L_w is shorter. As L_w increases, the BOX eventually becomes too short to support the electrical field, and the device's BV decreases.

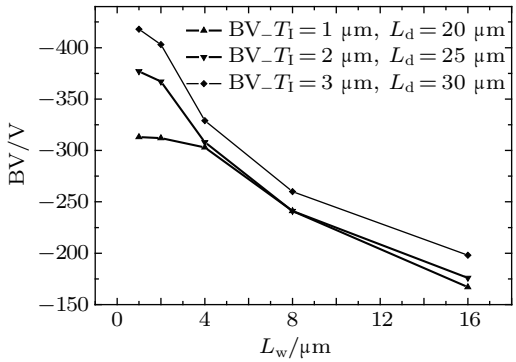


Fig. 5. BV versus L_ws of NPCL P channel SOI LDMOS.

The on-state characteristics of the conventional structure and the proposed structure are plotted in Fig. 6. In the conventional structure, diode D1 mainly sustains the voltage drop. The decreasing concentration in the P drift region contributes to sustaining a higher BV. However, beyond a certain concentration, breakdown occurs in the device because the maximum electrical field on the source side exceeds the critical electric field. With the help of a field plate, the conventional structure achieves a maximum BV of -202 V at $N_d = 4\times10^{14}$ cm^{-3}. The specific on-resistance ($R_{on,sp}$) is 32.3 Ω·mm^2 when V_g is -10 V and V_{ds} is -1 V.

In the proposed structure, the equipotential layer NPCL is boosted to a high voltage. This facilitates the drain-section BOX and the Si region under the drain sustaining the BV. The proposed structure achieves its maximum BV at a much higher N_d than the conventional structure. The maximum BV is -313 V at $N_d = 2\times10^{15}$ cm^{-3}, and $R_{on,sp}$ is 10 Ω·mm^2, for the same dimensions and test conditions as for the conventional one. $R_{on,sp}$ is reduced by 69% in the proposed structure.

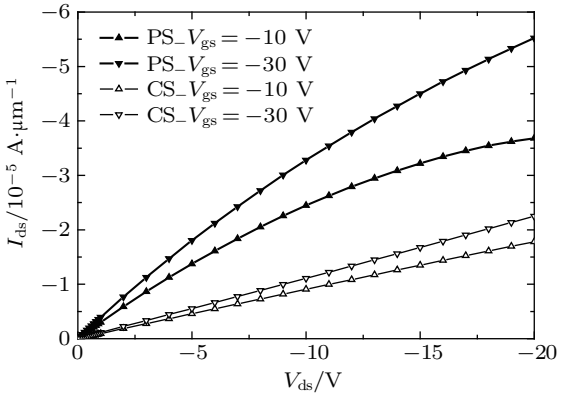


Fig. 6. I_{ds} as a function of V_{ds} of conventional and NPCL P channel SOI LDMOS ($L_d = 20$ μm, $T_d = 6$ μm, $T_I = 1$ μm, $L_w = 1$ μm).

The 3-D temperature profiles of the conventional structure and the proposed structure are shown in Fig. 7. In the

simulation, the substrate temperature was set to be 300 K, and V_g was set to be −15 V when the devices were under on-state conditions, with a power of 1 mW/μm. Figure 7(b) shows the 3-D temperature profile of the proposed structure. The Si window in the middle of the BOX provides a path to conduct heat away. The temperature profile is low around the Si window, and as a result, the temperature of the entire device is obviously reduced. The T_{max} of the conventional structure is 334.4 K, whereas the T_{max} of the proposed structure is only 318.9 K, a reduction of 15.5 K.

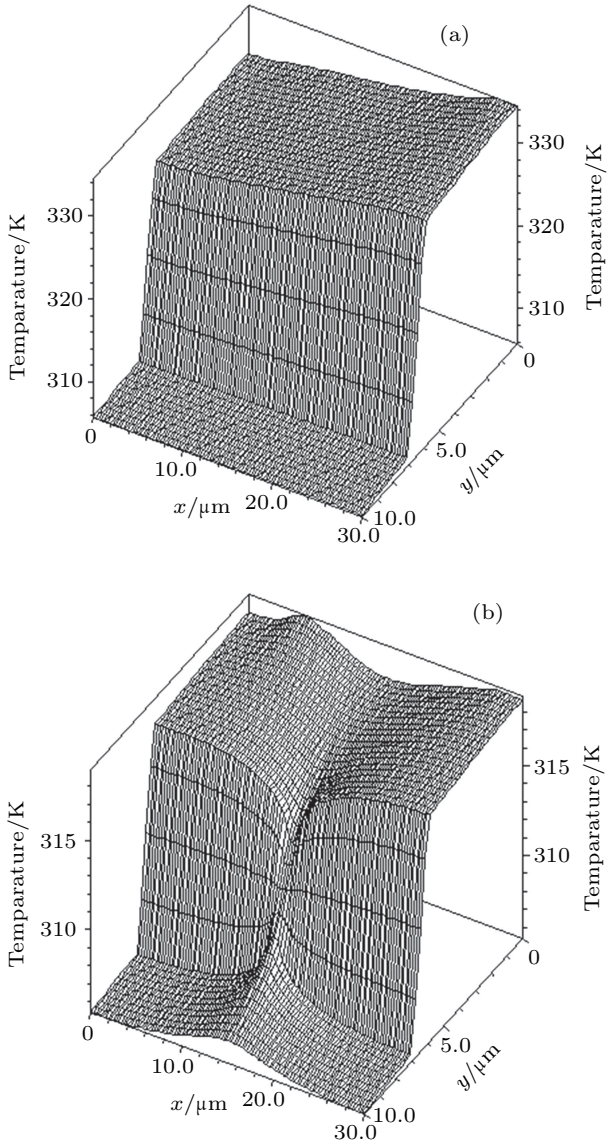


Fig. 7. 3-D temperature distribution in (a) conventional P channel SOI LDMOS, and (b) NPCL P channel SOI LDMOS. ($L_d = 20$ μm, $T_d = 6$ μm, $T_I = 1$ μm, $L_w = 1$ μm).

4. Conclusions

A novel structure is proposed in this paper for doubling the vertical breakdown voltage of silicon-on-insulator (SOI) devices. The proposed structure was verified for a P-channel NPCL SOI LDMOS by means of simulation. In this new structure, one BOX is split into two sections with the assistance of an NPCL. Under ideal conditions, the new structure can sustain nearly double the vertical BV that a conventional structure can sustain. The simulation results indicate that the BV is improved by 55% and the $R_{on,sp}$ is reduced by 69% in the proposed structure, in comparison to those in the conventional structure. Furthermore, the window in the middle of the BOXes alleviates the SHE, and T_{max} is reduced by 15.5 K in the proposed structure. Thus, the new structure is considered a promising technology for use in power SOI devices.

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