# Scaling dependence of memory windows and different carrier charging behaviors in Si nanocrystal nonvolatile memory devices*

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Based on the charge storage mode, it is important to investigate the scaling dependence of memory performance in silicon nanocrystal (Si-NC) nonvolatile memory (NVM) devices for its scaling down limit. In this work, we made eight kinds of test key cells with different gate widths and lengths by 0.13-μm node complementary metal oxide semiconductor (CMOS) technology. It is found that the memory windows of eight kinds of test key cells are almost the same of about 1.64 V @ ±7 V/1 ms, which are independent of the gate area, but mainly determined by the average size (12 nm) and areal density ($1.8\times10^{11}$/cm$^2$) of Si-NCs. The program/erase (P/E) speed characteristics are almost independent of gate widths and lengths. However, the erase speed is faster than the program speed of test key cells, which is due to the different charging behaviors between electrons and holes during the operation processes. Furthermore, the data retention characteristic is also independent of the gate area. Our findings are useful for further scaling down of Si-NC NVM devices to improve the performance and on-chip integration.

**Keywords:** silicon nanocrystals, nonvolatile memory, scaling dependence, different charging behaviors

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## 1. Introduction

Nanocrystal (NC) floating gate nonvolatile memory (NVM) devices based on a discrete charge storage concept have been considered as a good candidate for the next generation NVM devices.[1–7] According to this operation principle, the charge is stored in the isolated NCs instead of a conductive poly-crystal Si floating gate, a weakness in the tunneling oxide can only cause the charge loss in the individual NCs near the defect.[8,9] Consequently, the NC NVM devices can be less sensitive to the local oxide defects, which can reduce the leakage of the stored charge and make the data retention characteristics be effectively improved. Therefore, an ultrathin tunneling oxide layer of less than 4 nm can be used in the NC NVM devices, which show a low operating voltage and a high program/erase (P/E) speed. Due to the compatibility with the standard CMOS technology, Si-NC NVM devices have been widely studied.[10–16] However, with the scaling down of the device structures, the number of Si-NCs in the floating gate of the device decreases gradually, resulting in the reduction of the stored charge quantity in the device. Therefore, what effect the reduction of stored charge quantity has on the memory window becomes the critical issue for the real application of Si-NC NVM devices.

In this study, we fabricated eight kinds of Si-NC NVM test key cells with different gate widths and lengths by 0.13-μm node CMOS technology. The size and density of Si-NCs are evaluated from the atomic force microscope (AFM) and scanning electron microscope (SEM) images, and the device structure can be verified by the cross-section transmission electron microscopy (TEM) images. We systematically measured the memory performance of eight kinds of Si-NC NVM test key cells from 14 pieces of 8-inch wafer. The results show that the memory window and retention characteristics are independent of the gate area of the Si-NC NVM devices, which are confirmed by calculated results based on discrete charge storage mode. The P/E speed characteristics are also independent of the gate width and the length of the devices, only the charging behavior is different between electrons and holes in Si-NC NVM devices.

## 2. Experiments

The devices were fabricated on 8-inch p-type (100) Si wafer with the resistivity of 6–8 Ω·cm. After the standard cleaning process, an ultrathin tunneling oxide layer with a thickness of about 3.5 nm was grown by dry oxidization, and the Si-NC layer was deposited *in-situ* in the LPCVD system. Subsequently, the nitridation treatment of Si-NCs was carried out and a control gate $SiN_x$ layer with the thickness of 26 nm was deposited at the surface-nitrided Si-NCs by LPCVD. The details of sample fabrication can be found in our previous work.[17] As listed in Table 1, eight kinds of test key

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cells with different gate widths and lengths are defined. The topographic-view AFM, SEM images, and statistic size distribution for Si-NCs are shown in Fig. 1. The size distribution of Si-NCs is uniform and the average size is about 12 nm. The standard deviation (STDEV) and the monodispersity of size are evaluated to be 1.5 nm and 12.5%, respectively. The area density of Si-NCs is estimated to be about $1.8\times10^{11}$ cm$^{-2}$. The cross-section TEM images of the standard test key cell D along the gate length and width, and the high resolution cross-section TEM of Si-NC floating gate are shown in Fig. 2, which clearly shows that the floating gate stack consists of an ultra-thin tunneling oxide layer, a Si-NC storage layer, and a control gate $SiN_x$ layer. The gate width and length are estimated to be 0.16 μm and 0.176 μm, respectively. The memory performance of test key cells selected from 14 pieces of 8-inch wafer was measured by using an Agilent B1500A semiconductor parameter analyzer with a pulse generator.

**Table 1.** Eight kinds of test key cells with different gate widths and lengths.

| Test key cell | Gate length/μm | Gate width/μm | $\Delta S$ ($S_{\text{gate,cell}(n)}-S_{\text{gate,cell(D)}}$) /$10^3$ nm$^2$ [a] |
|---|---|---|---|
| A | 0.176 | 0.200 | 7.04 |
| B | … | 0.190 | 5.28 |
| C | … | 0.176 | 2.82 |
| D | … | 0.160 | 0 |
| E | … | 0.150 | –1.76 |
| F | … | 0.140 | –3.52 |
| G | 0.200 | 0.160 | 2.50 |
| H | 0.160 | … | –2.56 |

[a] $n$ =A, B, C, D, E, F, G, H.

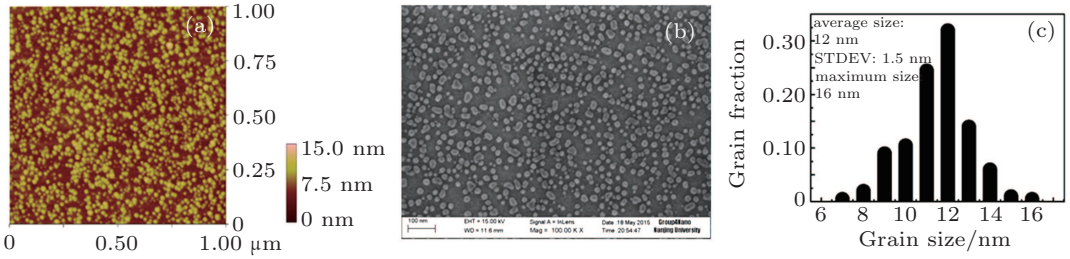



**Fig. 1.** (color online) The topographic-view (a) AFM and (b) SEM images of Si-NCs before nitridation. (c) The statistical size distribution of Si-NCs before nitridation.

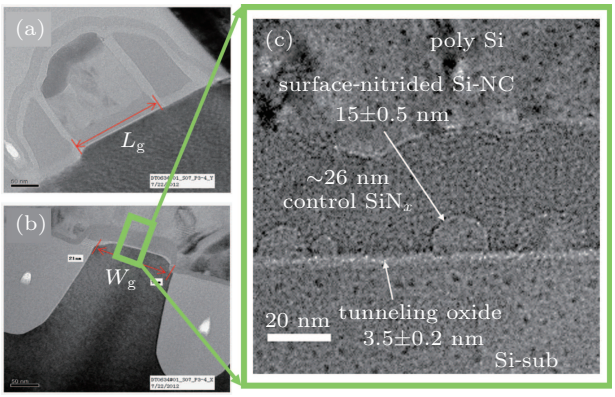



**Fig. 2.** (color online) The cross-section TEM images of test key cell D along the (a) gate length and (b) width. (c) The high resolution cross-section TEM image of the Si-NC floating gate structure.

## 3. Results and discussion

Figure 3 shows the transfer characteristics of five kinds of Si-NC NVM test key cells with different gate widths and lengths, i.e., test key cells A, G, D, H, and F. The transfer characteristics of the test key cells were measured at a constant of $V_D = 0.1$ V and the step interval of 50 mV. The five kinds of test key cells all show good transfer characteristics with low cut-off current ($\sim 10^{-13}$ A), high On/Off current ratio ($> 10^7$), and low subthreshold swing (~0.14 V/decade). It is beneficial to distinguish the program and erase states. In our previous work, we reported that the surface-nitrided Si-NC NVM devices show low subthreshold swing, which is due to good passivation of the Si-NC surface defect during the nitridation treatment.[17] After the erasing operation under a −7-V pulse voltage of 1 ms, the transfer characteristic curves of five kinds of test key cells are in good agreement with each other. After the programming operation under +7 V pulse voltage of 1 ms, the transfer characteristic curves are also in good agreement with each other. Then a memory window of about 1.64 V can be observed after programming and erasing operations.

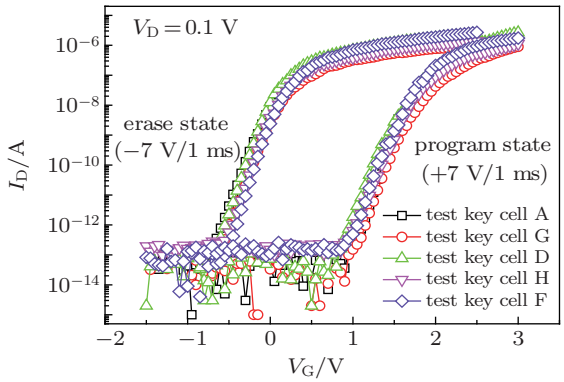



**Fig. 3.** (color online) Transfer characteristics of five kinds of Si-NC NVM test key cells with different gate widths and lengths after programming and erasing operations. Here, $V_D$ is the drain voltage, $I_D$ is the drain current, and $V_G$ is the gate voltage.

As shown in Fig. 3, the memory window of five kinds of Si-NC NVM test key cells with different gate widths and lengths are almost the same. Subsequently, we systematically study the relation of the memory window with the gate area. Figure 4 shows the measured and calculated results of the memory window distribution of Si-NC NVM test key cells with different gate areas. In our previous work, we reported that the electrical performance of test key cell D, which shows the characteristics of superior endurance, faster P/E speed, and good data retention.[17] Here, we take test key cell D as a reference cell. The $x$ axis represents the area difference between the gate and the reference cell ($\Delta S$). The programming and erasing conditions are $+7$ V and $-7$ V pulse voltages of 1 ms, respectively. The memory windows are defined as the $\Delta V_{\rm th}$ of program and erase states at which the drain current $I_{\rm D} = 1$ nA. As shown in Fig. 4, compared with that of reference test key cell D, the distribution of measured memory windows is about $1.64 \pm 0.2$ V with the decrease or increase of the gate areas of the Si-NC NVM test key cells, which means that the memory widow is independent of the gate area.

The charge and discharge behaviors for Si-NC NVM devices can be described by the charging effect of parallel plate capacitor. It is well known that the relation of the bias voltage ($V$) and charge quantity ($Q$) for parallel plate capacitor can be expressed by the following equation:

$$V = \frac{Q}{C} = \frac{Q}{\varepsilon_0 \varepsilon_{\rm r} A} d, \tag{1}$$

where $C$ is the capacitance of the parallel plate capacitor. Thus the voltage variation ($\Delta V$) of the parallel plate capacitor can be estimated by the following equation:

$$\Delta V = \frac{\Delta Q}{\varepsilon_0 \varepsilon_{\rm r} A} d, \tag{2}$$

where $\varepsilon_0$ is the effective permittivity, $\varepsilon_{\rm r}$ is the relative permittivity, $d$ is the plates separation, and $A$ is the area of the plates. For the Si-NC floating gate structure, $\Delta Q$ and $d$ can be expressed by the following equations:[1,18]

$$\Delta Q = qnN_{\rm dot}S, \tag{3}$$

$$d = t_{\rm con} + \frac{1}{2}\frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm Si}} t_{\rm dot}, \tag{4}$$

where $q$ is electron charge, $n$ is the number of charge stored in the individual Si-NC, $N_{\rm dot}$ is the areal density of Si-NCs, $S$ is the Si-NC floating gate area, $t_{\rm con}$ is the thickness of a control $SiN_x$ layer, $t_{\rm dot}$ is the linear dimension of Si-NC, $\varepsilon_{\rm ox}$ and $\varepsilon_{\rm Si}$ are the permittivities of an ultra-thin $SiO_2$ tunneling layer and Si-NCs, respectively. Therefore, the memory window ($\Delta V_{\rm th}$) of the Si-NC NVM device can be described as

$$\Delta V_{\rm th} = \frac{qnN_{\rm dot}}{\varepsilon_{\rm ox}} \left( t_{\rm con} + \frac{1}{2}\frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm Si}} t_{\rm dot} \right), \tag{5}$$

where $\Delta V_{\rm th}$ is mainly determined by the average size and areal density of Si-NCs. As shown in Fig. 1, the average size and areal density of Si-NCs are about 12 nm and $1.8\times10^{11}$ cm$^{-2}$, respectively. According to Eq. (5), if $n = 3$, namely, the number of electrons or holes stored in the individual Si-NC is three after the programming or erasing operation, we can obtain that both the electron and hole memory windows are about 0.7 V. Then a total memory window of about 1.4 V can be obtained, which is shown in Fig. 4. Similarly, if $n = 4$, a total memory window of about 1.86 V can be obtained, which is also shown in Fig. 4. The measured memory window of Si-NC NVM devices in Fig. 4 is about 1.64 V. According to Eq. (5), we can deduce that there are about 48% of Si-NCs stored three electrons or holes and 52% of Si-NCs stored four electrons or holes after programming or erasing operations. This is due to the dispersion of the size distribution of Si-NCs.

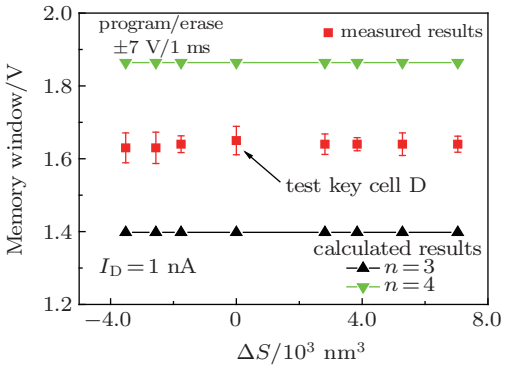



**Fig. 4.** (color online) Measured and calculated results of the memory window distribution of Si-NC NVM test key cells with different gate areas.

Figure 5 shows the P/E speed characteristics of Si-NC NVM test key cells under $\pm7$ V with varying pulse widths from 100 ns to 100 ms. Before the programming operation, the test key cells were set at the full erased state. While before the erasing operation, the test key cells were set at the full programmed state. As shown in Fig. 5, $\Delta V_{\rm th}$s increase with the increase of the pulse widths for both program and erase states at the beginning, which means that the electrons or holes are starting charging processes. With the pulse widths increasing further, $\Delta V_{\rm th}$s for the program state reach saturation after programming under $+7$-V pulse voltage of 1 ms, which means that Si-NCs can be fully charged by electrons in 1 ms. Whereas in the erase process, Si-NCs can be fully charged by holes in 10 μs, which means that the erase speed is faster than the program speed. This is because of the different charging behaviors between electrons and holes in Si-NC NVM devices on the p-type Si substrate. In order to explain it, we first emphasize that electrons and holes are injected through the tunneling oxide layer from the Si substrate into Si-NCs mainly by the direct tunneling mechanism,[19,20] which was verified by $I_{\rm gs}$–$V_{\rm gs}$ measurements of Si-NC NVM test key cells (not shown here). In this study, under the operation bias voltage of $+7$ V, the effective voltage on the tunneling oxide layer is only about 1.2 V. It means that the car-

rier tunneling barrier is about 1.2 eV. This value is much lower than the tunneling barrier height of the $SiO_2$/p-Si interface barrier in the Fowler–Nordheim (FN) tunneling model, which is about 3.4 eV.[18,21,22] During the erasing operation processes under a negative voltage, the holes as the majority carriers in p-Si substrate can be directly injected into Si-NCs. However, during the programming operation processes under a positive voltage, an n-channel inversion layer should be formed firstly, which requires extra time for the depletion of holes in the p-Si substrate. Subsequently, the electrons can be injected into Si-NCs from the n-channel inversion layer. Thus, the charging time of electrons is longer than that of holes, resulting in that the erase speed is faster than the program speed. As reported in Refs. [23] and [24], the response time of the majority carriers in the metal–oxide–semiconductor (MOS) capacitor is on the order of nanoseconds, whereas that of minority carriers is on the order of microseconds. Furthermore, figure 5(a) shows the effect of gate length on P/E speed characteristics of test key cells with a fixed gate width of 0.16 μm, the speeds are almost unchanged with the decrease of the gate length from 0.2 μm to 0.16 μm. Figure 5(b) shows the effect of gate width on P/E speed characteristics of test key cells with a fixed gate length of 0.176 μm, the speeds are also almost unchanged with the decrease of the gate width from 0.2 μm to 0.14 μm. It indicates that the P/E speed characteristics of Si-NC NVM devices are independent of the gate length and width.

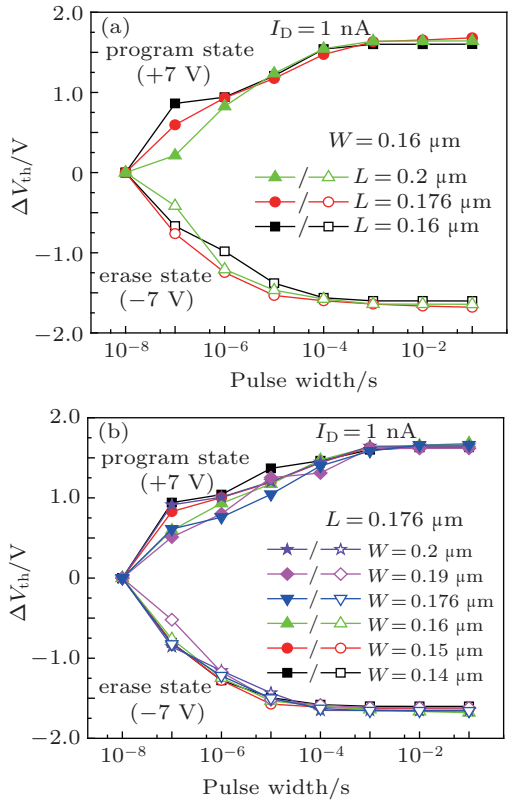



**Fig. 5.** (color online) Program and erase speed characteristics of Si-NC NVM test key cells with (a) different gate lengths $L$ and (b) different gate widths $W$.

Figure 6 shows the transient memory window as a function of retention time of test key cells A and F at room temperature. The test key cells were programmed and erased under ±7 V pulse voltages of 1 ms. The erase state and program state are selected as the initial states of electron and hole memory windows, respectively. As listed in Table 1, test key cells A and F are Si-NC NVM cells with the biggest and smallest gate areas of $3.52\times10^4$ nm$^2$ and $2.46\times10^4$ nm$^2$, respectively. Figure 6 shows that both test key cells A and F show good data retention characteristics with the charge loss rate of about 20% after $10^5$ s, both of their electron windows and hole windows decrease quickly at the beginning of the measurement, and then become more and more stable with the increase of retention time. Comparing test key cells A and F, there are no obvious differences of the charge loss rate between them, which means that the data retention characteristic is independent of the gate area of Si-NC NVM devices. As shown in Fig. 1, the areal density of Si-NCs is about $1.8\times10^{11}$ cm$^{-2}$, thus the numbers of Si-NCs in the floating gate layers of test key cells A and F are 63 and 44, respectively. There is more charge stored in the Si-NC floating gate layer of test key cell A than that of test key cell F. However, as described in Eq. (5), $\Delta V_{th}$ is dependent on the stored charge density, which is determined by the areal density of Si-NCs and the number of stored charge in individual Si-NC. For the test key cells A and F, both their average sizes of Si-NCs are about 12 nm, thus they have the same average number of charge stored in each Si-NC. As the charge loss probability of each Si-NC is constant, the charge loss per unit area of test key cell A is equal to that of test key cell F, thus, we can observe that $\Delta V_{th}$s of test key cells A and F show the same decrease after $10^5$ s.

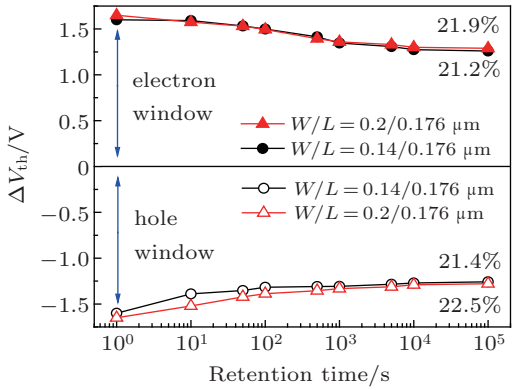



**Fig. 6.** (color online) Retention characteristics of the test key cells A and F at room temperature.

## 4. Conclusion

The Si-NC NVM devices with different gate widths and lengths have been systematically investigated. It is found that the memory windows of test key cells are independent of the gate area, but mainly determined by the average size and areal density of Si-NCs. The erase speed is faster than the program

speed due to the different charging behaviors between electrons and holes. The P/E speed characteristics are almost independent of the gate width and length. Furthermore, the data retention characteristic is also independent of the gate area. These results indicate that Si-NC NVM devices can be further scaled down for improving the performance and on-chip integration.

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