Effect of NO annealing on charge traps in oxide insulator and transition layer for 4H-SiC metal–oxide–semiconductor devices*

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The effect of nitric oxide (NO) annealing on charge traps in the oxide insulator and transition layer in n-type 4H–SiC metal–oxide–semiconductor (MOS) devices has been investigated using the time-dependent bias stress (TDBS), capacitance–voltage (*C*–*V*), and secondary ion mass spectroscopy (SIMS). It is revealed that two main categories of charge traps, near interface oxide traps ($N_{\rm niot}$) and oxide traps ($N_{\rm ot}$), have different responses to the TDBS and *C*–*V* characteristics in NO-annealed and Ar-annealed samples. The $N_{\rm niot}$ are mainly responsible for the hysteresis occurring in the bidirectional *C*–*V* characteristics, which are very close to the semiconductor interface and can readily exchange charges with the inner semiconductor. However, $N_{\rm ot}$ is mainly responsible for the TDBS induced *C*–*V* shifts. Electrons tunneling into the $N_{\rm ot}$ are hardly released quickly when suffering TDBS, resulting in the problem of the threshold voltage stability. Compared with the Ar-annealed sample, $N_{\rm niot}$ can be significantly suppressed by the NO annealing, but there is little improvement of $N_{\rm ot}$. SIMS results demonstrate that the $N_{\rm niot}$ are distributed within the transition layer, which correlated with the existence of the excess silicon. During the NO annealing process, the excess Si atoms incorporate into nitrogen in the transition layer, allowing better relaxation of the interface strain and effectively reducing the width of the transition layer and the density of $N_{\rm niot}$.

Keywords: 4H–SiC metal–oxide–semiconductor devices, NO annealing, near interface oxide traps, oxide traps

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1. Introduction

Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) are expected to replace Si-based MOSFETs for high-temperature and high-power applications, owing to its superior material properties such as high critical breakdown electric field strength, high electron saturation velocity, and high thermal conductivity. Besides its super desirable properties, stable silicon dioxide (SiO_2) insulator on silicon carbide can be formed by conventional thermal oxidation, which makes the SiC device fabrication process easier compared with other wide band gap semiconductors. In the light of these advances, SiC MOSFETs are poised to become the main power control switch over pre-existing Si-based devices, offering substantial advantages in applications where high power, temperature, and frequency are required.[1–6]

In recent years, SiC MOSFETs have become commercially available. However, their performance is still far from theoretical limits. Typically, former researchers have attributed the low channel mobility to the large density of interface traps ($N_{\rm it}$) located at the SiO_2/4H–SiC interface.[7,8] Many attempts were applied to reduce the density of $N_{\rm it}$ and improve the channel mobility, but it is still much lower than the bulk mobility of SiC material.[9–11] Thus, many recent studies have focused on the charge traps in the SiO_2 insulator, in which some results on the instability of the threshold voltage have provided evidence for the existence of charge traps in the insulator of 4H–SiC MOS devices.[12–14] Moreover, recent works have shown that charge traps near the interface can exchange charge with the semiconductor readily, which may significantly affect the performance and the reliability of SiC MOS devices.[15,16] However, previous research on this issue has almost ignored the distinction between near interface oxide traps ($N_{\rm niot}$) and oxide trap ($N_{\rm ot}$). A more serious problem is that the distribution of these charge traps in the SiO_2 insu-

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lator is not very clear, especially the region where the $N_{\rm niot}$ exist. Meanwhile, a better understanding of the mechanism is required to account for the property of these charge traps in the SiO_2 insulator.

It has been confirmed that n-channel MOSFET operated in strong inversion (in a positive gate bias) can be equivalent to an n-type MOS capacitor in the accumulation state, in terms of the possible interaction between the surface electrons and the charge traps at and near the SiO_2/SiC insulator interface. Therefore, it is possible to utilize an n-type MOS capacitor to characterize the SiO_2/SiC interfacial properties, instead of a complete n-channel MOSFET.

In this paper, time-dependent positive bias stress measurements are applied on n-type 4H–SiC MOS capacitors annealed in Ar and NO ambiences. The bidirectional high-frequency capacitance–voltage measurements are performed to investigate the influence of bias stress time on these charge traps. The hysteresis of the bidirectional C–V and the shift of flat band voltage ($V_{\rm fb}$) after different bias stress time are used to evaluate the densities of $N_{\rm niot}$ and $N_{\rm ot}$. Moreover, secondary ion mass spectroscopy (SIMS) is applied to investigate the components in the NO- and Ar-annealed samples, so as to indicate the region of the $N_{\rm niot}$ and the improvement of the traps for NO annealing.

2. Experimental methods

Silicon faced 4° off-axis n-type 4H–SiC wafer purchased from Epi World International Co., LTD., with an epitaxial layer thickness of 13.28 μm and nitrogen-doped concentration of 7.79×10^{15} cm^{-3}, was used in this experiment. Following the RCA cleaning, an HF dip, water rinsing, and thermal oxidation were carried out in a dry O_2 environment at a temperature of 1300 °C. Afterwards, the samples were annealed in Ar and NO ambiences, respectively. Post-oxidation-annealing (POA) for all of the samples was performed under the condition of 1175 °C for 2 h. The oxide thicknesses ($d_{\rm ox}$) determined by ellipsometry were 49 nm and 51 nm for the POA samples with Ar and NO ambiences, respectively. After SIMS measurements for the annealed samples, Ni was evaporated for the backside ohmic contact and Al was sputtered on the oxidized surface to form the gate electrode.

The samples in this study were bias-stressed and measured using an Agilent B1505A semiconductor parameter analyzer. The properties of SiO_2/4H–SiC interfaces on n-type MOS capacitors were examined by the measurements of bidirectional capacitance–voltage (C–V). Then, time-dependent positive bias stress measurements were applied on the samples, and the bidirectional C–V curves were again measured after different bias stress time, in which the measurements were implemented at room temperature and the samples were applied by bias stresses of about 3 MV/cm for different stress time in the range of 300–5000 s, followed by the bidirectional capacitance–voltage measurements with each sweeping time of 60 s. The setting parameter of C–V measurement has been adjusted to ensure the consistency in the entire measurement procedure. The schematic diagram indicating the TDBS measurements is shown in Fig. 1.

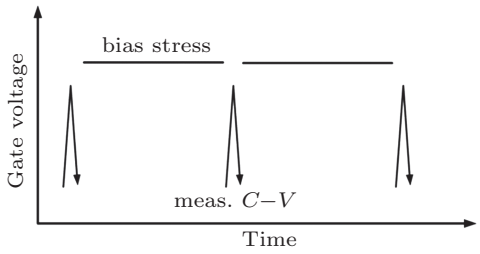


Fig. 1. Bias stress and measurement sequence for the TDBS measurements.

The densities of $N_{\rm niot}$ and $N_{\rm ot}$ were evaluated by the hysteresis of bidirectional C–V and the shift of flatband voltage after different bias stress time shown as[14]

$$N_{\rm niot} = \frac{\left|V_{\rm fb-up} - V_{\rm fb-down}\right| C_{\rm ox}}{qS}, \tag{1}$$

$$N_{\rm ot} = \frac{|\Delta V_{\rm fb}| C_{\rm ox}}{qS}, \tag{2}$$

where S is capacitance area, $C_{\rm ox}$ is the oxide capacitance, q is the electronic charge, $V_{\rm fb-up}$ is the flatband voltage of the clockwise C–V curve, $V_{\rm fb-down}$ is the flatband voltage of the counter-clockwise C–V curve, and $\Delta V_{\rm fb}$ is the shift of $V_{\rm fb-up}$ after different bias stress time compared with the first measured results. The flat-band voltage ($V_{\rm fb}$) was estimated from the ideal flatband capacitance ($C_{\rm fb}$).

3. Results and discussion

The first measured bidirectional capacitance–voltage results for the samples without TDBS are shown in Fig. 2, with sweeping the gate voltage in clockwise and counter-clockwise at the frequency of 10 kHz at 300 K, in which C–V data are normalized by the oxide capacitances ($C_{\rm ox}$) in the accumulation region.

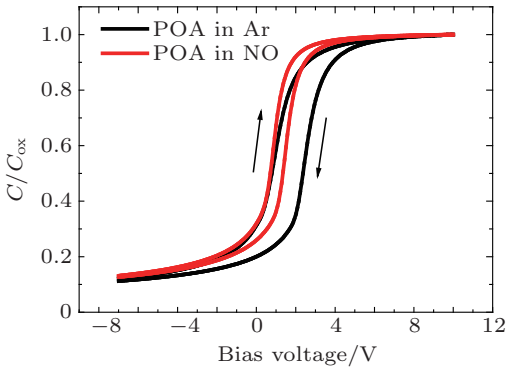


Fig. 2. Bidirectional capacitance–voltage characteristics of the samples annealed in Ar and NO ambiences at 10 kHz for the first measurement, in which the arrows indicate the voltage sweep directions.

In Fig. 2, the Ar-annealed sample shows a poor interface quality as identified from the stretch out shape of the *C*–*V* curves, possibly due to the carbon-related defects as discussed in the literature.[7] Besides, it is worth noting that the large hysteresis of bidirectional *C*–*V* is clearly observed in the curves, especially in the Ar-annealed samples. It is suggested that electrons, majority carriers of n-type SiC substrate, are injected into the charge traps during the clockwise *C*–*V* measurement.

The bidirectional *C*–*V* results measured at 10 kHz for the samples annealed with NO and Ar are shown in Figs. 3(a) and 3(b) when TDBS is applied. It is clear that the positive shift of $V_{\mathrm{fb-up}}$ shows an increasing trend each stress time. It is considered that more electrons are injected into the charge traps during the high bias stress, and most of the charge traps hardly release electrons back into the semiconductor quickly, still keeping their filling state during the subsequent measurements. The charge traps named oxide traps (N_{ot}) versus bias stress time calculated by Eq. (2) are shown in Fig. 3(c). Moreover, the hysteresis of bidirectional capacitance–voltage was also observed after TDBS, as shown in the inset of Figs. 3(a) and 3(b). The phenomena can be attributed to electrons emptying and filling some charge traps in response to the direct-current (DC) gate bias during the time scale of the bidirectional *C*–*V* measurements. Figure 3(d) shows N_{niot} versus bias stress time, which was calculated according to Eq. (1).

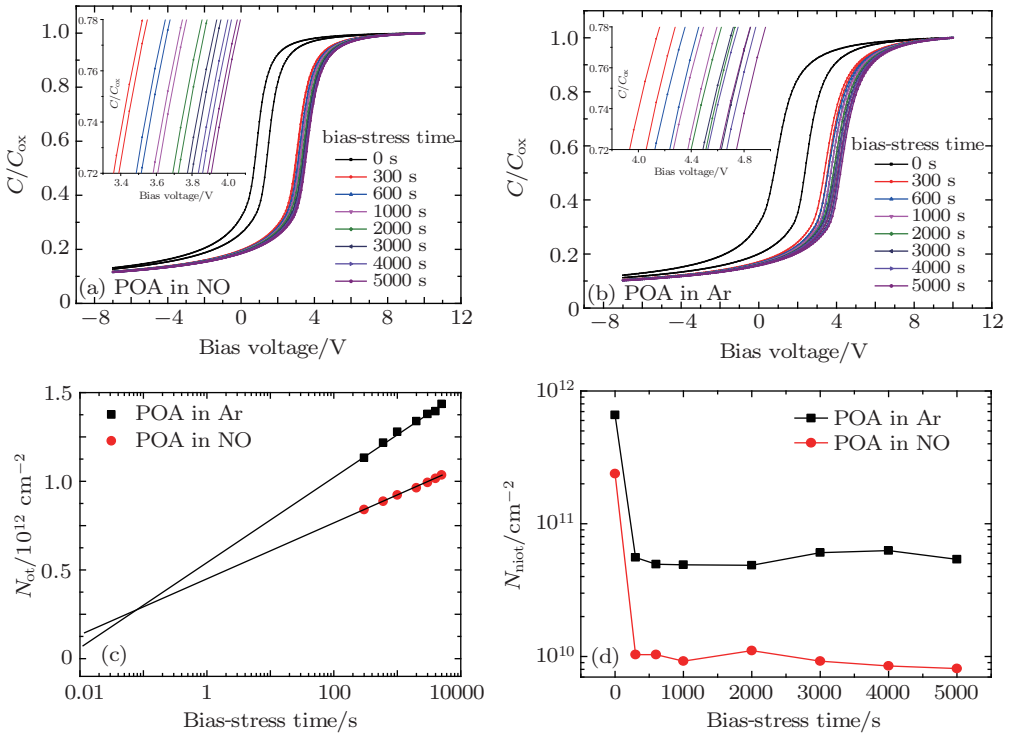


Fig. 3. Bidirectional *C*–*V* curves obtained from the samples with (a) NO and (b) Ar annealing after TDBS, and the densities of (c) N_{ot} and (d) N_{niot} versus bias-stress time.

From Fig. 3(c), it is clearly seen that the density of N_{ot} for the sample annealed in Ar is 1.3 to 1.5 times larger than the sample annealed in NO. Since the observed N_{ot} increases linearly in logarithmic coordinate of the bias stress time, it is suggested that electrons are tunneled into the oxide traps located in an extended distance from the semiconductor interface.[12–14] During bias stress, the N_{ot} captures the electrons incessantly, which are difficult to release. It is suggested that this kind of charge trap would seriously affect the threshold voltage stability of 4H–SiC MOSFET devices.

In Fig. 3(d), the values of N_{niot} extracted from the first measured bidirectional *C*–*V* curves, without suffering from TDBS (bias-stress time = 0), are larger than that suffering from TDBS, which can be explained through the four times repeated and uninterrupted bidirectional *C*–*V* measurement without suffering from TDBS, as shown in Fig. 4. The positive DC gate bias during the bidirectional *C*–*V* measurements can be regarded as a short time bias stress, which can make electrons inject into the charge traps. In Fig. 4(c), it is clear that the density of N_{niot} is decreased and the density of N_{ot} is increased with rising the measurement times. Thus, it is implied that in the first *C*–*V* measurement, electrons are injected into the charge traps, which include not only N_{niot} but also a part of N_{ot}. However, the remaining stable N_{niot} are very close to the semiconductor interface after the high bias stress, so that they can capture channel electrons to reduce the number of free carriers and the trapped charge centers also increase coulombic scattering to lower the actual channel mobility when the 4H–

SiC MOSFET devices are biased into strong inversion. As can be seen from Fig. 3(d) clearly, the density of stable $N_{\rm niot}$ for the annealed samples in Ar is 5 to 6 times larger than that of as-prepared samples. Taking the large reduction of $N_{\rm niot}$ into account, it may be reasonable to explain the observed interface state reduced by a factor of 4 to 5, which can induce a 10 to 15 fold increase in electron mobility.[17]

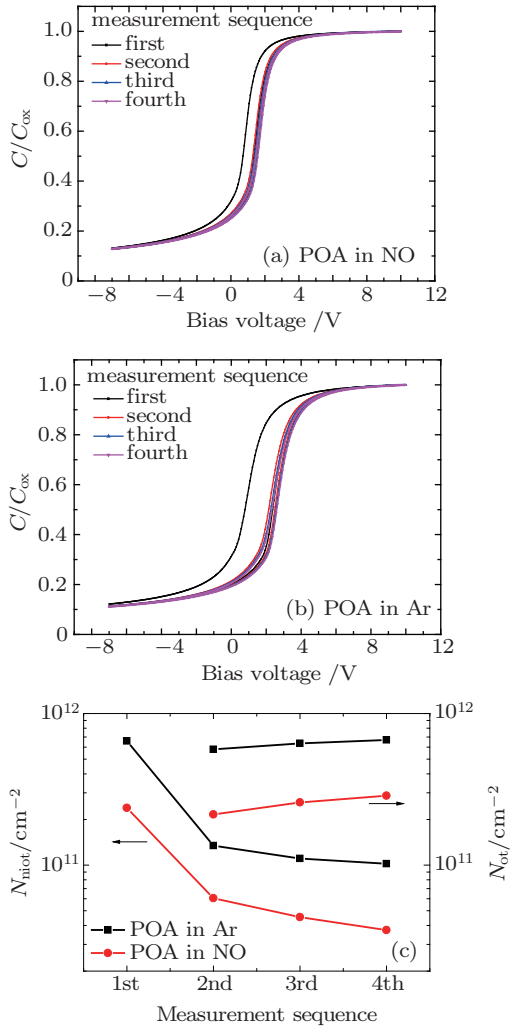


Fig. 4. Bidirectional *C–V* curves of the samples annealed in (a) NO and (b) Ar ambiences for the four times repeated and uninterrupted measurement without suffering from TDBS. (c) The densities of $N_{\rm niot}$ and $N_{\rm ot}$ versus measurement sequence.

Based on the distinction between $N_{\rm niot}$ and $N_{\rm ot}$ mentioned above, it is noticed that these charge traps are in different distances from the semiconductor interface, resulting in different response times. Moreover, the POA in NO gas produces a different improvement for $N_{\rm niot}$ and $N_{\rm ot}$, since the NO annealing shows a significant effect on $N_{\rm niot}$ but little improvement on $N_{\rm ot}$ compared with the Ar-annealed sample, which means that the mechanism to form charge traps is also different.

Next, in order to investigate the region of the $N_{\rm niot}$ and discuss the difference of $N_{\rm niot}$ and $N_{\rm ot}$ for these samples, SIMS was performed to investigate the components of the NO and Ar annealed samples, as shown in Fig. 5.

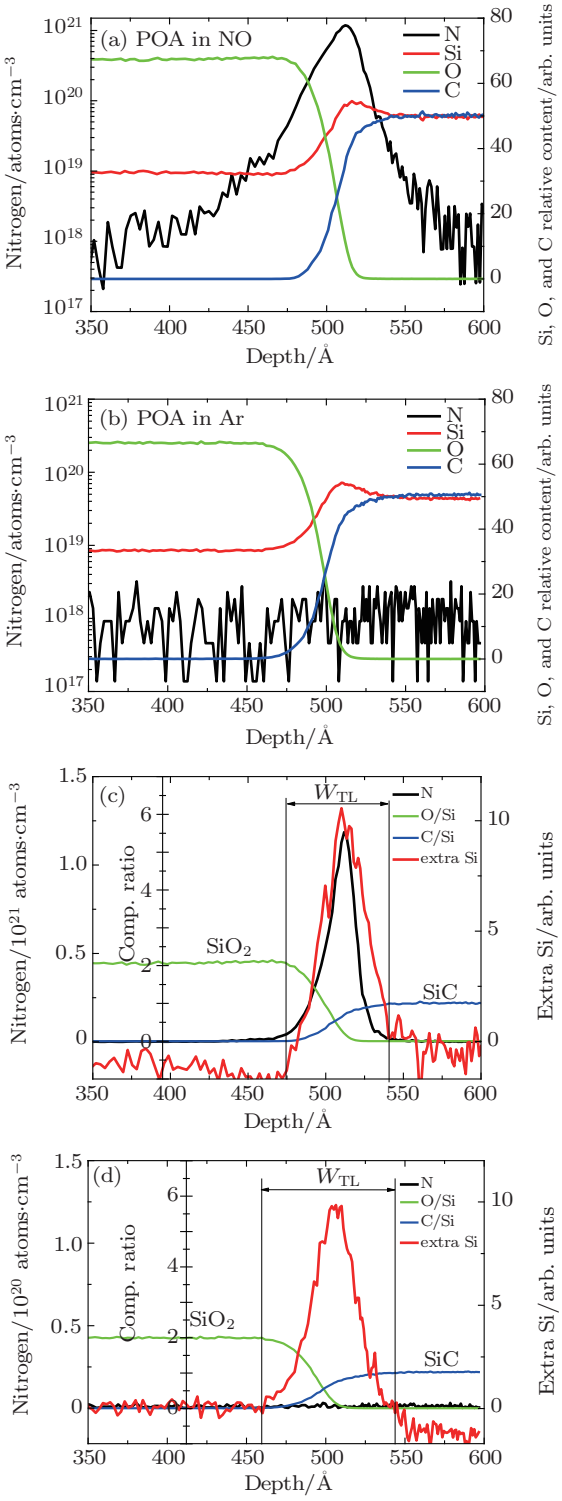


Fig. 5. SIMS profiles for the (a) NO and (b) Ar annealed samples. Transition layer width extracted from O/Si and C/Si composition ratio curves and the excess Si relative content with (c) NO and (d) Ar annealing versus oxide thickness.

It is clearly seen that POA in NO ambience makes a Gaussian-like profile of nitrogen near the interface, which coincides with that reported in Ref. [18]. However, no nitrogen is observed above the detection limit near the interface in the Ar-annealed sample. In both samples, it is found that the relative contents of Si, O, and C change slowly near the interface, indicating that there is a transition layer at the interface. The

transition layer width (W_{TL}) extracted from the SIMS profile is about 6.65 nm and 8.45 nm for the samples annealed with NO and Ar, respectively, which is defined as the region between the pure SiO_2 and SiC, as shown in Figs. 5(c) and 5(d). It is also worth noting that Si is accumulated near the interface and a small accumulation peak is formed. In Figs. 5(a) and 5(b), the silicon relative content in the accumulation peak is even more than that in the SiC epi-layer. Thus, the relative content of excess Si is obtained by the content of silicon minus the content of carbon and half of oxygen. Clearly, a Gaussian-like accumulation within the transition layer is caused by the excess Si as shown in both Figs. 5(c) and 5(d). It is inferred that some unreacted silicon atoms are accumulated in the transition layer, which stems from the excess Si atoms diffusion driven by the internal stress resulted from the lattice mismatch between SiO_2 and SiC at the interface. However, in the transitional region, the "SiO_x" is not stoichiometric SiO_2, and the excess Si atoms may exist in the form of the strained Si–Si bonds or Si interstitials,[19,20] which are associated with the N_{niot}. Thus, it can be seen that N_{niot} are distributed within the transition layer, which is very close to the semiconductor interface. As shown in Fig. 5(c), the Gaussian-like accumulation of N and excess Si atoms are aligned in the transition layer. Therefore, NO annealing causes some of the excess Si atoms to incorporate into the nitrogen to change the strained Si–Si bonds with a strong Si≡N bond, allowing better relaxation of the interface strain and reducing the width of transition layer and the density of N_{niot}. As the former work reported, the relatively thick gate oxide thickness leads to more serious threshold instability.[14] Thus, the N_{ot} is distributed in the entire SiO_2 insulator, which may be related to the carbon-related residua in the insulator.[21] It is thought that the NO annealing induces a slow re-oxidation process to consume the carbon related residua in the SiO_2 insulator and leads to the reduction of the density of N_{ot}.

4. Conclusion

In conclusion, the hysteresis of bidirectional C–V and the shift of flatband voltage after TDBS show N_{niot} and N_{ot}, existing in the oxide insulator and transition layer for 4H–SiC MOS devices. The N_{niot} are distributed within the transition layer between the pure SiO_2 and SiC, which correlated with the existence of the excess silicon. Thus, the N_{niot} are very close to the semiconductor interface and can readily exchange charge with the inner semiconductor, so that these traps may significantly affect the channel mobility of the SiC MOS device. However, the N_{ot} is distributed in the entire oxide insulator and may be related to the carbon related residua in the insulator. The charges trapped in the N_{ot} need a long time to be released, which will affect the stability of threshold voltage. Compared with the Ar-annealed sample, it is found that only N_{niot} can be significantly suppressed by the NO annealing, but little improvement of N_{ot}. The results from SIMS have demonstrated that the excess Si incorporates into nitrogen in the transition layer during the NO annealing process, allowing better relaxation of the interface strain and effectively reducing the width of the transition layer and the density of N_{niot}. As for the N_{ot}, the carbon-related residua can be consumed by the slow re-oxidation process in NO annealing. Two different charge traps existing in the oxide insulator and transition layer will cause different impacts on the performance of devices. Therefore, it is important to reduce all types of charge traps to enhance the performance and reliability of SiC MOSFETs.

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