Growth condition optimization and mobility enhancement through inserting AlAs monolayer in the InP-based $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ HEMT structures*

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The structure of InP-based $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ pseudomorphic high electron mobility transistor (PHEMT) was optimized in detail. Effects of growth temperature, growth interruption time, Si δ-doping condition, channel thickness and In content, and inserted AlAs monolayer (ML) on the two-dimensional electron gas (2DEG) performance were investigated carefully. It was found that the use of the inserted AlAs monolayer has an enhancement effect on the mobility due to the reduction of interface roughness and the suppression of Si movement. With optimization of the growth parameters, the structures composed of a 10 nm thick $In_{0.75}Ga_{0.25}As$ channel layer and a 3 nm thick $AlAs/In_{0.52}Al_{0.48}As$ superlattices spacer layer exhibited electron mobilities as high as 12500 $cm^2\cdot V^{-1}\cdot s^{-1}$ (300 K) and 53500 $cm^2\cdot V^{-1}\cdot s^{-1}$ (77 K) and the corresponding sheet carrier concentrations (N_s) of 2.8×10^{12} cm^{-2} and 2.9×10^{12} cm^{-2}, respectively. To the best of the authors' knowledge, this is the highest reported room temperature mobility for InP-based HEMTs with a spacer of 3 nm to date.

Keywords: high electron mobility transistor, two-dimensional electron gas, InP

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1. Introduction

InP-based $In_xGa_{1-x}As/In_yAl_{1-y}As$ pseudomorphic high electron mobility transistors (PHEMTs) exhibit outstanding performances in high-frequency and low-noise devices and have been widely studied over the last decade.[1–7] This is attributed to the great electrical properties of the InGaAs channel such as high saturation velocity and high electron mobility. Therefore, it is necessary to maximize both electron mobility (μ) and sheet carrier concentration (N_s) in the channel to get better HEMT device performance. Since the improvements of these two figures often contradict each other, and at the same time, various growth-related scattering effects, e.g., scattering by alloy disorder, interface roughness, and remote impurity, significantly influence the electrical properties of the two-dimensional electron gas (2DEG) structures,[8,9] the 2DEG properties are greatly dependent on the quality of the epitaxial heterostructures and the structure parameters such as the Si δ-doping density, the channel thickness and In content, and the spacer layer thickness and In content. Hence, growth optimization is needed to enhance the 2DEG properties and improve the device performance.

In this work, we systematically investigate the effect of the growth conditions and the structure parameters on the 2DEG properties of the $In_xGa_{1-x}As/In_yAl_{1-y}As$ PHEMT structures grown by gas-source molecular beam epitaxy (GSMBE), which are extremely enhanced by optimizing the growth temperature, the growth interruption time, the δ-doping condition, and the channel layer thickness and In content.

2. Experiment

The HEMT epitaxial structures were grown on single-side polished, Fe-doped InP (001) substrates by a V90 GSMBE system. The 7N-purity elemental indium (In), aluminum (Al), and gallium (Ga) were used as the group III sources, while the phosphorus and arsenic beams obtained by thermal cracking of phosphine (PH_3) and arsine (AsH_3) at 1000 °C provided the group V elements. The silicon (Si) effusion cell was used as the n-type doping source and the doping density was controlled by Si-cell temperature (T_{Si}) and doping time. Before the growth of the HEMT structures, the substrate was heated to 515 °C for 5 min under P_2 overpressure to desorb the surface oxide until a sharp (2×4) reconstruction was observed by *in situ* reflection high energy diffraction (RHEED). The basic HEMT structure is shown in Table 1. The configuration of the HEMT structures is as follows from bottom to top: a 500 nm thick $In_{0.52}Al_{0.48}As$ buffer layer over the InP substrate, a strained $In_xGa_{1-x}As$ channel with thickness t_w, a 3 nm thick $In_{0.52}Al_{0.48}As$ spacer layer, a Si-δ-doping layer, an 8 nm thick $In_{0.52}Al_{0.48}As$ Schottky barrier layer, a 4 nm InP etching stopper layer, a 15 nm $In_{0.52}Al_{0.48}As$ cap layer, a 15 nm $In_{0.53}Ga_{0.47}As$ cap layer, and finally, a 10 nm

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$In_{0.65}Ga_{0.35}As$ cap layer. The electron mobility and 2DEG density are measured by an Accent HL5500 Hall system at room temperature and 77 K, respectively, after keeping the samples in the dark for 2 min.

Table 1. Epi structure of InP-based $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ HEMT.

Layer	Thickness/nm	Doping/cm^{-3}
n^+-$In_{0.65}Ga_{0.35}As$ cap	10	3×10^{19}
n^+-$In_{0.53}Ga_{0.52}As$ cap	15	3×10^{19}
n^+-$In_{0.52}Al_{0.48}As$ cap	15	2×10^{19}
InP etching stopper	4	un
$In_{0.52}Al_{0.48}A$ barrier	8	un
Si δ-doped sheet	$2.\times10^{12}$–$7.\times10^{12}$ cm^{-2}	
$In_{0.52}Al_{0.48}As$ spacer	3	un
$In_xGa_{1-x}As$ channel	t_w	un
$In_{0.52}Al_{0.48}As$ buffer	500	un

3. Results and discussion

3.1. Substrate growth temperature

Generally, the quality of the epitaxial InGaAs/InAlAs heterostructures is strongly affected by the substrate growth temperature (T_{sub}). Because the lower growth temperatures for the InAlAs layer lead to an increased density of As-rich related defects[10] and the higher growth temperatures for the heavily strained InGaAs layers introduce misfit dislocations in the crystal.[11,12] Both of the As-rich related defects and the misfit dislocations introduce acceptor centers, which will trap electrons and degrade the mobility.[13,14] On the other hand, different growth temperatures for the InGaAs and InAlAs layers introduce longer growth interruption time, which leads to an excessive density of undesired background impurities right at the InAlAs/InGaAs interface and degrades the 2DEG properties. It is advantageous to find a common growth temperature for both InAlAs and InGaAs layers. In order to study the effect of the growth temperature on the 2DEG properties of the HEMTs, a series of samples were grown with δ-doping time of 7 s at Si-cell temperature (T_{Si}) of 1265 °C under As_2 overpressure. The channel thickness and In content were kept constant at 10 nm and 0.7, respectively. The HEMT structures were deposited at the substrate temperatures of 435 °C, 455 °C, 475 °C, and 495 °C. Figure 1 shows the electron mobility and 2DEG density versus the growth temperature of the HEMT structures at 300 K and 77 K. As shown in this figure, the highest value of the product of μ and N_s is obtained at the growth temperature of 475 °C. Higher or lower growth temperatures result in lower values of the product, which is unfavorable for the device performance. Thus, the substrate temperature of 475 °C is found to be the optimum growth temperature for further growth optimization in order to maximize the electron mobility in the above-described structures.

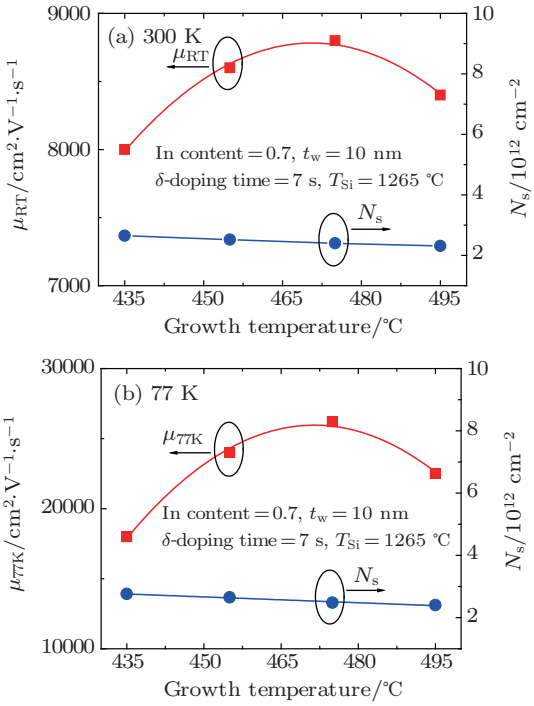


Fig. 1. (color online) Electron mobility (μ) and 2DEG density (N_s) versus growth temperature measured at (a) room-temperature and (b) 77 K.

3.2. Growth interruption time

A growth interruption under As_2 overpressure was used at the InGaAs/InAlAs interfaces. It would provide sufficient time for the migration of atoms on the growth surface to make the crystal interface smooth, which could reduce the interface roughness, remote impurity scattering, and alloy disorder scattering and increase the electron mobility.[15] But the different growth interruption time introduces a different density of undesired background impurities right at the InGaAs/InAlAs interfaces, which enhance the electron scattering and reduce the electron mobility. In order to study the effect of the growth interruption time on the 2DEG properties, a series of samples with different growth interruption times were grown at the substrate temperature of 475 °C. During the growth, all the other growth conditions and the structure parameters remained as discussed above. Figure 2 shows the electron mobility and 2DEG density as a function of the growth interruption time at 300 K and 77 K. It can be seen that the highest electron mobility is achieved with a growth interruption of 10 s. The Hall measurements indicate the room-temperature and 77 K mobilities as high as 10300 cm^2·V^{-1}·s^{-1} and 32200 cm^2·V^{-1}·s^{-1}, respectively, and the corresponding sheet carrier concentrations are 2.5×10^{12} cm^{-2} and 2.6×10^{12} cm^{-2}. Hence, 10 s is found to be the optimum growth interruption time for the InAlAs/InGaAs interface to achieve the highest electron mobility.

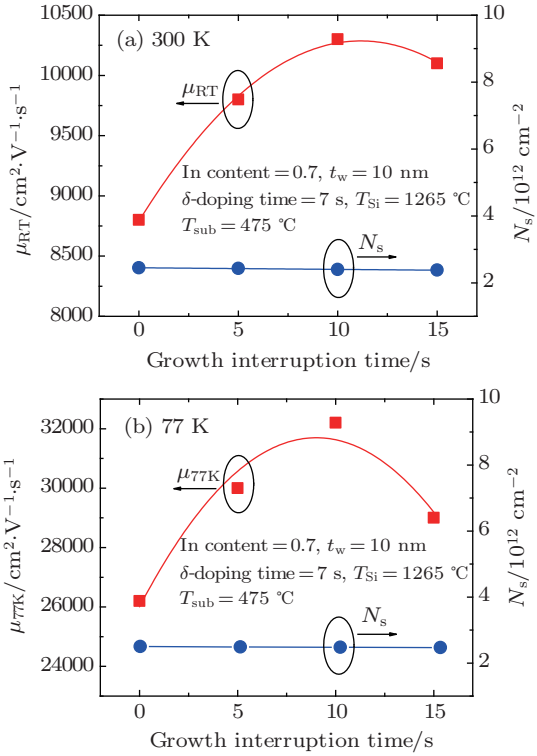


Fig. 2. (color online) Electron mobility (μ) and 2DEG density (N_s) versus growth interruption time measured at (a) room-temperature and (b) 77 K.

3.3. Channel In content and thickness

Normally, increasing the In fraction and the thickness of the InGaAs channel layer will enhance the electrical property of the 2DEG structure, but precaution must be taken not to exceed the critical thickness. This is due to the fact that a high In content will increase the effective band gap difference between the InGaAs channel layer and the InAlAs barrier layer, and will also weaken the alloy disorder scattering of 2DEG. But the critical thickness of the channel layer will be reduced. The scattering by interface, alloy disorder, and misfit dislocations will be enhanced once the thickness exceeds the critical one or is too short. In order to study the effect of the channel In content and thickness on the 2DEG properties, two series of HEMT structures were grown with δ-doping time of 7 s at a Si-cell temperature of 1265 °C under As_2 overpressure. The growth temperature was kept constant at 475 °C. In the first series, the channel thickness t_w is 10 nm and the channel In content is varied, while the channel In content is kept at 0.75 and the channel thickness t_w is varied in the second series. Figures 3(a) and 3(b) show the electron mobility and 2DEG density versus the channel In content at 300 K and 77 K, respectively. Figures 3(c) and 3(d) show the electron mobility and 2DEG density versus the channel thickness at 300 K and 77 K, respectively. The room-temperature Hall measurements indicate that the 2DEG density increases monotonously with the increase of the channel In content, while the 2DEG density almost keeps constant with the increase of the channel thickness. A maximum mobility of $\mu_{RT} = 10600\ \text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$ with a 2DEG density of $N_s = 2.7\times10^{12}\ \text{cm}^{-2}$ is obtained in the sample with the channel In content of 0.75 and the channel thickness of 10 nm, as shown in Figs. 3(a) and 3(c). The Hall measurements of this sample at 77 K display an electron mobility as high as $\mu_{77K} = 33500\ \text{cm}^2\cdot\text{V}^{-1}\cdot\text{s}^{-1}$ ($2.8\times10^{12}\ \text{cm}^{-2}$).

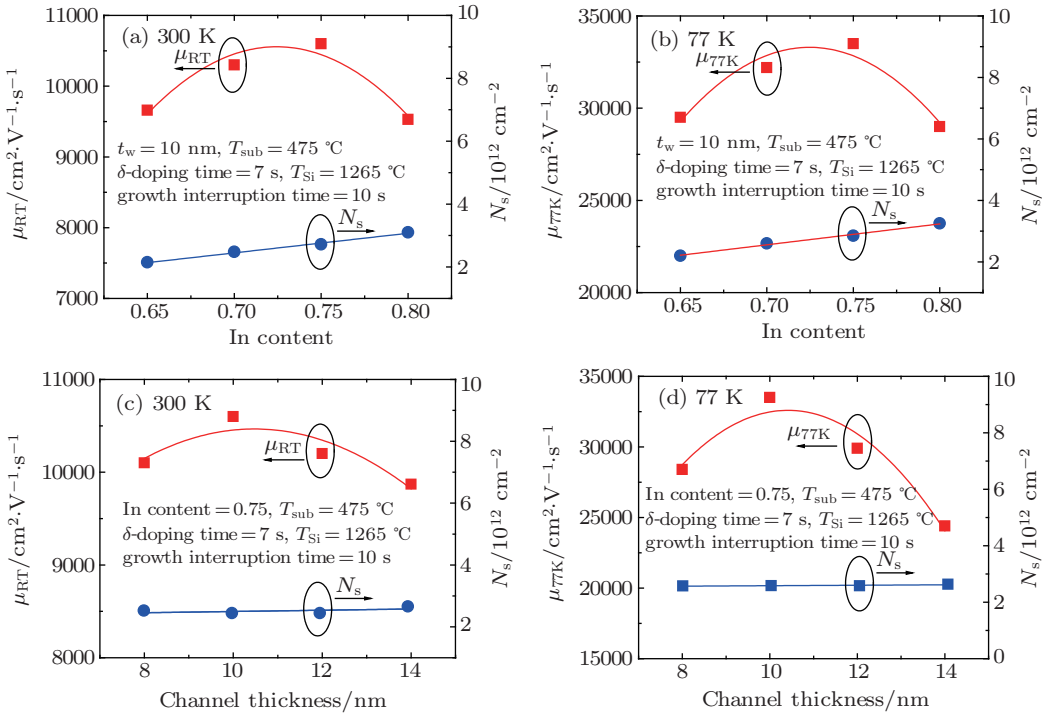


Fig. 3. (color online) Electron mobility (μ_{RT}) and 2DEG density (N_s) as a function of In content measured at (a) room-temperature and (b) 77 K. Electron mobility (μ_{RT}) and 2DEG density (N_s) as a function of channel thickness measured at (c) room-temperature and (d) 77 K.

3.4. Si δ-doping condition

In order to study the effect of the Si δ-doping condition on the 2DEG properties, a series of HEMT structures were grown with different δ-doping times ranging from 3 s to 12 s at a Si-cell temperature of 1265 °C under As_2 overpressure. During the growth, all the other growth conditions and the structure parameters remained as discussed above. Figures 4(a) and 4(b) show the electron mobility and 2DEG density as a function of the δ-doping time at 300 K and 77 K, respectively. Both room-temperature and 77 K Hall measurements demonstrate a quasi-linear dependence of the 2DEG concentration versus the δ-doping time. The mobility at room-temperature decreases gradually before 9 s, and dramatically after 9 s, whereas the mobility at 77 K reveals a maximum of $\mu_{77K} = 33900\ cm^2 \cdot V^{-1} \cdot s^{-1}$ with a sheet carrier concentration of $N_s = 2.3 \times 10^{12}\ cm^{-2}$ in the sample with the δ-doping time of 6 s.

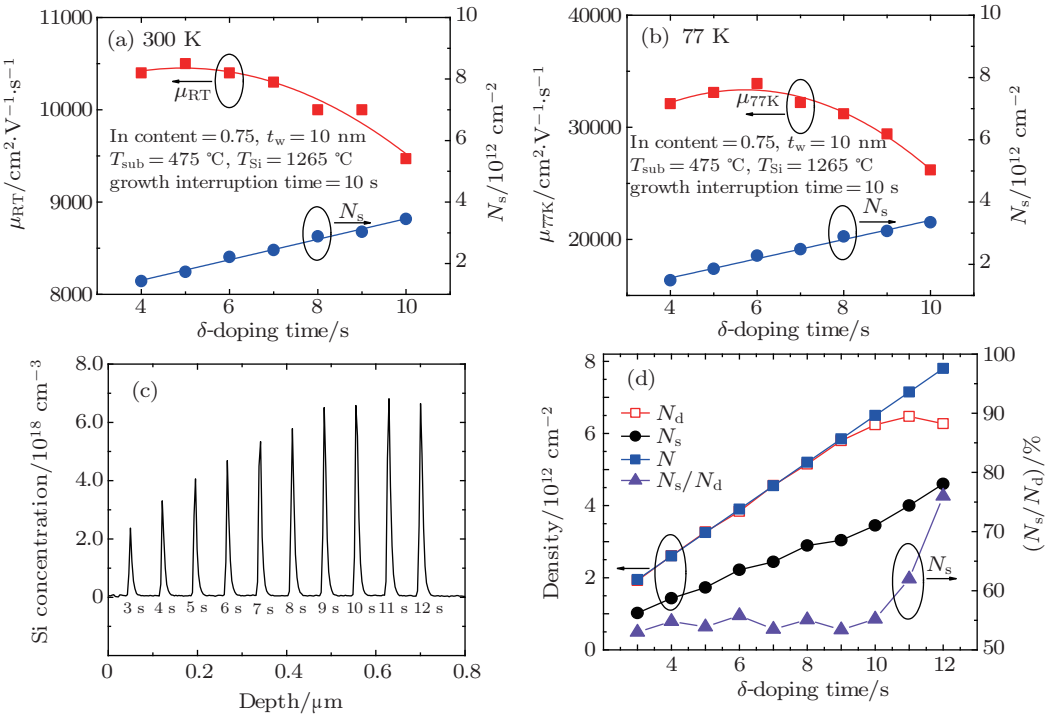


Fig. 4. (color online) Electron mobility (μ) and 2DEG density (N_s) as a function of δ-doping time measured at (a) room-temperature and (b) 77 K. (c) Si concentration distribution of different δ-doping times in the InAlAs bulk material measured by SIMS. (d) Dependences of Si total flux (N), donor density (N_d), 2DEG density (N_s), and doping efficiency (N_s/N_d) on δ-doping time.

In order to analyze the degradation of the electron mobility with the δ-doping time , a δ-doping structrure with different Si δ-doping times ranging from 3 s to 12 s in the InAlAs bulk material was grown at 475 °C under As_2 overpressure and the donor concentrations were calibrated by SIMS, as shown in Fig. 4(c). Figure 4(d) shows the dependences of Si total flux (N), donor concentration (N_d), 2DEG density (N_s), and doping efficiency (N_s/N_d) on the δ-doping time. Below 9 s, it shows a quasi-linear dependence of the donor density (N_d) versus the Si δ-doping time and the donor density is almost equal to the Si total flux injected into the growth surface. The Si atoms cover the growth surface and gradually spread into the monolayer of the spacer layer with increasing δ-doping time, which mainly enhances the remote impurity scattering.[16] Thus, the electron mobility gradually degrades due to the increasing scattering by remote impurity, as shown in Fig. 4(a). Above 9 s, the donor density slowly increases and reaches a saturation at about $6.0 \times 10^{12}\ cm^{-2}$. The results indicate that the δ-doped layer has the aggregation of silicon, which results in the degeneration of the crystal interface.[17,18] The mobility dramatically degrades mainly due to the increasing remote scattering and interface scattering, as shown in Fig. 4(a). Thus, the δ-doping time of 9 s at a Si-cell temperature of 1265 °C under As_2 overpressure is found to be the optimum δ-doping condition and the corresponding δ-doping density is about $6 \times 10^{12}\ cm^{-2}$. A rather high overall doping efficiency N_s/N_d of 0.55 estimated from the results in Fig. 4(d) can be attributed to the relatively thin spacer layer, which benefits the electron of the δ-doping layer tunneling into the channel layer.

3.5. Inserted AlAs monolayer

In order to study the effect of the inserted AlAs monolayer on the 2DEG properties of the HEMTs, a set of samples A, B, C, and D were grown. Figure 5 shows the structure differences of the samples. Sample A without the inserted AlAs

monolayer is used as a reference. All the other growth parameters as well as the layer thicknesses remained as discussed above. As shown in Table 2, the electron mobilities of samples B and C increase by 14% and 9% compared to that of sample A at room temperature, respectively, which indicate that the inserted AlAs monolayer at the InGaAs/InAlAs interface and the spacer layer enhance the mobility. Because Al has the lowest surface mobility compared to other atom species involved in the growth, the AlAs monolayer is able to prevent interdiffusion effects at the InGaAs/InAlAs interfaces and consequently to reduce the interface roughness and alloy disorder. On the other hand, the Si diffusion into the channel layer can be suppressed by the AlAs monolayer, which reduces the remote impurity scattering. Figure 6 shows the numerical simulation close to the channel region of the band diagram, the donor concentration, and the 2DEG density for the HEMT structure of sample D with the inserted AlAs monolayer at the InAlAs/InGaAs interface and the InAlAs spacer layer. The AlAs monolayer is simultaneously inserted at the interface and the spacer layer in sample D, the electron mobility is increased to 12500 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature with a 2DEG density of 2.8×10^{12} cm^{-2} To the best of the authors' knowledge, this is the highest reported room temperature mobility for InP-based HEMTs with a spacer of 3 nm to date. At 77 K, the 2DEG density is $N_s = 2.9 \times 10^{12}$ cm^{-2} and the mobility reaches 535000 $cm^2 \cdot V^{-1} \cdot s^{-1}$, which is 82% higher compared to that of sample A without the inserted AlAs monolayer. The results indicate that the use of the inserted AlAs monolayer has an enhancement effect on the mobility due to the reduction of interface roughness and the suppression of Si movement.

Table 2. Hall data of the InGaAs/InAlAs HEMT structures.

Sample	Channel	$N_d/10^{12}$ cm^{-2}	300 K		77 K	
			$N_s/10^{12}$ cm^{-2}	$\mu/10^4$ $cm^2 \cdot V^{-1} \cdot s^{-1}$	$N_s/10^{12}$ cm^{-2}	$\mu/10^4$ $cm^2 \cdot V^{-1} \cdot s^{-1}$
A	$In_{0.75}Ga_{0.25}As$	6.0	3.036	1	3.180	2.94
B	$In_{0.75}Ga_{0.25}As$	6.0	2.919	1.14	3.079	4.05
C	$In_{0.75}Ga_{0.25}As$	6.0	2.964	1.09	3.127	3.92
D	$In_{0.75}Ga_{0.25}As$	6.0	2.825	1.25	2.932	5.35

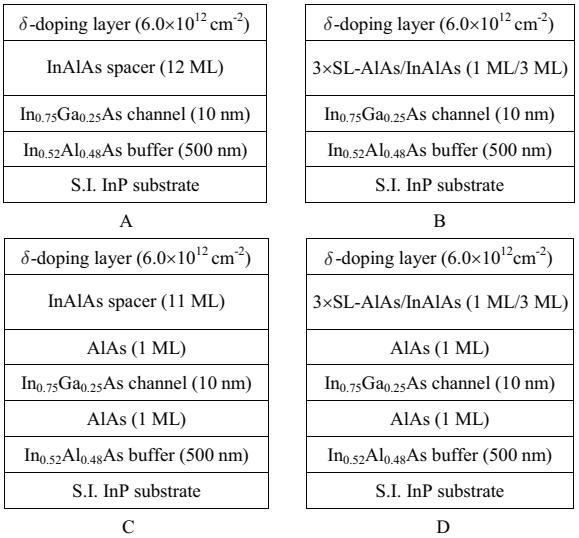


Fig. 5. Sketch of the structure differences of samples A, B, C, and D.

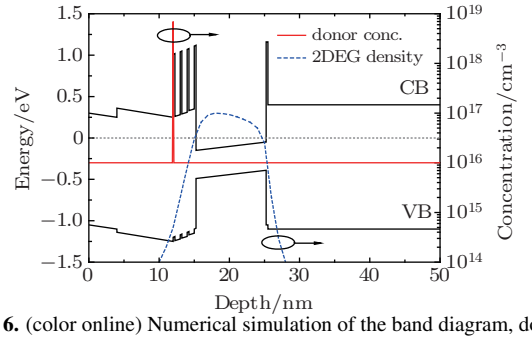


Fig. 6. (color online) Numerical simulation of the band diagram, donor concentration, and 2DEG density in the region around the 2DEG for the HEMT structure of sample D with the inserted AlAs monolayer at the InAlAs/InGaAs interface and the InAlAs spacer layer.

4. Conclusion

We have carefully investigated the effects of the growth temperature, growth interruption time, Si δ-doping condition, channel thickness and In content, and inserted AlAs monolayer (ML) on the electrical properties of the InP-based $In_xGa_{1-x}As/In_{0.52}Al_{0.48}As$ HEMT structures. The results indicate that the growth interruption under As_2 overpressure reduces the interface roughness and improves the crystal interface. It is found that the use of the inserted AlAs monolayer has an enhancement effect on the mobility due to the reduction of interface roughness and the suppression of Si movement. With optimization of the growth parameters, the structures composed of a 10 nm thick $In_{0.75}Ga_{0.25}As$ channel layer and a 3 nm thick $AlAs/In_{0.52}Al_{0.48}As$ superlattices spacer layer have the electron mobilities as high as 12500 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (300 K) and 53500 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (77 K) and the corresponding sheet carrier concentrations (N_s) of 2.8×10^{12} cm^{-2} and 2.9×10^{12} cm^{-2}, respectively.

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