Pattern dependence in synergistic effects of total dose on single-event upset hardness*

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The pattern dependence in synergistic effects was studied in a 0.18 μm static random access memory (SRAM) circuit. Experiments were performed under two SEU test environments: 3 MeV protons and heavy ions. Measured results show different trends. In heavy ion SEU test, the degradation in the peripheral circuitry also existed because the measured SEU cross section decreased regardless of the patterns written to the SRAM array. TCAD simulation was performed. TID-induced degradation in nMOSFETs mainly induced the imprint effect in the SRAM cell, which is consistent with the measured results under the proton environment, but cannot explain the phenomena observed under heavy ion environment. A possible explanation could be the contribution from the radiation-induced GIDL in pMOSFETs.

Keywords: pattern dependence, total dose, single event upset (SEU), static random access memory (SRAM)

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1. Introduction

The synergistic effects of total dose on single-event-upset- (SEU) sensitivity in memories have been studied since the early 90s.[1] It has been shown that the SEU hardness can deteriorate as devices have been exposed to total dose ionizing (TID) source first.[2,3] For technologies with relatively thick gate oxide, total dose irradiation induces different levels of threshold voltage shifts in the transistors within the memory cell, due to different bias conditions correspondingly. Thus, the imbalance in threshold voltages can significantly increase or decrease the SEU cross section.[1,2] For state-of-the-art technologies with thin gate oxide, although the TID effects in gate oxide get weaker, the radiation-induced charge trapping in shallow trench isolation (STI) may still represent a potential reliability threat.[4] Evident synergistic effects have been reported in lower than 0.25 μm technologies.[3,5–7]

From the former results, one thing worth noticing is that the memory patterns written to the cells during TID irradiation and during SEU cross section measurement strongly affect the evaluation of the synergistic effects. Some results indicate that opposite patterns during TID irradiation and in SEU tests can deteriorate the SEU hardness of the memories (imprint effect).[3,5,8] However, some results suggest that the same patterns correspond to the worst-case test conditions.[3,5,9] Moreover, some other results showed that no evident synergistic effects can be observed.[3,5]

To explain these phenomena, efforts have been devoted to exploring the underlying mechanisms, mainly for older technologies with thick gate oxide. From analytical quantification, the imprint effect is reasonable and consistent with the threshold voltage shifts during TID irradiation.[8] From the microbeam SEU test results, after high dose irradiation with pattern No. 1 and the opposite pattern No. 2, the area of the SEU error regions located in the N-type transistors keeps decreasing and that for the P-type transistors keeps increasing, indicating the competition resulting from the TID effects in the two inverters within the cell.[10] For modern technologies, a light emission microscopy photograph suggests the radiation-induced degradation in peripheral circuitry, which lowered the output voltage of internal circuitry used to control the bias levels to the internal memory circuits,[3] In a word, due to the subtle differences in the specific circuits, the measured synergistic effects can be very different.

In this work, we focus on studying the pattern dependence in synergistic effects in one 0.18 μm static random access memory (SRAM), based on both SEU test results under proton and heavy ion environments and TCAD simulation. We aim to present the interesting measurement results and explore the corresponding mechanisms by device simulation.

2. Experimental details

2.1. Test structures

The SRAM circuit used in this study was fabricated in a 0.18 μm bulk CMOS technology, with the vendor of Renesas, the capacity of 8 Mbit and the bias voltage of 3.3 V. The SRAM cell is made of 6-T design and the corresponding physical size is 3.01×1.28 μm^2 (3.85 μm^2). From the earlier study reported in Ref. [11], the SRAM circuit is immune to single event latchup (SEL) even irradiated with the heavy ion Au with

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a linear energy transfer (LET) value of 77.6 MeV·cm^2/mg.

2.2. Irradiation setup

The irradiation experiments contain two parts: the first one was performed with 3 MeV protons; the second one was performed with γ ray photons and heavy ions. A test system developed by the Northwest Institute of Nuclear Technology was used to monitor the logical states of the memory cells.[11] The devices were de-lidded before the experiments.

In the first part, 3 MeV proton irradiation was performed in the Heavy Ion Accelerator Laboratory of Peking University. The values of LET, NIEL, and range in Si are 0.084 MeV·cm^2/mg, 2.25×10^{-5} MeV·cm^2/mg and 84.3 μm, respectively[12]. A high flux of 10^9 cm^{-2}·s^{-1} was chosen for the TID irradiation (a dose rate of 1.2 krad(Si)/s), where the devices were irradiated with a checkerboard pattern (CB) written to the memory array. Then a low flux of 10^5 cm^{-2}·s^{-1} was chosen for SEU measurement, where the devices were tested with four different patterns, CB, CBn (the pattern with every bit opposite to that in a CB pattern), all 1's and all 0's, in the vacuum. Upsets can be observed when the SRAM circuits were irradiated to 3 MeV protons. Till the end of irradiation, the deposited dose was 214 krad(Si) and the 1 MeV neutron equivalent fluence was 1.1×10^{11} n/cm^2. Since the properties of most MOS devices are not significantly affected by minority carrier lifetime, the SRAM circuit is relatively insensitive to the resulting displacement damage (DD),[13] especially for a low neutron equivalent fluence, like in this study.

In the second part, TID irradiation was performed with the Co-60 γ ray in the Northwest Institute of Nuclear Technology. Devices were irradiated with the CB pattern at a dose rate of 50 rad(Si)/s, under room-temperature environment. Since the time interval between the γ ray irradiation and the SEU test is not negligible but around 24 hours, the annealing problem has to be considered. To slow down the process, we implemented two approaches referring to the American military standard MIL-STD 883 TM1019: connecting all terminals of the chips together and storing the chips inside a container full of the carbon dioxide ice (with a temperature of around −80 °C). Thus, the annealing procedure was suppressed to a large extent. The SEU measurement was performed with the heavy ion ^{129}Xe produced in the Heavy Ion Research Facility in Lanzhou (HIRFL), with the LET value of 64.5 MeV·cm^2/mg, the energy of 914 MeV, and the range in Si of 67.7 μm. In this period, devices were irradiated with four patterns (CB, CBn, all 1's and all 0's) in the vacuum.

3. Results and discussion

3.1. Irradiation results

Figure 1 shows the measured SEU cross section when irradiated with the 3 MeV protons, as a function of the calculated total dose. First, due to the low energy of protons, the cross section value is very small (2 μm^2/8×10^6 comparing to the cell size of 3.85 μm^2). Secondly, evident synergistic effects can be observed, and the SEU sensitivity of the SRAM circuit is found to be related to the deposited dose. Thirdly, there is an evident dependence of the synergistic effects on the patterns written to the SRAM array during the test.

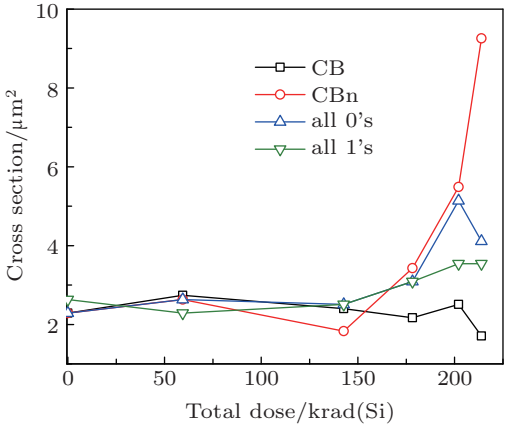


Fig. 1. (color online) Measured SEU cross section when irradiated with protons, as a function of the calculated total dose.

Figure 2 shows the measured SEU cross section when irradiated with heavy ions, as a function of the deposited dose irradiated with Co-60 γ ray. The cross section value is less than but close to the cell size 3.85 μm^2, suggesting that the cross section at 64.5 MeV·cm^2/mg has reached the saturation value. Here we can also observe the pattern dependency in the synergistic effects.

Comparing the results in Fig. 1 with those in Fig. 2, there are some inconsistencies worth noticing. From Fig. 1, when the SRAM circuit was irradiated with CB pattern during TID and CB pattern during SEU test (CB/CB in the following paper), the measured cross section remained almost the same. For CB/all 0's and CB/all 1's patterns, the SEU sensitivity increased at high deposited dose. For CB/CBn pattern, when the SRAM circuit was irradiated with the opposite patterns during TID irradiation and during SEU test, the SEU sensitivity increased evidently at high deposited dose. The phenomena were consistent with the imprint effect.[8] However, from Fig. 2, the SEU sensitivity of the SRAM circuit decreased at high dose for all the patterns. The CB/CBn pattern corresponds to the smallest SEU cross section, whereas the highest cross section was reached at CB/CB pattern. Thus, it is possible to attribute the phenomena partly to the performance degradation of the peripheral circuits (cross section decrease for all the patterns), and partly due to the SRAM cells (dependence of the cross section on patterns). Here the dependence of the SEU sensitivity on patterns was inconsistent with the imprint effect. The underlying mechanisms will be explored by means of TCAD simulation in the next section. Besides, there seems to be an inconsistency in the deposited dose where the

synergistic effects became visible, further suggesting the existence of more than one mechanism contributing to the phenomena.

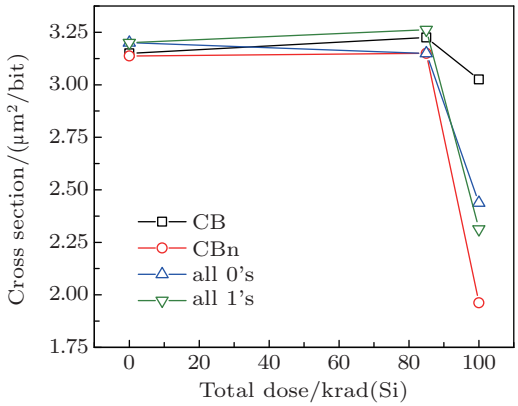


Fig. 2. (color online) Measured SEU cross section when irradiated with heavy ions, as a function of the total dose.

3.2. TCAD simulation

To understand the mechanisms of synergistic effects in the 0.18 μm technology and explain the phenomena observed, TCAD simulation was performed using the DESSIS 10.0 from ISE,[14] which has been widely used in studying TID-induced charge trapping and SEU behaviors.[15]

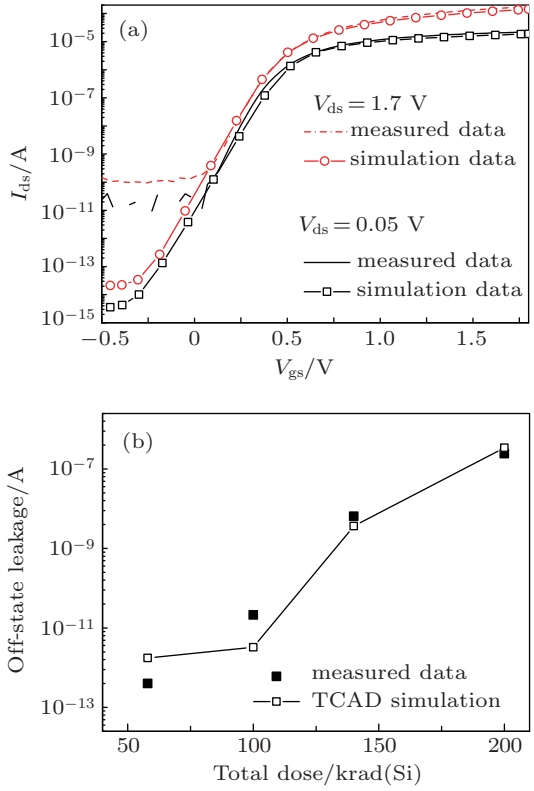


Fig. 3. (color online) (a) Calibration of TCAD simulatedI_{ds}–V_{gs} curves of $W/L = 0.22/0.18$ μm fresh nMOSFET with the measured curves; (b) calibration of the simulated off-state leakage after irradiation with the measured data.

Concerning the simulation parameters, the geometrical and doping parameters were extracted by fitting with the measurement results of MOS transistors fabricated by the manufacturer. The I_{ds}–V_{gs} curves were measured with a HP4156A both before and after TID irradiation by Co-60 γ ray. For deep-submicron MOS transistors irradiated to hundreds of kilorads, TID-induced degradation in pMOSFETs was very limited, and the TID-induced degradation in nMOSFETs was mainly due to the charge trapping in STI. Figure 3 shows the calibration results of measured and simulated I_{ds}–V_{gs} curves before irradiation (Fig. 3(a)) and off-state leakage after irradiation (Fig. 3(b)) for the 0.22/0.18 μm nMOSFET. Then we also got the values of other parameters considered in the simulations: the uniform trap density in the oxide $N_T = 3\times10^{17}$ cm^{-3}, the hole capture cross section $\sigma_{pt} = 5 \times 10^{-12}$ cm^2, and the cross section of electron recombination on trapped holes $\sigma_{pr} = 1 \times 10^{-14}$ cm^2.

Then we performed the mixed-mode simulation in the SRAM cell to study the synergistic effects, and the schematic of the simulation is shown in Fig. 4. The four transistors P_1 and P_2 (0.35/0.18 μm), N_1 and N_2 (0.22/0.18 μm) were described by 3-D device models. The other two transistors (A_1 and A_2) were described by SPICE models.

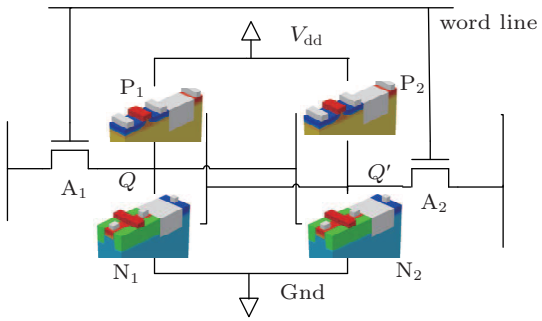


Fig. 4. (color online) Schematic of performing mixed-mode simulation in the SRAM cell.

In case of $Q = 0$ during TID irradiation, we focus on both $Q = 0$ and $Q = 1$ setups in SEU test to evaluate the evolution of the SEU sensitivity at CB/CB and CB/CBn patterns correspondingly. At $Q = 0$, the SEU sensitive regions include the drain regions of N_1 and P_2. Figure 5 shows the evolution of Q and Q' voltages when N_1 or P_2 were irradiated in SEU test. From Fig. 5(a), at LET = 1.11 MeV·cm^2/mg, the logical state stored in the node Q turned to the opposite value '1' when the heavy ion struck the drain region of N_1 before TID irradiation (the diamond symbols). After the total dose of 60 krad(Si), strike at N_1 drain would cause upset after a very long time (the circle symbols). Then after 140 krad(Si) total dose, strike at the same point did not induce upset (the triangle symbols). The simulated results suggest that the SEU sensitivity of N_1 region decreases with the total dose. Similarly, when P_2 drain was struck at LET = 2.15 MeV·cm^2/mg heavy ion (Fig. 5(b)), the SEU sensitivity also decreased with the total dose (upsets occurred at 0 and 60 krad(Si) dose, but did not

occur at 140 krad(Si)). To sum up, when the SRAM cell was irradiated with the same logical states during TID irradiation and in SEU test, the SEU sensitivity decreased.

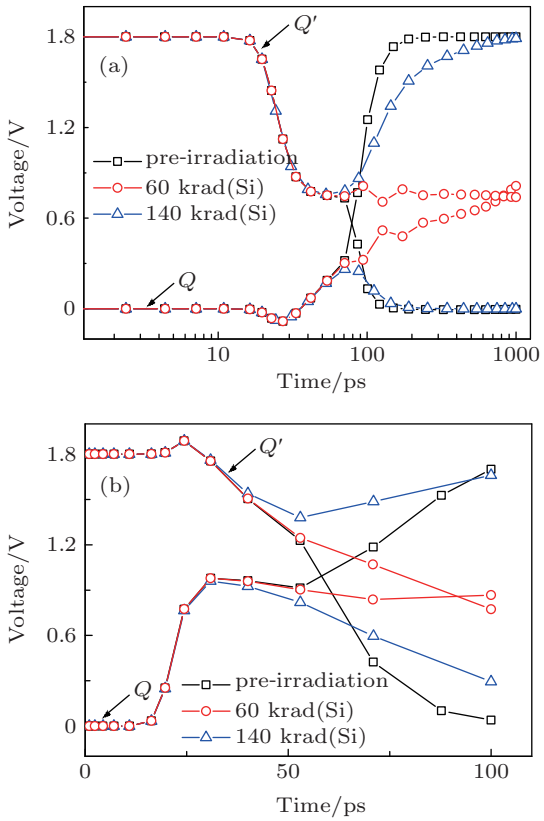


Fig. 5. (color online) Evolution of Q and Q' voltages when N_1 (a) or P_2 (b) were struck in SEU test. The pattern combination during irradiation was $Q = 0/Q = 0$.

Then we discuss the simulation results with $Q = 1$ in SEU test. From Fig. 6(a), when N_2 drain was struck by LET = 1.2 MeV·cm^2/mg heavy ion, the SEU sensitivity increased with the total dose (upsets did not occur at lower than 60 krad(Si) doses, but occurred at 140 krad(Si)). Then from Fig. 6(b), when P_1 drain was struck by LET = 2.1 MeV·cm^2/mg heavy ion, the SEU sensitivity increased with the total dose (upsets did not occur at lower than 140 krad(Si) doses, but occurred at 200 krad(Si)). Therefore, when the SRAM cell was irradiated with opposite logical states during TID irradiation and in SEU test, the SEU sensitivity increased.

The simulation results are consistent with the measured results under proton irradiation (Fig. 1), where the CB/CBn pattern during TID irradiation and in SEU test introduces a negative impact in the SEU sensitivity of the SRAM circuit.

In the TCAD simulation, we only take into account the TID effects in nMOSFETs due to the common theory of TID. Till now, the simulation results are not able to completely explain the measured phenomena. There must be other mechanisms contributing together.

From reference, there are some reported results that focus on the radiation-induced gate-induced-drain-leakage (GIDL) in pMOSFETs,[16] where the accumulated trapped charge and interface traps can possibly activate the electron tunneling between drain and nwell. Suppose there are also these phenomena in this study, at $Q = 0$ during TID irradiation, P_1 will degrade and there will be an increase in the off-state leakage. Under this circumstance, contrast to the TID degradation in N_1, $Q = 0$ in SEU test will increase the SEU sensitivity of the cell, whereas $Q = 1$ setup will decrease the SEU sensitivity.

Comparing the irradiation setups regarding the results in Figs. 1 and 2, it can be seen that the LET of the 3 MeV protons is close to the threshold LET due to the very small SEU cross section, whereas the cross section reached its saturation in the heavy ion test in Fig. 2. When the LET is close to the threshold value, the SEU-sensitive region is mainly part of the nMOSFET drain region which is connected to V_{dd}. Along with the increase in LET, the sensitive region will extend to the part of the pMOSFET drain region which is connected to the ground. Therefore, it is reasonable to suppose the existence of the two competitive mechanisms: TID-induced off-state leakage increase in nMOSFET and radiation-induced GIDL in pMOSFET. It is true that the contribution from GIDL is only an assumption in this study, and more works should be done in the future focusing on the behaviors of pMOSFETs, hopefully in the radiation-hardened devices where nMOSFETs are robust.

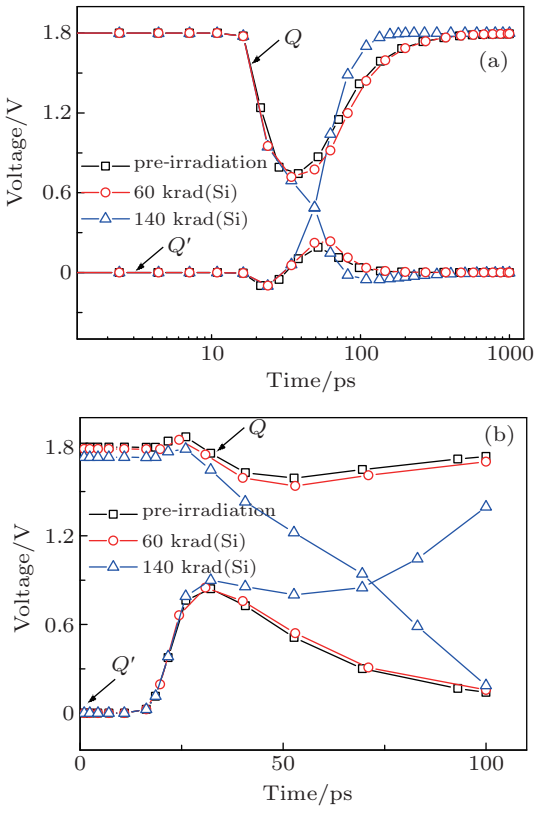


Fig. 6. (color online) Evolution of Q and Q' voltages when N_2 (a) or P_1 (b) were struck in SEU test. The pattern combination during irradiation was $Q = 0/Q = 1$.

4. Conclusion

Pattern dependence in synergistic effects was studied in a 0.18 μm SRAM circuit. The measured results under proton environment were consistent with the imprint effect, the CB/CBn pattern during TID irradiation and in SEU test corresponded to the highest SEU cross section. However, the results under heavy ion SEU test were quite different, where the cross section reached its saturation, and the CB/CBn pattern combination corresponded to the lowest SEU cross section. The degradation in the peripheral circuitry also existed because the measured SEU cross section decreased regardless of the patterns written to the SRAM array.

TCAD simulation was performed to explore the underlying mechanisms. When only considering the TID-induced degradation in nMOSFETs, the simulated results were consistent with the measured results under proton environment but cannot explain the phenomena observed under heavy ion environment. Supposing that there was a contribution from the radiation-induced GIDL in pMOSFETs, the measured results can be explained consistently. Regarding this, more works should be done in the future focusing on the behaviors of pMOSFETs, hopefully in the radiation-hardened devices where nMOSFETs are robust.

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