Analysis of the damage threshold of the GaAs pseudomorphic high electron mobility transistor induced by the electromagnetic pulse*

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An electromagnetic pulse (EMP)-induced damage model based on the internal damage mechanism of the GaAs pseudomorphic high electron mobility transistor (PHEMT) is established in this paper. With this model, the relationships among the damage power, damage energy, pulse width and signal amplitude are investigated. Simulation results show that the pulse width index from the damage power formula obtained here is higher than that from the empirical formula due to the hotspot transferring in the damage process of the device. It is observed that the damage energy is not a constant, which decreases with the signal amplitude increasing, and then changes little when the signal amplitude reaches up to a certain level.

Keywords: PHEMT, electromagnetic pulse, damage threshold, empirical formula

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1. Introduction

With the increasingly complicated electromagnetic environment, the electromagnetic pulse (EMP) threat to semiconductor devices has received growing attention in recent years.[1,2] It is important to make a reasonable estimate of whether or not the device will be damaged by EMP events. Such a prediction requires a knowledge of the damage threshold. There has been extensive work done in this aspect. Wunsch and Bell investigated the pulse power damage level of a semiconductor junction, and developed a semi-empirical formula based on the thermal failure model and extensive experimental data.[3] Tasca divided the damage level into three domains by the pulse width, i.e., the short pulse under the assumption of adiabatic condition, the longer pulse with considering heat loss which is similar to the Wunsch–Bell model,[3] and the steady state phase with thermal equilibrium established.[4] All these researches assumed the device to be a fixed heat source to study the EMP-induced damage threshold, and did not consider the internal physical mechanism of the device. So, uncertainties and errors associated with these models existed in EMP assessment and hardening design.[5] With the size of the device getting smaller, these uncertainties and errors become more and more serious. It is desired to find the relationship between the damage threshold and damage mechanism of the device. However, very few data have been presented in the literature in this aspect to date.[6]

The present study on the damage threshold of devices is completely different from that from the conventional method based on a simple thermal model. It establishes directly the damage model with the realistic damage process of the GaAs PHEMT device injected by EMP. Based on this model, the damage thresholds with terms of the damage power and damage energy are investigated. In addition, adopting the curving fit method, the GaAs PHEMT damage power formula related to the pulse width is also established.

2. Damage model

2.1. Simulation model

Figure 1 shows the geometric structure of GaAs PHEMT analyzed in this work, which consists of GaAs substrate, InGaAs channel layer, AlGaAs spacer layer, δ-doping layer which provides carriers for the channel layer, AlGaAs barrier layer, GaAs cap layer and passivation layer. It can be seen that there is a spacer layer between the InGaAs channel layer and δ-doping layer to reduce the coulomb impurity scattering and increase the electronic mobility of the carriers in the channel. The thermal electrode is located at the bottom of the device in which the lattice temperature is fixed to be 300 K.

Presently, the researchers mostly take the step voltage pulse as the signal model in the study of the damage effect of the semiconductor device with the EMP event.[7–9] In this work, a step voltage pulse with a rising time of 0.1 ns and amplitude of 9 V is applied to the gate electrode of the device, in which the other two electrodes are biased at 2 V on the drain and grounded on the source, respectively. With the help of the device simulation software Sentaurus TCAD, the internal physical behavior of the device injected with pulse signal is simulated by solving the Poisson equation, the carrier continuity equation, the carrier temperature and heat flow equations. Here, we take the lattice temperature reaching 1511 K, the melting point of GaAs, as the damage criterion of the device.

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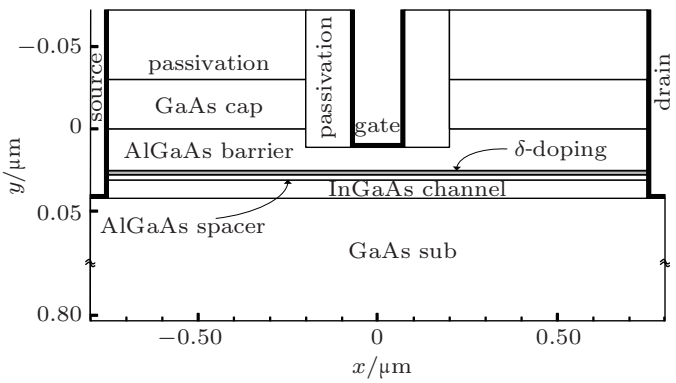


Fig. 1. Two-dimensional GaAs PHEMT structure.

2.2. Damage effect and mechanism

When the device is subjected to step voltage pulse on the gate electrode, there is a current path emerging between the gate and the InGaAs channel due to the Schottky barrier being lowered. Considering the potential differences between the gate, source and drain, the current path is closer to the source and the maximum electric field is located below the gate near the source, which then leads to the temperature distribution of the device (Fig. 2). As the increase of the injection voltage, when the electric field strength reaches to the critical value at which avalanche breakdown happens, the carriers increase rapidly. With the time going by, the carriers below the gate side can be transferred quickly because of the higher electric field at this position. Beneath the gate center, the electrons can be injected into the gate electrode, and the holes begin to accumulate, which makes the hole density below the gate center higher than at other positions (Fig. 3(a)) and causes the the electric field to shift to this position[10] (Fig.3(b)). This effect also makes the current density correspondingly extend to the barrier layer center (Fig. 3(c)). With the time increasing,

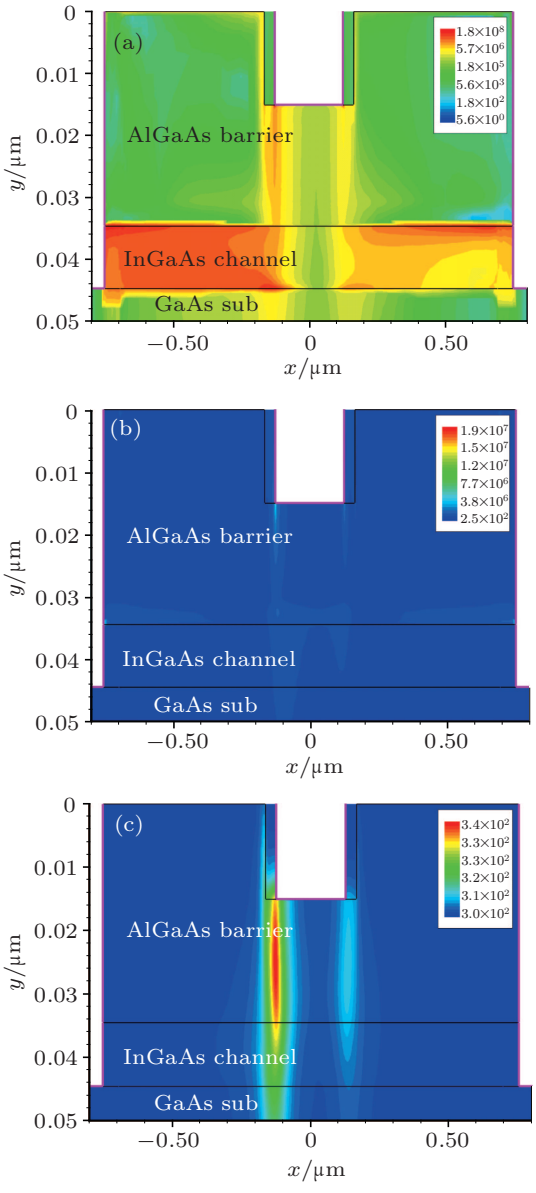


Fig. 2. (color online) Distributions of the device parameters: (a) current density (A/cm^2), (b) electric field (V/cm), and (c) temperature (K), at $t = 0.08$ ns.

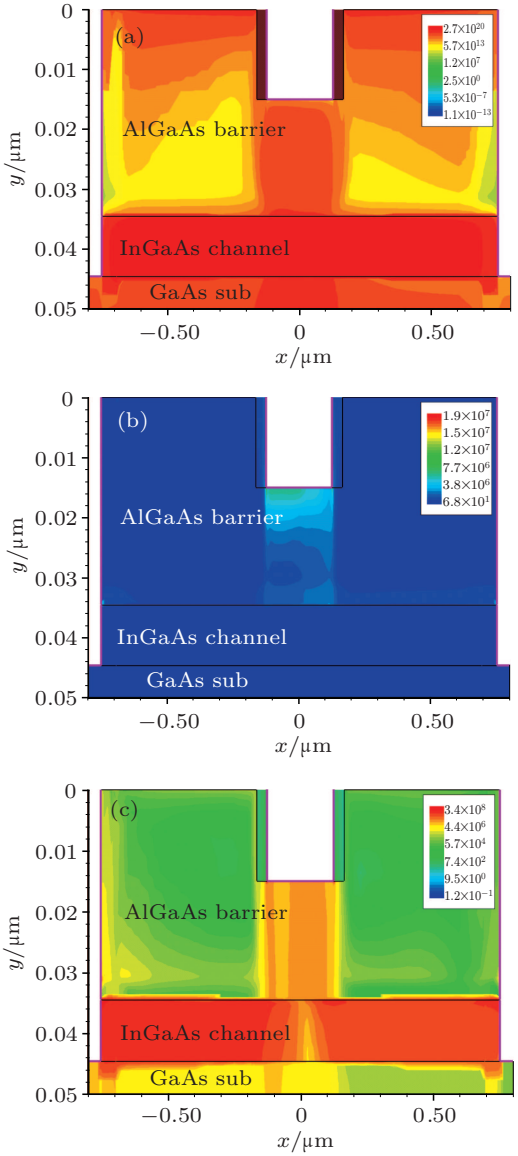


Fig. 3. (color online) Distributions of the device parameters: (a) hole density (cm^{-3}), (b) electric field (V/cm), and (c) current density (A/cm^2), at $t = 0.25$ ns.

there is an electric field peak forming beneath the gate center near the drain (Fig. 4(a)), and a current density peak in the barrier layer is centered near the drain finally (Fig. 4(b)). Figure 4(c) shows the temperature distribution of the device at the burnout time. It can be seen that the maximum temperature is located beneath the gate center near the drain, which can be easily understood because the electric field and current density peaks are both at this position. It should be noted that the device hotspot is not always at the same position, which transfers from the location beneath the gate near the source (Fig. 2(c)) to that beneath the gate center near the drain (Fig. 4(c)) in the damage process of the device.

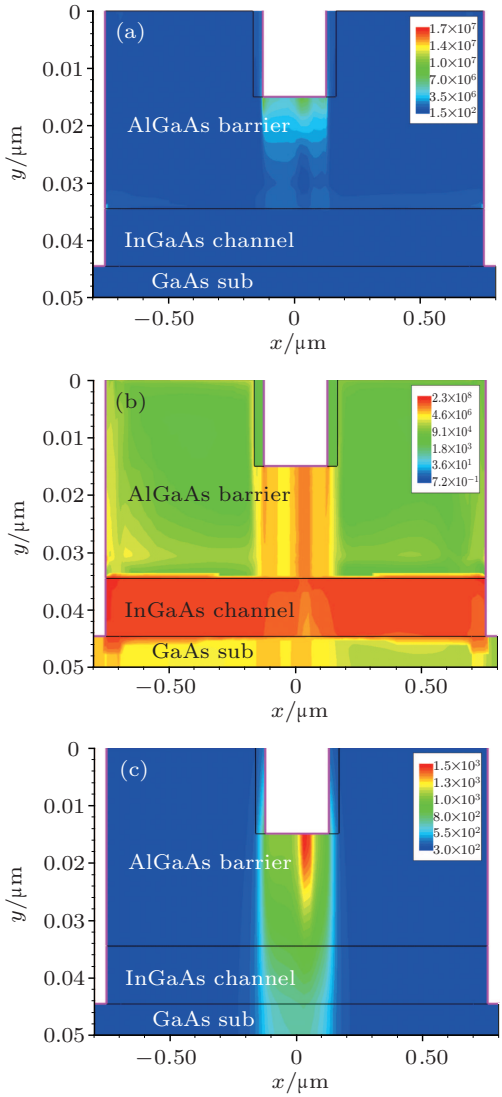


Fig. 4. (color online) Distributions of the device parameters: (a) electric field (V/cm), (b) current density (A/cm^2), and (c) temperature (K), at $t = 3.40$ ns.

3. Damage threshold analysis

Generally, the EMP-induced damage effect on the device is divided into three cases by the pulse width:[3,4,11] for the short pulse on the assumption that the device is adiabatic, for the long pulse with considering heat dissipation, and for the steady state with thermal equilibrium established. Figure 5 shows the variation rules of the damage threshold with the pulse width under different phases. In the EMP-injected process (nanosecond order of magnitude) the device is under the adiabatic condition, in which empirical formulas with terms of the damage power and energy shown in Fig. 5 accordingly are as follows:

$$P = C_1 T^{-1}, \tag{1}$$

$$E = B_1. \tag{2}$$

In order to analyze the damage threshold of the GaAs PHEAT, such as the damage power, damage energy, we simulate the burnout process of the device with different amplitudes of step voltage pulse based on the damage model illustrated in Section 2. Here, the pulse width is the duration time of injection signal before the device is burnout, the damage power is the average power absorbed by the device, and the damage energy is determined by calculating the instantaneous voltage and current waveform on the device each as a function of the pulse width.

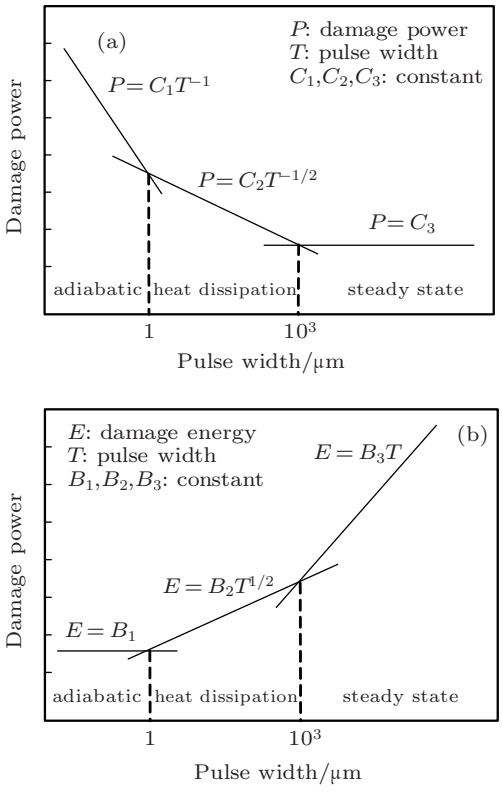


Fig. 5. Variation rules of the damage threshold ((a) damage power and (b) damage energy) with pulse width.

3.1. Variation of the damage power with pulse width

Figure 6 shows the relationship between the damage power and the pulse width. It indicates that the damage power decreases with the increase of the pulse width, which illustrates that the device EMP-induced damage is an energy dependent process. Adopting the curve fitting software to fit the

data points, the relationship between the damage power P and the pulse width T meets the formula

$$P = 0.08T^{-0.57}, \tag{3}$$

which has a high correlation coefficient of up to 0.99.

From the comparison between formulas (1) and (3), it can be seen that the pulse width exponent of formula (3) obtained in this paper is higher than that of the empirical formula (1). This is because of the hotspot transferring in the damage process of the device analyzed in Subsection 2.2 previously. Part of the injected power is absorbed by the hotspot beneath the gate near the source (Fig. 2(c)), which is not the final damage location of the device (Fig. 4(c)). However, the empirical formula is computed based on one fixed hotspot.[4] It is easily understood that the power in formula (3) needs more time to damage the device than that in formula (1). Therefore, the pulse width index of the damage power formula uses −0.57 to assess the EMP-induced damage effect on the GaAs PHEMT more realistically.

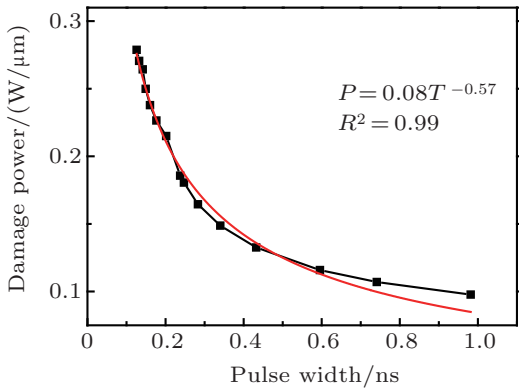


Fig. 6. (color online) Dependence of the damage power on pulse width.

3.2. Variation of the damage energy with signal amplitude

From the analysis in Subsubsection 2.3.1, it is noted that the device damage belongs to energy-induced damage under the injection of EMP. Figure 7 shows the relationship between the damage energy and the signal amplitude. It can be seen that the damage energy decreases with the increase of the signal amplitude, and then changes little once the signal amplitude reaches to a certain level. When the signal amplitude is low, the damage energy is also dissipated at the location below the gate near the source beside the damage position below the gate center near the drain. With the increase of the signal amplitude, the pulse width decreases, which gives rise to the decrease of energy absorbed by the location below the gate near the source (outside the damage position). Thus, the damage energy of the device also decreases accordingly. However, when the signal amplitude is up to 11.5 V, the device is damaged beneath the gate near the source before forming the electric field and current density peaks beneath the gate center near the drain (Fig. 8). The maximum temperature is at the same position in the damage process of the device. So, the damage energy is almost a constant under the high signal amplitude, which is consistent with empirical formula (2).

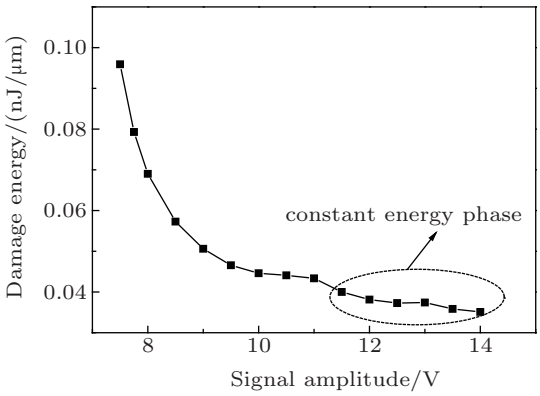


Fig. 7. Dependence of the damage energy on signal amplitude.

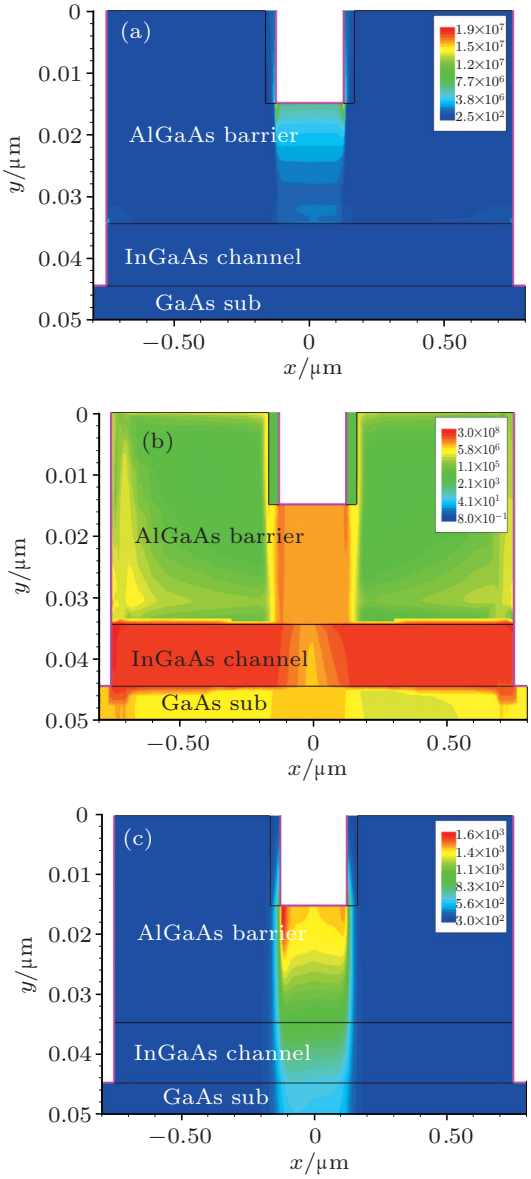


Fig. 8. (color online) Distributions of the device parameters: (a) electric field (V/cm), (b) current density (A/cm^2), and (c) temperature (K), under 11.5 V injection voltage.

4. Comparison with experimental results

Reference [12] shows the HPM induced injection experiment on the GaAs PHEMT. Subjected to the microwave signals is the gate electrode of the device, which has the same structure as that in Subsection 2.1. Experimental results show that both positions beneath the gate near the drain and source could possibly be damaged (Fig. 9), which are consistent with the simulation results in this paper. In Ref. [12] only the experimental phenomenon was described, but the interior damage mechanism of the device was not analyzed. From the analysis in this paper, it can be seen that the change of the damage location is due to the variation of the signal amplitude. When the low amplitude of step voltage pulse is applied to the device, the damage position occurs beneath the gate center near the drain, and when the amplitude of the applied step voltage is high enough the damage location appears beneath the gate near the source firstly.

Here it should be pointed out that although the injection signal in this work is different from the one in Ref. [12], damages induced by both the step voltage pulse and microwave pulse are both energy dependent processes,[13] which has a certain similarity, i.e., they have the same structures and injection locations. The good agreement between the simulation results and experimental results implies that the damage model established here can predict the damage effect of EMP-induced injection on the GaAs PHEMT well.

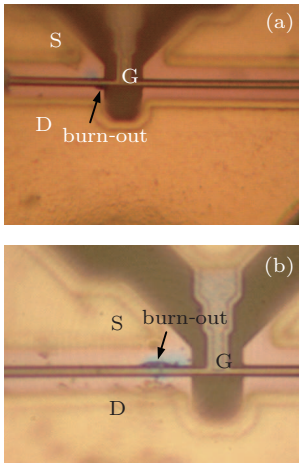


Fig. 9. (color online) Photomicrographs of damaged devices: (a) sample $11^{\#}$ and (b) sample $12^{\#}$, with microwave pulse.[12]

5. Conclusions

It is necessary to have a knowledge of the damage threshold in the EMP assessments and hardening designs. The method used in this study is distinctively different from the traditional method of the threshold study that is based on the thermal model: here we directly use the damage effect and mechanism of the typical device as the damage model. It is demonstrated that the empirical formula $P = C_1 T^{-1}$ should be modified into P= $P = C_1 T^{-0.57}$ for the GaAs PHEMT due to the hotspot shifting in the damage process of the device. Because the damage position varies with the amplitude of injection signal, the damage energy is not a constant, which is different from the empirical viewpoints. It should be noted that in this paper we only investigate the difference between the damage threshold obtained from the empirical viewpoint and that from the simulation analysis. In the future research, the experiment data will also be considered to fit the damage power formula with the pulse width index obtained in this paper.

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