Self-aligned-gate AlGaN/GaN heterostructure field-effect transistor with titanium nitride gate

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Self-aligned-gate heterostructure field-effect transistor (HFET) is fabricated using a wet-etching method. Titanium nitride (TiN) is one kind of thermal stable material which can be used as the gate electrode. A Ti/Au cap layer is fixed on the gate and acts as an etching mask. Then the T-shaped gate is automatically formed through over-etching the TiN layer in 30% H_2O_2 solution at 95 °C. After treating the ohmic region with an inductively coupled plasma (ICP) method, an Al layer is sputtered as an ohmic electrode. The ohmic contact resistance is approximately 0.3 Ω·mm after annealing at a low-temperature of 575 °C in N_2 ambient for 1 min. The TiN gate leakage current is only 10^{-8} A after the low-temperature ohmic process. The access region length of the self-aligned-gate (SAG) HFET was reduced from 2 μm to 0.3 μm compared with that of the gate-first HFET. The output current density and transconductance of the device which has the same gate length and width are also increased.

Keywords: AlGaN/GaN HFETs, wet etching, self-aligned-gate

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1. Introduction

For high-power and high-frequency applications, the AlGaN/GaN heterostructure field-effect transistor (HFET) is regarded as an excellent candidate because of its high current density, high breakdown voltage and high saturation velocity performance.[1,2] But, the large access region between the gate and the source/drain in the conventional lithography process will restrict the current and the operation frequency due to the increase of access resistance. Ion implantation is a method that can effectively reduce the access resistance. But this process is hard for industrial application because it is complicated and expensive.[3] From a fabrication viewpoint, using the self-aligned-gate (SAG) process to suppress the access region can alleviate this problem.[4] In a typical SAG process, a T-shaped gate is first fabricated and then used as a mask directly for ohmic metal evaporation. However, the fabrication of the SAG structure always encounters two problems. One is that the Schottky gate structure will degrade after annealing with source/drain electrodes since the annealing temperature is commonly higher than 800 °C,[5] and the other is that the fabrication of T-shaped gate always needs multiple lithography or a multilayer photoresist.[6] Therefore, it is relatively difficult and complex to realize a T-shaped gate with good morphology especially for AlGaN/GaN HFETs.

In this paper, we use the wet-etching method to fabricate the SAG AlGaN/GaN HFETs. The whole fabrication process for the T-shaped gate is simplified into two steps with just one-time lithography. Furthermore, a low-temperature ohmic process which only needs annealing below 600 °C is used to form the ohmic contact.[7,8] Assisted with this process, the SAG AlGaN/GaN HFET is fabricated with good device performance. The thermal-stable titanium nitride (TiN) gate electrode shows no obvious degradation after low-temperature ohmic annealing.

2. Synthesis and wet-etching of TiN

TiN film with a thickness of 100 nm was deposited on sapphire substrate by reactive sputtering in Ar and N_2 mixture ambient with a Ti target.[9] A 4-point method using a bridge structure with a length of 400 μm and a width of 15 μm was used to evaluate the wet-etching rate of TiN (inset in Fig. 1). From our previous study, solutions of BHF/HNO_3, NH_4OH, and H_2O_2 can be used to etch the TiN layer. Considering the ability to control the etching speed and the compatibility with the semiconductor technology, H_2O_2 is regarded as the most suitable etchant. A 30% H_2O_2 solution was heated to 95 °C to etch the TiN pattern. The 4-point method was used to measure the conductances of the patterned TiN film, after it had been etched for 0, 15, 35, 55, 75, and 85 s, respectively. The conductance of the TiN versus the etching time is shown in Fig. 1. The fitting result shows that the conductance decreases linearly with etching time with a slope of −2.31 mS/s and an

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intercept of 2.05 mS. In the etching process, even the TiN film can also be etched in the lateral direction, the width of the TiN bridge structure can be assumed to be a constant. Because even the etching depth in the lateral direction is equal to the TiN thickness, it only takes 1.32% of the 4-probe structure's whole width. Assuming the etching rate α to be a constant, the conductance G with the etching time t can be described as a linear relationship as follows:

$$G = \frac{\mathrm{d}I}{\mathrm{d}V} = \frac{W(T_0 - \alpha t)}{\rho L}, \tag{1}$$

where I is the current of the patterned TiN film, V is the voltage of the patterned TiN film, W is the pattern width, T_0 is the initial thickness (100 nm), ρ is the resistivity of the TiN film, and L is the pattern length. By using the slope and the intercept in Fig. 1, the calculated etching rate α is approximately 1.12 nm/s.

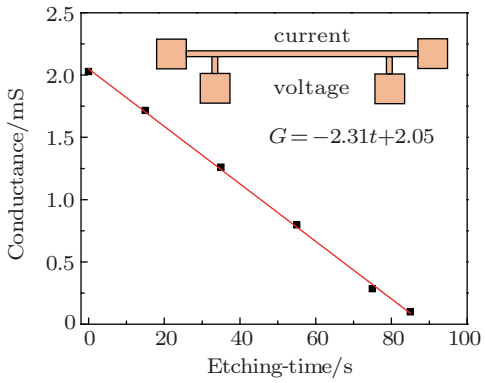


Fig. 1. (color online) Fitting result of the conductance against the etching time for the 4-point TiN pattern.

3. Device fabrication and characterization

The epitaxial layers of the AlGaN/GaN HFET were grown by metal organic chemical vapor deposition (MOCVD) on a silicon substrate. It consisted of a buffer layer, a 1-μm i-GaN, a 25-nm i-AlGaN, and a 2-nm i-GaN from the bottom to the top. The Al mole fraction of the AlGaN layer was 25%. From the Hall measurement at room temperature, the mobility and average sheet resistance of the two-dimensional electron gas were about 2459 $\mathrm{cm^2 \cdot v^{-1} \cdot s^{-1}}$ and 385 Ω/□, respectively.

The SAG HFETs were fabricated to test the feasibility of this method and to evaluate the device performance. Device fabrication was based on a standard photolithography technology. Mesa isolation with a thickness of 60 nm was first implemented by inductively coupled plasma (ICP) etching. Then, a 200-nm thick TiN layer was deposited on the whole surface of the wafer by the reactive sputtering process.[10,11] A 3-μm-long gate footprint with a width of 55 μm was patterned using photolithography. Then a gate cap layer of Ti/Au (120 nm/120 nm) was deposited on the TiN surface. After the lift-off process, the left Ti/Au layer could act as an etching mask of the gate region. The whole sample was then dipped into a 30% H_2O_2 solution at 95 °C for 8 min, and a T-shaped gate was formed due to the isotropic property of the wet-etching method. What we need to mention is that the whole fabrication process of the T-shaped gate included only two steps and just one-time lithography. The source/drain region was treated by $SiCl_4$ plasma for 20 s with an ICP/bias power of 100 W/100 W, $SiCl_4$ flow of 3 sccm and treating pressure of 0.25 Pa, and then cleaned in BHF/HNO_3 (1:1) solution for 30 s to remove the possible Si contamination induced at the ICP treatment process.[12] As ohmic metal, Al film with a thickness of 100 nm was then deposited and annealed in N_2 ambient at 575 °C for 1 min to form low temperature ohmic contact. Figure 2 shows the cross-sectional view of an SAG HFET.

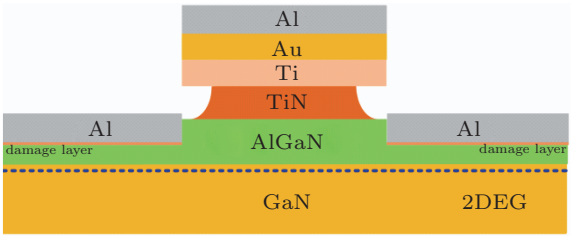


Fig. 2. (color online) Cross-section view of the SAG HFET.

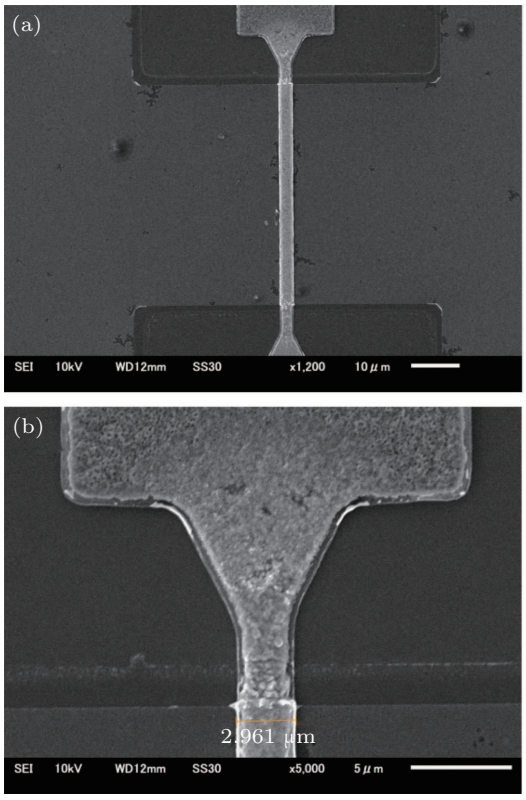


Fig. 3. (color online) Typical low (a) and high (b) magnification SEM image of the SAG HFET.

Based on the etching rate and the etching time of the SAG structure, the etching depth in our experiment could be calcu-

lated to be approximately 500 nm. Because the thickness of the TiN layer was approximately 200 nm, the lateral recess under the gate cap layer was assumed to be approximately 300 nm on each side due to the isotropic etching effect. A keystone shape TiN layer was assumed to have a top width of approximately 2 μm and the bottom width of approximately 2.4 μm. The width of the Ti/Au layer was designed to be 3 μm, so the width of the access region was approximately 0.3 μm on each side. Figure 3 shows the SEM images of the SAG HFET. From Fig. 3(b), it can be confirmed that the cap layer of the gate is 2.96 μm, which is consistent with the recommended value. However, it is difficult to take a cross-section view of the SEM photograph to confirm the size of the access region. Furthermore, there are some damages caused by the Al ball-up in the annealing process in the ohmic region (Fig. 3(a)), an Al/TiN structure can be utilized to solve this problem and will be used to fabricate the SAG HFETs in future.[7] The ohmic contact was evaluated by the transmission line model (TLM) method.

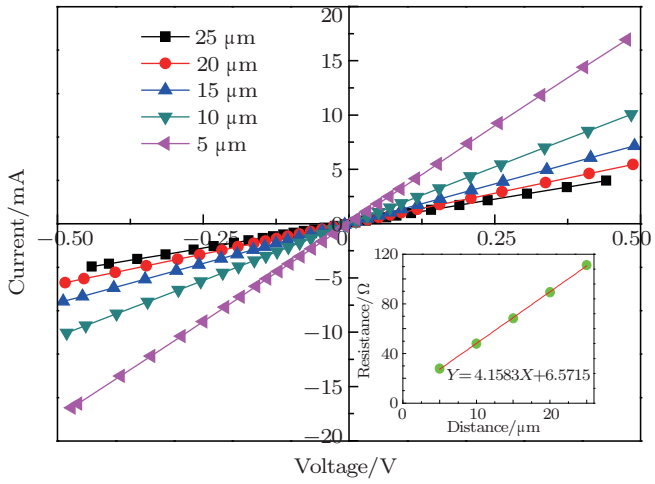


Fig. 4. (color online) *I*–*V* characteristics and TLM fitting result of the TLM pattern.

Figure 4 shows the current–voltage (*I*–*V*) characteristics recorded on the TLM patterns with intervals of 5, 10, 15, 20, and 25 μm, respectively, and a width of 96 μm. The linear curves suggest that good ohmic contact behavior was formed between the metal stack and the semiconductor. An ohmic contact resistance of 0.32 Ω·mm and a sheet resistance of 399 Ω/□ were calculated by the TLM method. In order to illustrate the advantage of the low temperature ohmic contact technology for SAG HFET, we fabricated some circular TiN Schottky diodes (with a diameter of around 150 μm) to evaluate the Schottky leak currents at different annealing temperatures. The *I*–*V* characteristics of the circular TiN Schottky diode are shown in Fig. 5(a). The gate leakage current without the annealing process was below 10^{-5} A. While after being annealed at 575 °C and 850 °C for 1 min, the leakage currents increases to 10^{-5} A and 10^{-4} A, respectively. This result shows that the annealing process can damage the Schottky contact and increase the leak current, especially after being annealed at high temperature. Fortunately, the leakage current under being annealed at 575 °C is comparable to the sample without being annealed. The calculated ideality factor n and Schottky barrier height (SBH) of the TiN shottky diode under 575 °C annealing are 2.50 eV and 0.727 eV from the thermionic emission theory. The gate leakage of the bar-type SAG HFET as shown in Fig. 5(b) is only 10^{-8} A, which confirms that the low temperature ohmic contact is useful for SAG HFET. In Fig. 6, the output and the transfer characteristics of the SAG HFETs are compared with a gate-first HFET, which was fabricated by the same low temperature ohmic process on the same wafer. The gate length and width of gate-first HFET were 2 μm and 55 μm respectively, and the access region size between gate and source/drain was 2 μm. For the gate-first HFET, a maximum current density and a transconductance were measured to be 500 mA/mm and 125 mS/mm respectively at a gate–source voltage of 1 V and a drain bias of 10 V. While for the SAG HFET, the maximum current density and the transconductance were measured to be approximately 750 mA/mm and 200 mS/mm respectively under the same condition. The increases of the drain current and the transconductance are ascribed to the decrease of access region from 2 μm to 0.3 μm in for the two devices.

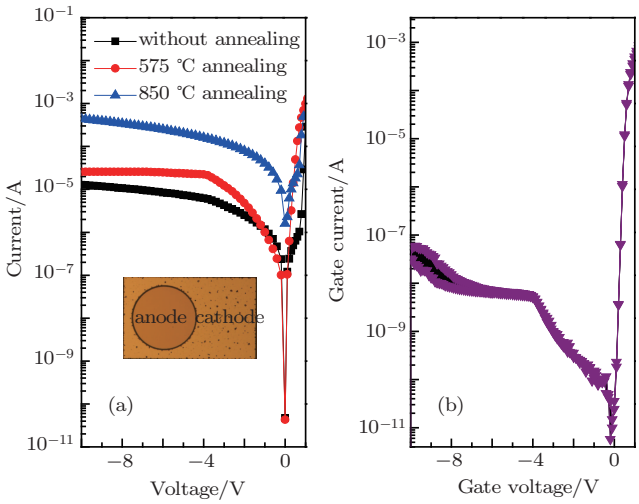


Fig. 5. (color online) *I*–*V* characteristics of (a) the circular TiN Schottky diode and (b) the SAG HFET.

Generally, the gate length is required to be as small as possible for the high frequency application of the AlGaN/GaN HFET. Herein, we show that the wet-etching method as well as the low temperature ohmic contact technology is useful for SAG HFET fabrication. However, our result is just an evaluation method for the high frequency SAG HFET because of the gate length at the cap layer and the bottom of the T-shaped gate were 3 μm and 2 μm, respectively. Compared with our previous SAG HFET (with a gate length of approximately 500 nm)

fabricated by electronic beam (EB) lithography, there still exists a large margin.[6] In the future, we need to further combine these two technologies with the EB lithography to fabricate an SAG HFET with nanoscale size.

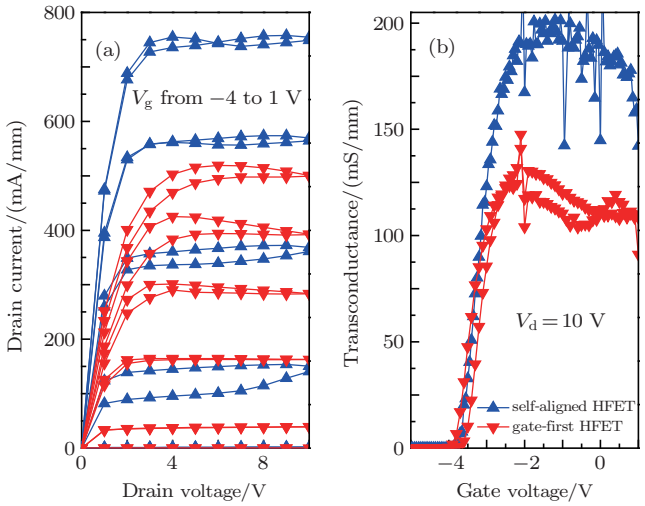


Fig. 6. (color online) Output (a) and transfer (b) characteristics of the SAG HFET and the gate-first HFET.

4. Conclusions

An SAG AlGaN/GaN HFET is fabricated based on wet-etching TiN gate and low-temperature ohmic process. Assisted by the ICP dry etching treatment, the ohmic contact resistance is only 0.32 Ω·mm. For the TiN gate structure, the gate leakage current is only 10^{-8} A under the annealing process at 575 °C, confirming that the TiN gate is thermally reliable. An SAG HFET shows good electrical performance. The drain current density is more than 750 mA/mm and the transconductance is over 200 mS/mm under a drain bias of 10 V and gate–source voltage of 1 V, which are much higher than those of a gate-first HFET with the same gate length and width. Since the fabrication process is easy and the TiN Schottky gate is thermally stable, this method is suitable for improving the device performance.

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