Study on influences of TiN capping layer on time-dependent dielectric breakdown characteristic of ultra-thin EOT high-*k* metal gate NMOSFET with kMC TDDB simulations*

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The thickness effect of the TiN capping layer on the time dependent dielectric breakdown (TDDB) characteristic of ultra-thin EOT high-*k* metal gate NMOSFET is investigated in this paper. Based on experimental results, it is found that the device with a thicker TiN layer has a more promising reliability characteristic than that with a thinner TiN layer. From the charge pumping measurement and secondary ion mass spectroscopy (SIMS) analysis, it is indicated that the sample with the thicker TiN layer introduces more Cl passivation at the IL/Si interface and exhibits a lower interface trap density. In addition, the influences of interface and bulk trap density ratio N_{it}/N_{ot} are studied by TDDB simulations through combining percolation theory and the kinetic Monte Carlo (kMC) method. The lifetime reduction and Weibull slope lowering are explained by interface trap effects for TiN capping layers with different thicknesses.

Keywords: high-*k* metal gate, TiN capping layer, TDDB, interface trap density

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1. Introduction

High-*k* metal gate stacks have been used for improving MOSFET performance since 45 nm technology node.[1–4] High dielectric constant material successfully suppresses the leakage of gate, however, the reliability issue of the high-*k* metal gate device becomes a challenge. The gate stack degradation and process optimization for trap reduction have been widely studied.[5–8]

In this paper, TiN is used as the capping layer after being deposited with high-*k* dielectric. Due to work function tuning and reliability consideration, the thickness of TiN capping layer is a trade-off for process optimization.[9–11] It is reported that the oxygen diffusion model and multi-phase soft breakdown could be used to explain the TiN thickness effect.[9] However, no detailed relation between bulk trap and time to breakdown is given and the Weibull slope change is not well explained.

As one of the most important reliability issues, time dependent dielectric breakdown (TDDB) is related to the bulk and interface trap generation in ultra-thin EOT high-*k*/IL/substrate stacks. Longer time to breakdown and larger Weibull slope are of benefit to lifetime assessment.[6] In recent studies, simulations combining percolation theory and the Monte Carlo (MC) method were proved to be a useful tool in TDDB analysis.[12,13]

In this paper, the thickness effects of the TiN capping layer on the TDDB characteristic of NMOSFET are studied. TDDB and SILC characteristics are compared for different TiN thickness of 1.4 nm and 2.4 nm. Both transconductance degradation and charge pumping results show that the interface trap plays an important role in dielectric degradation. The origin of interface trap difference is studied by SIMS measurement. Finally, the effects of bulk and interface trap density on TDDB are simulated by combining percolation theory and the kMC method. The Weibull distribution parameters are systemically studied by varying the ratio between bulk and interface trap density.

2. Experiment

In this paper, NMOSFET devices under tests are fabricated by a standard gate last process. Interfacial layer and HfO_2 are chemically formed by ozone oxidation and atomic layer deposition (ALD), respectively. Then, post-deposition annealing (PDA) in nitrogen at 450 °C is performed. Ultra-thin TiN films with thickness values of 1.4 nm and 2.4 nm are deposited as a capping layer. Then 5-nm TiAl (PVD), 5-nm TiN (PVD), and 75-nm W (ALD) are fabricated as following gate stacks and the whole gate stacks structure as shown in

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Fig. 1.

In this work, devices with TiN capping layers of different thickness and $L_g = 0.5$ μm have a similar threshold voltage in a range of 0.23 V∼0.25 V. The EOT results are 0.85 nm and 0.87 nm for 1.4-nm TiN and 2.4-nm TiN, respectively. The nominal W/L ratios of NMOSFET are 8 μm×2 μm and 1 μm×0.5 μm for SILC and TDDB measurement, respectively. All reliability measurements are done by an Agilent 4156C at 125 °C. All tests are done by constant voltage stress, with considering the worst condition for devices reliability.

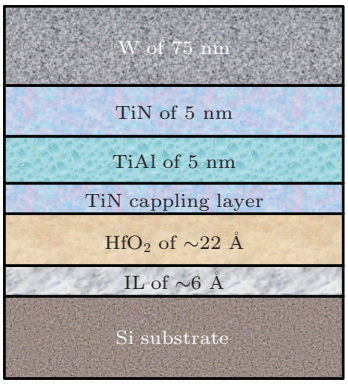


Fig. 1. (color online) High-k metal gate stacks of NMOSFET under test. The thickness of TiN capping layer is varied for process optimization.

3. Results and discussion

3.1. SILC and TDDB characteristics

As shown in Fig. 2, the SILC characteristic at low gate voltage is monitored during stress time. For the device with 1.4-nm TiN, $\Delta I_g/I_{g0}$ peaks are observed at −1.2 V, −0.4 V, and 0.4 V on the x axis, and the highest increment of SILC is more than 400 times. While, for 2.4-nm TiN devices, much lower SILC is observed only at −0.4 V with an increment of less than 150 times. According to multi-phonon trap assisted tunneling theory,[14] the peak position on the x axis is based on the gate stack composition, and the increment of $\Delta I_g/I_{g0}$ is varied with the trap generation rate. Thus, it is demonstrated that a more severe trap is generated in a thinner TiN device.

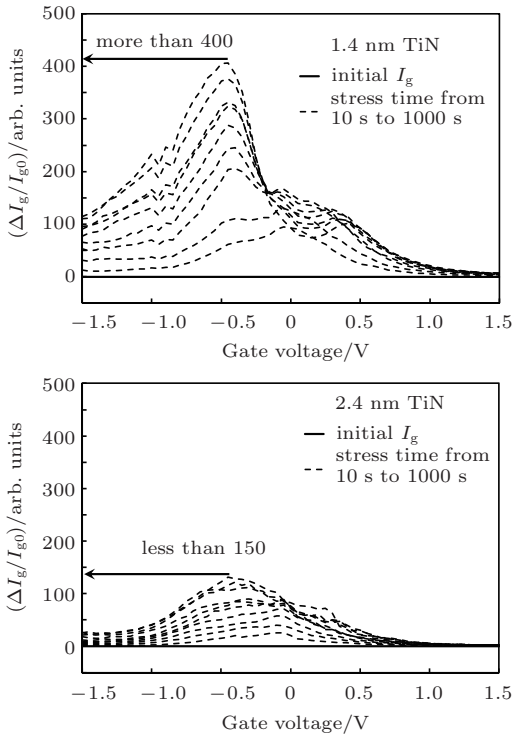


Fig. 2. $\Delta I_g/I_{g0}$ evolutions with gate voltage at low gate voltage for different stress times.

TDDB is measured at a gate bias 1.8 V, and 16 devices are used for making a statistical analysis, and the results are shown in Fig. 3. It is found that with 2.4-nm TiN capping layer, time to breakdown is improved nearly 10 times higher than that of 1.4-nm TiN devices. The Weibull slopes are both nearly 0.9. It is less than the expectation in a range from 1 to 2 for ultra-thin EOT devices.[2,9,12,13] Neither the reduction of time to breakdown nor the shallow Weibull slope value is good for reliability consideration. Thus, from the view of reliability, a thicker TiN layer is much more beneficial.

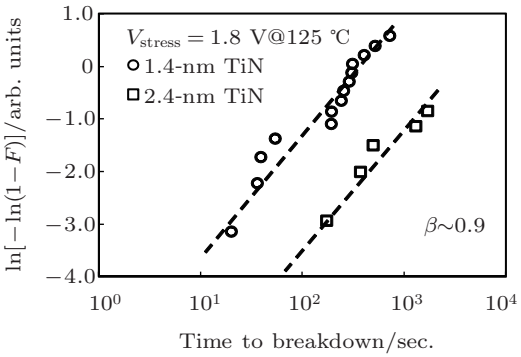


Fig. 3. TDDB results for 1.4-nm and 2.4-nm TiN NMOSFET devices.

3.2. Interface trap degradation

To confirm the cause of gate stack degradation, the transconductance and threshold voltage shift are monitored during SILC stress. As shown in Fig. 4, V_T shift and G_m degradation are extracted from I_d–V_g curves. During stress time, an obvious G_m degradation is observed (more than 40%). It is concluded that the interface trap degradation is severe under such a high stress condition, which is different from PBTI characteristic in our previous work.[15,16]

The charge pumping method is used to directly measure interface trap density in fresh devices. In charge pumping measurement, the pulse amplitude is constant and base level voltage sweep is applied. The frequency for charge pumping is 500 kHz. The amplitude of pulse is 1.2 V and base voltage sweep is from −0.6 V to −0.3 V. As shown in Fig. 5, the interface trap densities are calculated from the charge pumping current based on the relation:

$$N_{it} = \frac{I_{CP}}{qfA},$$

where q is the elementary charge, f is the frequency of charge pumping measurement, and A is the effective gate area. The

results show that the device with a thinner TiN layer has an interface trap density about twice that with the thicker TiN layer. Thus, it could be concluded that a thicker TiN layer induces less interface trap.

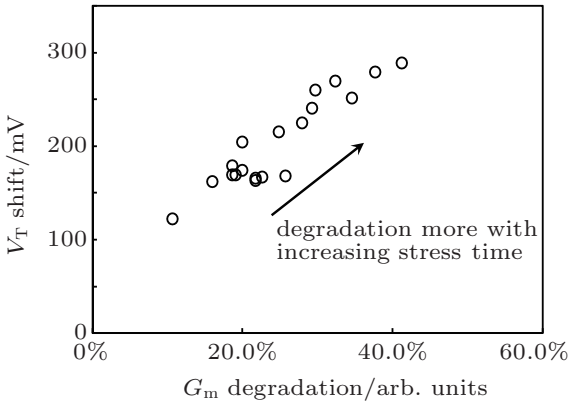


Fig. 4. V_T shift versus G_m degradation during stress time.

To study the origin of the TiN thickness effect on the interface state, SIMS is used to analyze the elemental compositions in the gate stacks. The SIMS results are shown in Fig. 6. Due to two layers TiN components in the gate stacks and the peaks of TiN concentration are mixed, the boundaries of TiN are identified from the other components. Thus, the separations for each layer are mainly determined from the peaks of TiAl and HfO_2 at about 40% of maximum concentration. From element analysis results, it is found that a significant difference for Cl is observed. The peak of Cl is observed at the position of the TiN cap layer and the peak values are 5.01×10^{20} atoms/cc and 1.84×10^{20} atoms/cc for 1.4-nm and 2.4-nm TiN caps, respectively. Meanwhile, the concentration of Cl at IL increases from 3.84×10^{18} atoms/cc to 1.36×10^{19} atoms/cc for thinner TiN. Also note that there is no obvious difference for other elements, such as C, O, H, and F (not shown in figures). Thus, it is concluded that Cl is introduced in the ALD TiN deposition process due to using $TiCl_4$ as precursor material in this work. The device with thicker TiN layer contains more Cl elements in the whole stacks.

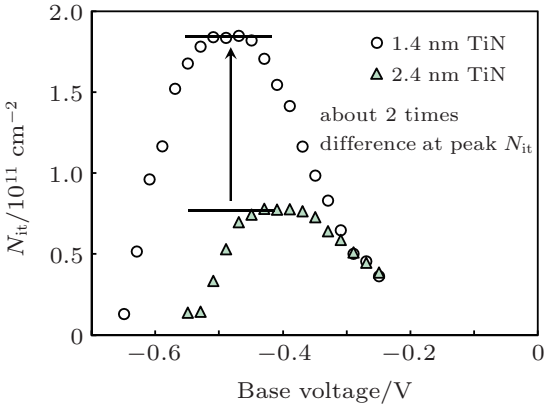


Fig. 5. (color online) Plots of interface trap density versus base level voltage for different thickness TiN layers.

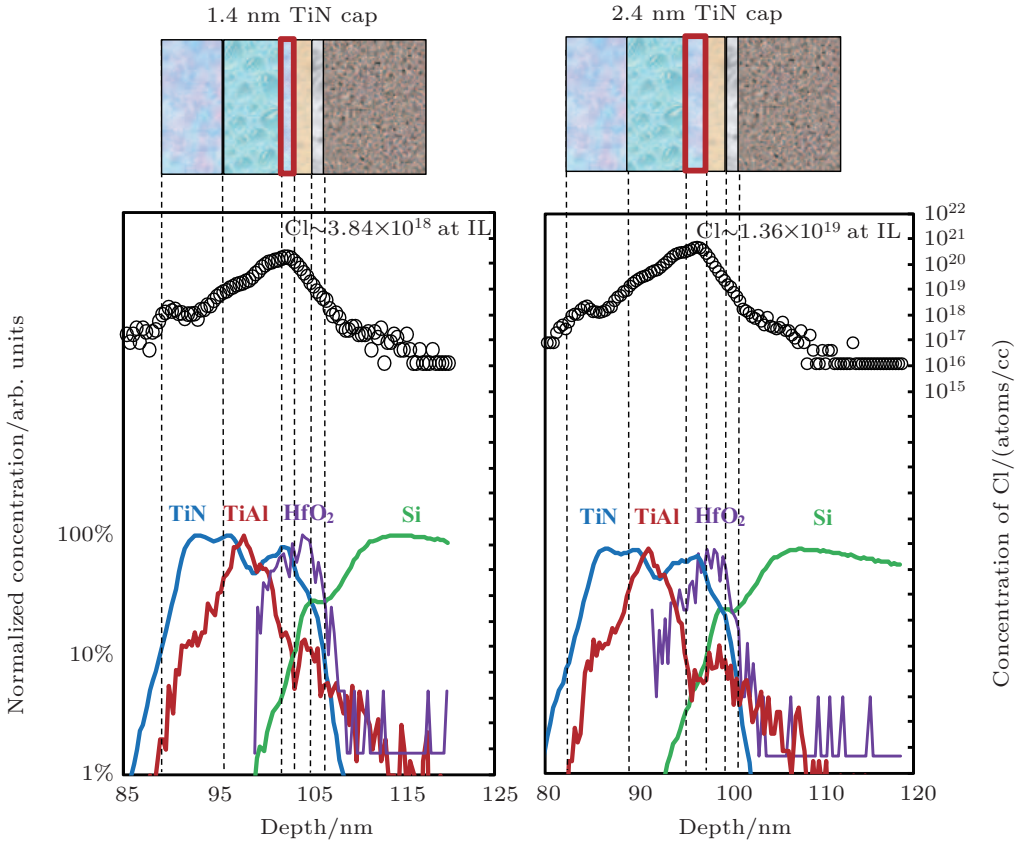


Fig. 6. (color online) SIMS measurement results for elemental analysis.

Based on the above results, the interface trap density difference could be described as the Cl passivation effect. Firstly, Cl is introduced when depositing the TiN. Then, in the subsequent annealing process, Cl diffuses from TiN layer to dielectrics and substrate. It is reasonably assumed that Cl passivation happens at the dangling bonds of the IL/Si interface, which is in detail studied by Park *et al.*[17] Thus, it is concluded that a thicker TiN capping layer will introduce higher Cl concentration and the passivation effect of Cl reduces interface trap density.

3.3. Simulations of trap density effects on TDDB characteristic

Based on the above results, the effects of interface trap density on the TDDB characteristic are studied in simulations. A cell-based simulator is set up by combining percolation theory with the kMC method as described in Ref. [13]. The physical layers of dielectric stacks are treated as 2 high-k layers +1 interfacial layer with the trap sizes of $a_{\rm HK} = 10$ Å and $a_{\rm IL} = 6$ Å for high-k and IL, respectively. Trap generation rate time exponent for bulk trap and interface trap are $\alpha = 0.38$ and $\alpha_{\rm it} = 0.16$, respectively. All these parameters are in accordance with those in Ref. [13].

Different ratios of interface and bulk trap density are simulated, and the distributions of time to breakdown are studied. As shown in Fig. 7, Weibull distributions are obtained for different ratios between $N_{\rm it}$ and$N_{\rm ot}$, where $N_{\rm ot}$ is set to be a constant value. It is indicated that when $N_{\rm it} \ll N_{\rm ot}$, the TDDB distributions show less change with $N_{\rm it}$ increasing. The lifetime is determined by bulk trap density and Weibull slope is determined by whole dielectric stacks (empty symbols in Fig. 7). Bulk trap dominant results are consistent with those of Chen's work and the oxygen diffusion model. However, for $N_{\rm it} \gg N_{\rm ot}$ conditions, time to breakdown decreases fast with $N_{\rm it}$ increasing. Meanwhile, Weibull slope degrades compared with that for bulk trap dominant conditions (solid symbols).

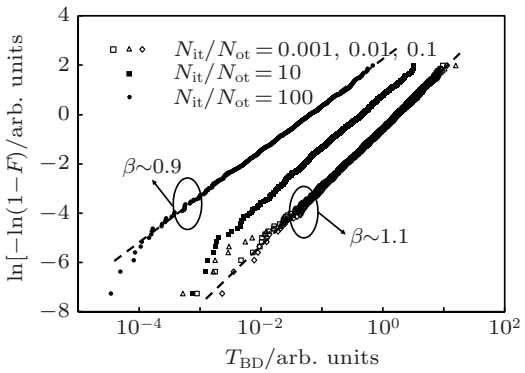


Fig. 7. Simulated TDDB distributions of different trap density ratios of bulk and interface.

It is demonstrated that when interface trap density is much larger than bulk trap density, the interface trap will strongly influence TDDB characteristic. The scaling $T_{\rm BD}$ follows a power law with the interface trap density as follows (see Fig. 8):

$$T_{\rm BD} \propto (N_{\rm it})^{-n}$$

where n is the power law factor, and it is about 0.9 in this work. Weibull slope decreases from 1.1 to 0.9, which is consistent with the percolation relation between 3α and $2\alpha + \alpha_{\rm it}$. The reduction of $T_{\rm BD}$ and the lower Weibull slope effect are also consistent with the experimental results in Fig. 3. The higher interface trap density effect of the thinner TiN layer could be well explained by the simulation results.

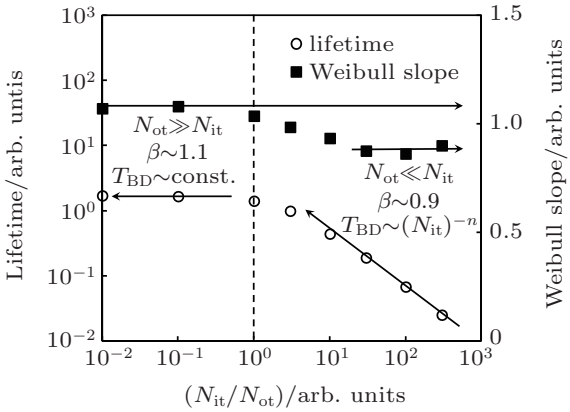


Fig. 8. $T_{\rm BD}$ and β versus $N_{\rm ot}/N_{\rm it}$ of simulation results.

Based on the above simulation results, interface trap influences on TDDB could be explained. As shown in Fig. 8, while increasing $N_{\rm it}$ with a constant $N_{\rm ot}$ ($N_{\rm it}/N_{\rm ot} > 10$), the lifetime reduces and Weibull slope lowers. It is consistent with experimental results in Fig. 3, and the interface trap differences are attributed to Cl diffusion and passivation effects. While in Chen and King's work,[9] oxygen vacancies are more important, however, the Weibull slope lowering from 1.52 to 1.05 could also be explained by the above results due to interface trap increasing. Meanwhile, if considering that $N_{\rm ot}$ decreases due to less oxygen diffusion, the lifetime reduction in Ref. [9] could be explained by both $N_{\rm ot}$ and $N_{\rm it}$ effects.

Thus, the effect of TiN thickness could be explained for both oxygen and Cl diffusion. In this work, the latter effect on interface trap is crucial for the reduction of lifetime and overall lower Weibull slope. While in Chen and King's work,[9] oxygen vacancies are more important. The different determinants for each work may be due to a thinner high-k layer in this work (EOT ~ 0.85 nm in this work and EOT ~ 1.33 nm in Chen and King's work). Thus, from the view of EOT scaling, interface trap degradation is more crucial for reliability concerns.

4. Conclusions

In this paper, the effects of TiN capping layer thickness on trap generation and TDDB characteristic are systemically studied. Samples with two thickness values of ultra-thin TiN

capping layer are tested and have nearly the same electrical characteristics. However, the device with 2.4-nm TiN capping layers shows less SILC increment and longer time to breakdown than those with 1.4-nm TiN. The degradation of $G_{\rm m}$ indicates that the interface trap is related to dielectric degradation, which is proved by charge pumping measurement. Based on SIMS analysis, it is demonstrated that a thicker TiN layer introduces a stronger Cl passivation effect in the ALD TiN deposition process and reduces the interface trap density.

In addition, simulations combined with percolation theory and the kMC method are used to study the detailed relation between TDDB and interface trap density. It is demonstrated that when $N_{\rm it} \gg N_{\rm ot}$, breakdown time decreases fast with $N_{\rm it}$ increasing. Meanwhile, the Weibull slope degrades compared with that under the bulk trap dominant conditions. It is well explained by the simulation results for lifetime reduction and Weibull slope changes due to oxygen and Cl diffusion of the TiN thickness effect. It is also concluded that with EOT scaling, interface trap degradation is more crucial for TDDB assessment.

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