Numerical and experimental study of the mesa configuration in high-voltage 4H–SiC PiN rectifiers*

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The effect of the mesa configuration on the reverse breakdown characteristic of a SiC PiN rectifier for high-voltage applications is analyzed in this study. Three geometrical parameters, i.e., mesa height, mesa angle and mesa bottom corner, are investigated by numerical simulation. The simulation results show that a deep mesa height, a small mesa angle and a smooth mesa bottom (without sub-trench) could contribute to a high breakdown voltage due to a smooth and uniform surface electric field distribution. Moreover, an optimized mesa structure without sub-trench (mesa height of 2.2 μm and mesa angle of 20°) is experimentally demonstrated. A maximum reverse blocking voltage of 4 kV and a forward voltage drop of 3.7 V at 100 A/cm^2 are obtained from the fabricated diode with a 30-μm thick N$^-$ epi-layer, corresponding to 85% of the ideal parallel-plane value. The blocking characteristic as a function of the JTE dose is also discussed for the PiN rectifiers with and without interface charge.

Keywords: silicon carbide, mesa configuration, PiN rectifier, breakdown voltage

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1. Introduction

The silicon carbide based device is a potential candidate to replace silicon in a high-performance power electronic system due to its superior properties like a wide bandgap (3.26 eV), high breakdown field (3 MV/cm), large thermal conductivity (4.9 W/cm·K) and high electron saturation velocity (2×10^7 cm/s).[1] For the advanced power distribution and transmission system application, the 4H–SiC PiN rectifier and IGBT transistor offer much-reduced on-state power losses compared with their unipolar counterparts, owing to the conductivity modulation effect.[2,3] In the literature, a space-modulated junction termination extension,[4] multiple-floating-zone termination extension,[5] etched JTE,[6] and mesa combined with JTEs[7–9] have been investigated for high-voltage SiC PiN devices. Among them, mesa combined with JTE structure is the most widely analyzed and manufactured. The mesa configuration plays a critical role in eliminating the electric field crowding for the SiC PiN rectifier. However, few studies of mesa shape dependence of the reverse blocking characteristic have been performed to date.

The influence of mesa architecture on the reverse blocking characteristic of a power 4H–SiC PiN rectifier is analyzed through two-dimensional (2D) Silvaco-TCAD simulations. Three geometrical parameters are considered, i.e., height, angle, and bottom corner. The improved mesa structure, formed by inductively coupled plasma (ICP), is fabricated for investigating the effect of mesa configuration on the breakdown characteristics of the rectifier. The best achieved breakdown voltage from the rectifier on the 30 μm epi-layers is 4 kV, corresponding to about 85% of the theoretical value. The dependences of JTE dose and SiO_2/SiC interface charge on the reverse blocking voltage are also experimentally discussed.

2. Device structure and optimization

The two-dimensional numerical device characteristics are realized with Atlas from Silvaco. The details of the 4H–SiC material parameters and simulation method are presented elsewhere.[10] In addition to basic models for mobility, carrier generation-recombination, incomplete ionization of impurities and bandgap, an anisotropic impact ionization model is also developed for 4H–SiC material.[11]

Figure 1 shows a schematic diagram of the simulated and fabricated 4H–SiC PiN rectifier with mesa combined with single-zone JTE structure. An N$^+$, 4° off-axis 4H–SiC (0001) substrate, an n-type drift layer (3×10^{15} cm^{-3}, 30 μm), a P$^+$ layer (2×10^{18} cm^{-3}, 1 μm), and a P^{++} contact layer ($>10^{19}$ cm^{-3}, 0.5 μm) are used in this study.

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The most critical aspects when designing a 4H–SiC PiN rectifier are the influences of JTE and mesa shape at the concave corner at mesa sidewall bottom on reverse breakdown voltage value. The sub-trench at the mesa bottom corner is usually observed in SiC mesa etching as shown in Fig. 2. This phenomenon is caused by the deflection of positive ions to bombard the bottom of the sidewall charged by electrons.[12,13]

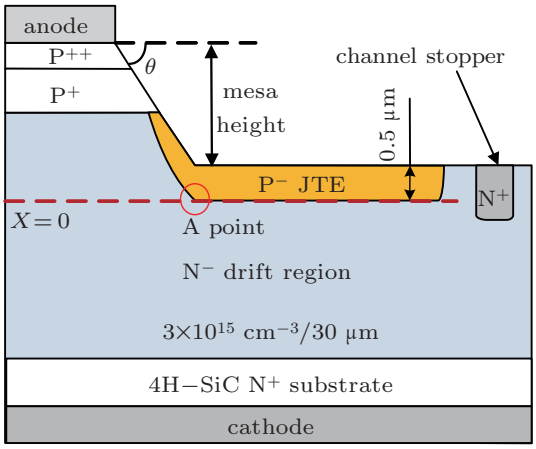


Fig. 1. (color online) Schematic diagram of simulated and fabricated 4H–SiC PiN rectifier.

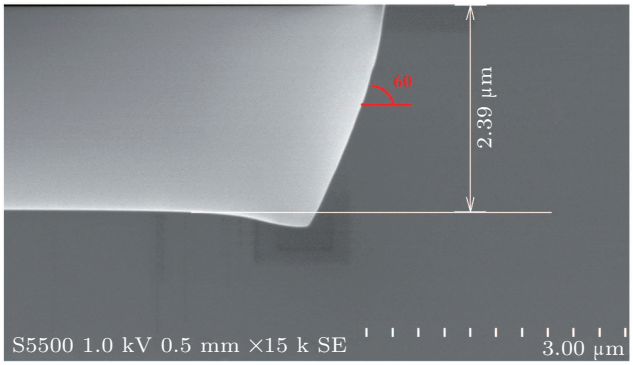


Fig. 2. (color online) SEM picture of 4H–SiC mesa with sub-trench.

Figure 3 shows the comparison between off-state breakdown voltages of a PiN rectifier with and without sub-trench at the concave corner at mesa sidewall bottom. A mesa height of 3 μm and a mesa angle of 60° are used in the simulation. The breakdown voltage is 3.9 kV for the mesa without a sub-trench but decreases from 3.9 kV to 2.8 kV in the mesa with the sub-trench structure. The effects of sub-trench depth (d) on the reverse blocking characteristics are also shown in Fig. 3. The premature breakdown is due to the fact that incomplete depletion occurs in the JTE region near the sub-trench bottom, revealing that the electric field is crowded, and thus enhancing the electric field strength at the main junction as shown in Fig. 4(a). On the other hand, figure 4(b) shows a low peak field combined with moderate edge distribution at the mesa bottom corner could be obtained in the case of the mesa without a sub-trench.

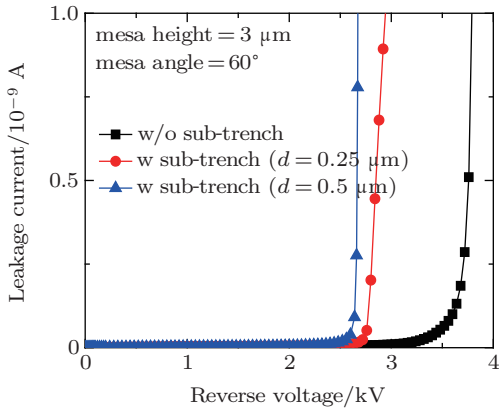


Fig. 3. (color online) Sub-trench depth dependences of reverse blocking characteristic for 4H–SiC PiN rectifiers with and without sub-trench.

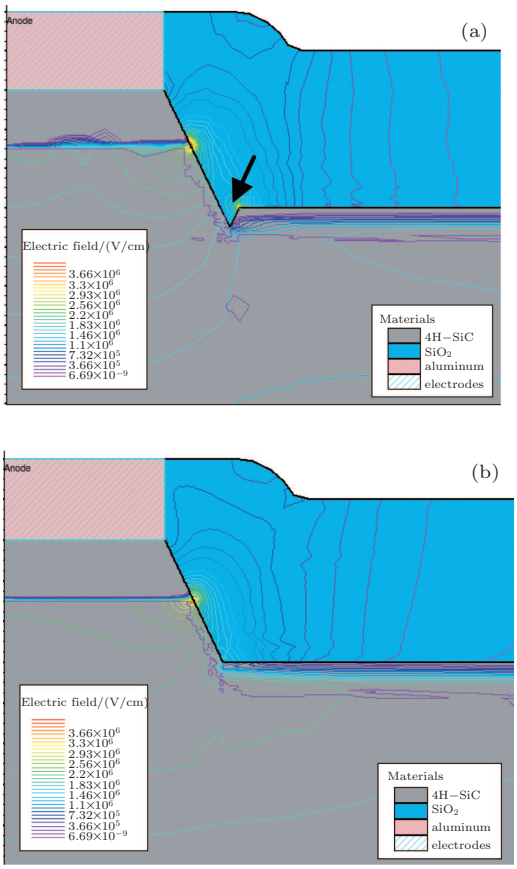


Fig. 4. (color online) Simulated electric field profiles for PiN rectifiers with (a) and without (b) sub-trench at the breakdown (mesa height of 3 μm and mesa angle of 60°).

Figure 5 shows the plots of simulated reverse blocking characteristics versus JTE dose for different mesa heights for 4H–SiC PiN rectifiers without sub-trench. The mesa angle is fixed to be 30°. With the increase of mesa height from 2 μm to 4 μm, the value of blocking voltage is improved from 3.8 kV to 4.2 kV. This is attributed to a decrease in the peak electric field at concave corner at the mesa sidewall bottom (i.e., A point in Fig. 1) as shown in Fig. 6. When the anode coupled

with a high reverse voltage, the depletion region of the diode with a deep mesa could widen further, which reduces the electric field crowding resulting in a higher breakdown voltage.

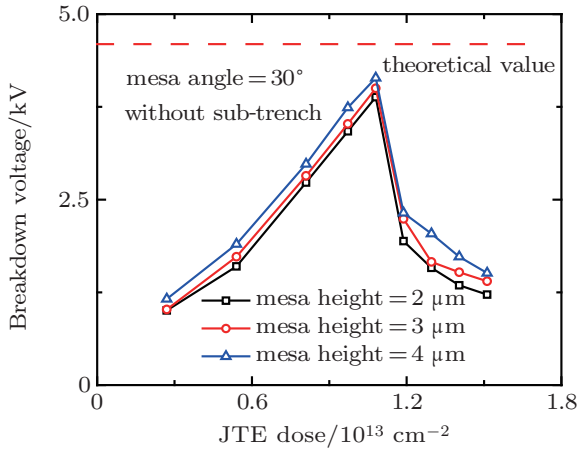


Fig. 5. (color online) Plots of reverse blocking characteristics versus JTE dose for different mesa heights.

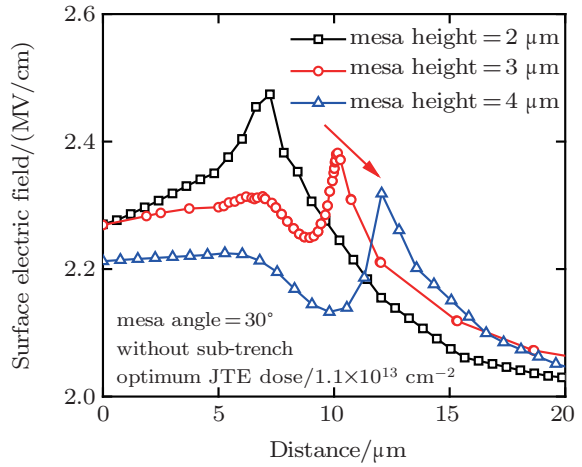


Fig. 6. (color online) Surface electric field distributions through the concave corner at mesa sidewall bottom for 4H–SiC PiN rectifiers.

Figure 7 shows the plots of breakdown voltage versus JIT dose for different mesa angles. The mesa height is fixed to be 3 μm. It can be seen that the behavior of mesa angle is similar to that of mesa height because the electric field strength at the sharp vertex of the mesa bottom is greatly enhanced under a high reverse voltage. The distributions of impact ionization generation rate at breakdown are shown in Fig. 8. The location of peak impact ionization generation rate shifts from the mesa bottom corner to the main junction as mesa angle varies from 60° to 10°. This is attributed to a gradual change of depletion region across the mesa bottom which results in a relatively smooth electric field distribution. In fact, the variation of mesa angle changes the doping profile of the JTE region at the mesa bottom, resulting in the decrease of the electric field near the mesa bottom. However, relatively small changes in JTE concentration will not affect the breakdown voltage.

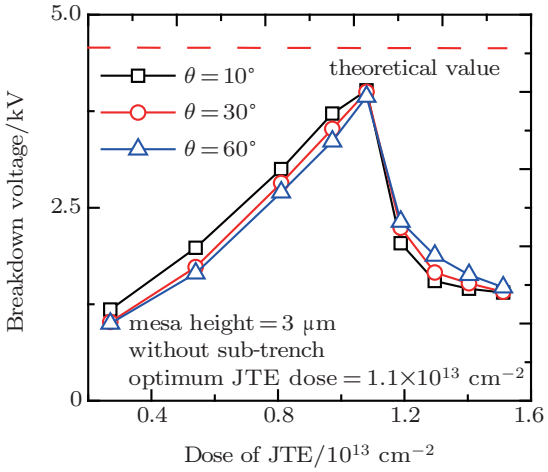


Fig. 7. (color online) Plots of breakdown voltage versus JTE dose for different mesa angles.

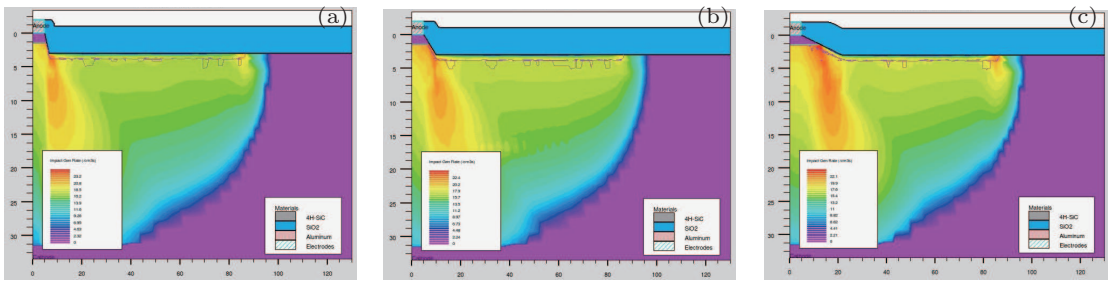


Fig. 8. (color online) Distributions of impact ionization generation rate in SiC PiN rectifiers with mesa angle of (a) 60°, (b) 30°, (c) 10°. The mesa height is fixed to be 3 μm.

3. Experiment and discussion

An optimized mesa configuration for the SiC PiN rectifier with a total chip area of 0.056 mm^2–6.8 mm^2 is experimentally investigated, and the results are shown in Fig. 9. Although a higher breakdown voltage can be achieved for the rectifiers with smaller mesa angles and deeper mesa heights, considering the processing complexity and tolerance, a mesa structure (mesa height = 2.2 μm, mesa angle = 20° and without sub-trench) is formed by ICP etching with CF_4–O_2 chemistry through using SiO_2 as an etching mask. The gas flow rate of CF_4/O_2/Ar is 1:1:1.5. An ICP coil power of 800 W and a bias platen power of 150 W are employed to form the gradual surface. Typically an etch rate of 310 nm/min and selectivity to 1.8:1 are achieved. Aluminum and nitrogen ion implanta-

tion at 500 °C are used to form the single-zone JTE region and channel stopper, respectively. The JTE dose and length are 1.25×10^{13} cm^{-2} and 100 μm respectively. Subsequently, Ti/Al and Ni annealed at 1000 °C for 2 min are employed as ohmic contacts on the anode and cathode. For the passivation, 100-nm-thick oxides thermally grown and annealing in NO at 1300 °C for 0.5 h are employed. Finally, both Si_3N_4 and polyimide layers are deposited as passivation layers.

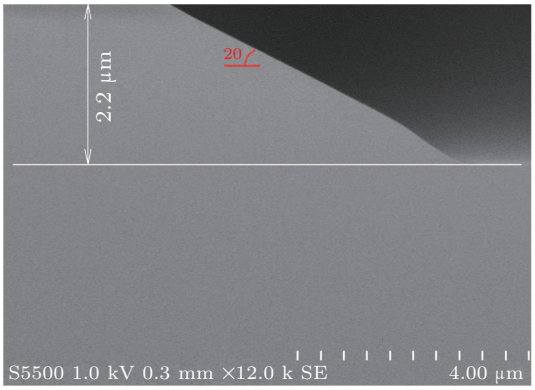


Fig. 9. (color online) SEM picture of 4H–SiC mesa without sub-trench.

Figure 10 shows the typical forward J–V performances of 4H–SiC PiN rectifiers, measured in a temperature range between 25 °C and 155 °C. The specific on-resistance of the PiN rectifier fabricated is 40 mΩ·cm^2 at room temperature. As can be clearly seen in the figure, the forward voltage drop is 3.7 V@100 A/cm^2 at 25 °C, which decreases to 3.5 V at 155 °C. There is an insignificant change (0.2 V) in the whole temperature range for the 4H–SiC PiN rectifiers fabricated.

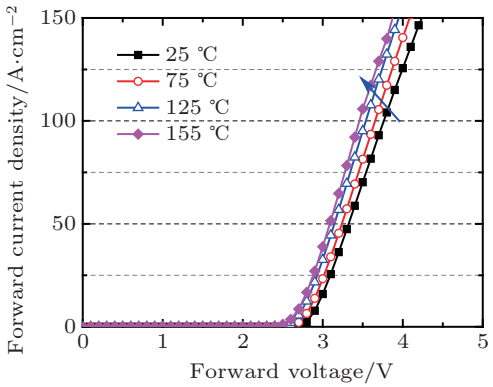


Fig. 10. (color online) Plots of forward current density versus forward voltage of fabricated PiN rectifiers, measured at different temperatures.

The relation between leakage current and reverse voltage is measured by using a Cascade Microtech probe and an Agilent B1505A Power Device Analyzer. The chips are immersed in fluorinert to prevent it from arcing in air condition tests. The breakdown voltage up to 4 kV of 4H–SiC PiN rectifiers with a die size of 6.8 mm^2 at room temperature is shown in Fig. 11, which is close to 85% of the ideal parallel plane breakdown voltage. The leakage current of the 4H–SiC PiN is 1 μA with a current density of 0.01 mA/cm^2 at breakdown. This is due to the fact that the optimized mesa structure without sub-trench alleviates the field-crowding effect at mesa bottom corner.

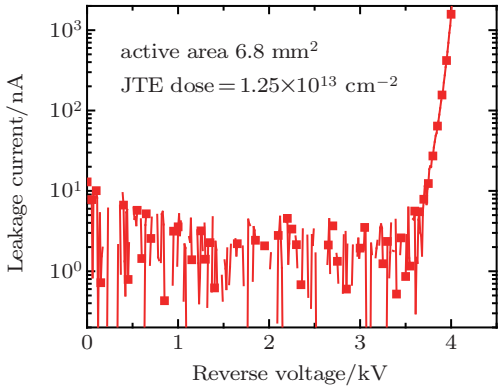


Fig. 11. (color online) Plot of leakage current versus reverse voltage of a 4-kV PiN diode with a die size of 6.8 mm^2.

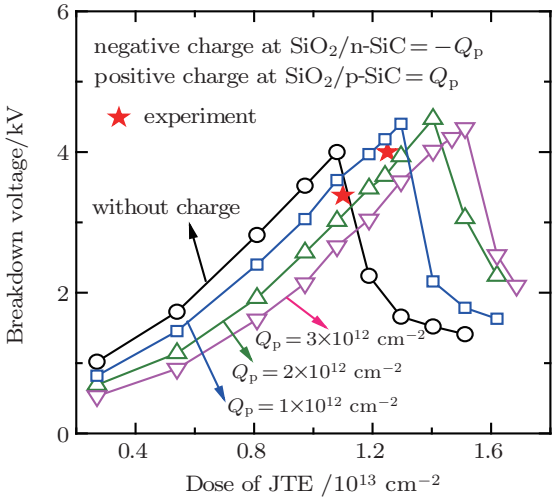


Fig. 12. (color online) Plots of breakdown voltage versus JTE dose for different interface charge densities. Symbols represent experimental results, and solid lines refer to simulation curves.

Surface passivation techniques are widely used in Si and SiC technologies to eliminate surface leakage current and enhance the breakdown of the device. However, there exists negative charge originating from electron trapping at the shallow acceptor-like interface state in SiO_2/n-SiC (epilayer) or positive charge caused by holes trapped at the energetically deep interface states and the fixed oxide charge in the SiO_2/p-SiC (JTE region) interface during the passivation layer formation process,[14–16] which results in a serious influence on the breakdown voltage. Because the interface charge will change by the passivation condition and may vary inside the same wafer, both positive charge and negative charge are simultaneously assumed to be in a range from 1×10^{12} cm^{-2} to 3×10^{12} cm^{-2} in our simulation. Figure 12 demonstrates the reverse blocking capability of the fabricated PiN rectifier with different JTE doses. The difference between simulated and experimental results for the breakdown voltage is dependant on the value of interface charge density. SiC PiN diode with

high interface charge density has a larger shift in the optimization JTE dose. A shift of 2×10^{12} cm^{-2} to 4×10^{12} cm^{-2} for the optimization JTE dose of the PiN rectifier with and without surface trap can be observed. This is due to the fact that negative charges of the ionized acceptors in the JTE region are partly compensated for by the positive charge and the spread of depletion caused by negative charge alleviating electric field crowding. It should be noted that the measured results are in good agreement with the simulated data in the variation trend.

4. Conclusions

This work focuses on three geometrical parameters, i.e., mesa height, mesa angle, and mesa bottom corner for 4H–SiC PiN rectifiers. The influence of mesa configuration on the reverse blocking voltage is numerically simulated and experimentally studied. Results show that a deep mesa height, a small mesa angle and a smooth mesa bottom (without subtrench) could contribute to a high breakdown voltage due to a smooth and uniform surface electric field distribution. By employing an optimized mesa structure, the best achieved breakdown voltage from the diodes on the 30-μm epi-layers is 4 kV, corresponding to about 85% of the theoretical value. In addition, the effect of interface charge on the breakdown voltage is also discussed.

References

[1] Palmour J W 2014 *International Electron Devices Meeting Technical Digest*, December 15–17, 2014, San Francisco, USA, p. 1.1.1

[2] Hu J X, Liu W Y and Yang J F 2015 *International Symposium on Power Semiconductor Devices & IC's*, May 10–14, 2015, Hong Kong, China, p. 7

[3] Fukuda K, Okamoto D, Okamoto M, Deguchi T, *et al.* 2015 *IEEE Trans. Electron Dev.* **62** 396

[4] Feng G, Suda J and Kimoto T 2011 *IEEE Trans. Electron Dev.* **59** 414

[5] Sung W, Brunt E V, Baliga B J and Huang A Q 2011 *IEEE Electron Dev. Lett.* **32** 880

[6] Ghandi R, Buono B, Domeij M, Malm G, Zetterling C M and Östling M 2009 *IEEE Electron Dev. Lett.* **30** 1170

[7] Kaji N, Niwa H, Suda J and Kimoto T 2015 *IEEE Trans. Electron Dev.* **62** 374

[8] Hiyoshi T, Hori T, Suda J and Kimoto T 2008 *IEEE Trans. Electron Dev.* **55** 1841

[9] Niwa H, Feng G, Suda J and Kimoto T 2012 *IEEE Trans. Electron Dev.* **59** 2748

[10] Deng X C, Feng Z, Zhang B, Li Z J, Li L and Pan H S 2009 *Chin. Phys. B* **18** 3018

[11] Hatakeyama T, Nishio J, Ota C and Shinohe T 2005 *IEEE International Conference on Simulation of Semiconductor Processes and Devices*, September 1–3, 2005, Tokyo, Japan, p. 171

[12] Koketsu H, Hatayama T, Amishima K, Yano H and Fuyuki T 2011 *Mater. Sci. Forum* **679–680** 485

[13] Han C, Zhang Y M, Song Q W, Zhang Y M, Tang X Y, Yang F and Niu Y X 2015 *IEEE Trans. Electron Dev.* **62** 1223

[14] Noborio M, Suda and Kimoto T 2009 *IEEE Trans. Electron Dev.* **56** 1953

[15] Kimoto T, Kanzaki Y, Noborio M, Kawano H and Matsunami H 2005 *Jpn. J. Appl. Phys.* **44** 1213

[16] Liu X Y, Wang Y Y, Peng Z Y, Li C Z, Wu J, Bai Y, Tang Y D, Liu K A and Shen H J 2015 *Chin. Phys. B* **24** 087304