Enhanced light extraction of GaN-based light-emitting diodes with periodic textured SiO_2 on Al-doped ZnO transparent conductive layer*

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We report an effective enhancement in light extraction of GaN-based light-emitting diodes (LEDs) with an Al-doped ZnO (AZO) transparent conductive layer by incorporating a top regular textured SiO_2 layer. The 2 inch transparent through-pore anodic aluminum oxide (AAO) membrane was fabricated and used as the etching mask. The periodic pore with a pitch of about 410 nm was successfully transferred to the surface of the SiO_2 layer without any etching damages to the AZO layer and the electrodes. The light output power was enhanced by 19% at 20 mA and 56% at 100 mA compared to that of the planar LEDs without a patterned surface. This approach offers a technique to fabricate a low-cost and large-area regular pattern on the LED chip for achieving enhanced light extraction without an obvious increase of the forward voltage.

Keywords: light-emitting diodes, III–V material, transparent conductive layer, anodic aluminum oxide

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1. Introduction

The development of high-efficiency GaN based light-emitting diodes (LEDs) is one of the most important topics in the area of solid state lighting. However, the severe current crowding under the p-electrode due to the high resistivity of p-GaN is one of the factors that limit the efficiency of the LEDs.[1] To address this, the thin Ni/Au layer[2] and transparent conductive oxides (TCO)[3] have been intensively used as the transparent conductive layer (TCL). In particular, the high-transparent and low resistivity indium tin oxides (ITO)[4] have been widely used as the p- and n-GaN contract layers. Unfortunately, indium is a rare and expensive element, which increases the production cost and is a disadvantage for large-scale commercialization in the future. Many researchers are motivated to find an alternative In-free TCL composed of abundant, inexpensive, and nontoxic elements. In the last decade, ZnO based TCLs including In-doped ZnO (IZO),[5] Al-doped ZnO (AZO),[6] and Ga-doped ZnO (GZO)[7] were reported to exhibit high transparency and low resistivity, and their properties are similar or even prior to those of ITO. For example, our recent study[8] has demonstrated that GaN based LEDs with AZO as TCL exhibit ultralow forward voltage and excellent light extraction.

On the other hand, the light extraction efficiency of a planar GaN based LED is still limited by the total internal reflection (TIR) resulting from the large index difference between GaN and air. The formation of micro- or nano-texture on the surface of the LED including photonic crystals (Phcs)[9–15] or roughening[16,17] is an effective approach to suppress the TIR by coupling the guided modes trapped inside the GaN layers. Various techniques such as electron beam lithography,[9,11] laser holographic lithography,[12] nano-sphere lithography,[13] and anodic aluminum oxide (AAO) templates[14–16] have been adapted to fabricate surface textures on the LED device. The AAO membrane has a self-organized nanostructure in spatially regular and hexagonal order, which is suitable to fabricate large-area two-dimensional periodic patterns with low cost and high throughout. The extraction efficiency of the GaN based LED with doped ZnO as the TCL is expected to be further increased by formatting textures on the surface. However, to the best of our knowledge, the fabrication of visible-scale ordered textures on the surface of the GaN based LED with doped ZnO as the TCL has not been reported. Also, an increased forward voltage is always accompanied with the fabrication of patterns[18,19] due to the etching damages on the current injection and spreading region, which is one of the critical issues that should be addressed for the practical LEDs incorporated with a textured structure.

In this paper, we report the fabrication of a highly ordered texture on the surface of the GaN based LED with AZO as

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the TCL by using the AAO membrane as the etching mask of inductively coupled plasma (ICP). In order to prevent an obvious increase of the forward voltage, the periodic texture is formed on the surface of the SiO_2 layer instead of the TCL or p-GaN layer reported in most of the literature. Fabricating an ordered surface texture using the AAO mask provides a promising mass-production approach for the AZO-TCL GaN-based LEDs with enhanced light extraction efficiency.

2. Experimental details

InGaN/GaN LED structures were grown on patterned sapphire substrates by MOCVD. The epitaxial structure is comprised of 4 μm thick n-GaN, 0.2 μm thick InGaN/GaN MQW active layer, and 0.35 μm thick p-GaN. A 250 nm thick AZO was grown on top of the p-GaN layer by an MD 600A 38×2″ MOCVD system. The 2″ wafer was fabricated into an LED chip with a size of 254 μm×762 μm. Stack layers of Cr/Pd/Au (20 nm/40 nm/200 nm) were deposited as the p- and n-type electrodes. The detail of the parameters of the epitaxial growth and chip fabrication can be found in our pervious report.[8] In the end of the fabrication, a 500 nm thick SiO_2 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) as the passivation layer.

The AAO membrane was fabricated with a 0.3 mm thick aluminum foil (99.99%) by the standard two-step anodization. The Al was anodized in a 4 wt.% phosphoric acid solution at 180 V and 0°. We have developed a fabricating procedure which is crucial for obtaining a large-area AAO membrane with a through-pore structure. Before anodization, the foil was coated by a negative photo resist with a 2″ diameter exposed area for anodization. After the anodization, the photo resist and aluminum on the back side of the anodization window were removed in sequence. Finally, the pore on the back side of the membrane was further enlarged in a phosphoric acid solution.

The procedure of ICP etching has been optimized to obtain a uniform pattern transferred from the AAO mask to the surface of the SiO_2 layer, which is illustrated in Fig. 1. The deposited 500 nm SiO_2 passivation layer was also used to protect the electrodes from being damaged during the dry etching. In order to obtain a uniform pattern transfer, the gap between the mask and the wafer had to be eliminated. Therefore, before etching, the SiO_2 mesa right above the p- and n-electrodes was defined and exposed by a lithography process, and then was etched away by a BOE etchant. The AAO mask was attached on the smooth surface of the wafer and then was etched by $Cl_2/BCl_3/N_2$ gas mixture for 3 min. Finally, the SiO_2 above the p- and n-electrodes was removed using the same process during the etching of the SiO_2 mesa. A quarter of the wafer was fabricated into an LED chip using the above process, while another quarter of the same wafer was fabricated without a patterned surface as the control sample. The light output power of all the LEDs was mapped and recorded. A typical LED chip, which has the statistical average power of its own kind, was selected and used as the study object.

The current–voltage (I–V) characteristic of the LED chip without packaging was measured by an Agilent B1500A semiconductor device analyzer. The light output was characterized by a Fit Tech IPT6000 LED chip/wafer probing and testing system. Electroluminescence and photoluminescence were measured using a Yokogawa AQ6373 optical spectrum analyzer and a Nanometrics RPM BLUE system (405 nm excitation source), respectively.

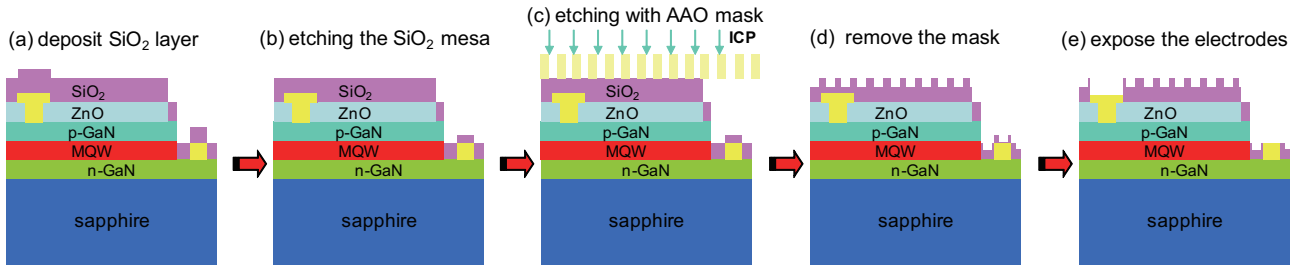


Fig. 1. (color online) Schematic illustration of (a)–(e) the critical steps of pattern transfer using AAO as the ICP etching mask.

3. Results and discussion

Figures 2(a) and 2(b) show the photograph of a typical 2″ diameter AAO membrane and its cross-section SEM image, respectively. The as-prepared AAO membrane is a transparent through-pore thin film with aluminum surrounding, which is very easy to be manipulated in the following etching process and thus is suitable for mass production. The thickness of the membrane used as the etching mask is about 8.1 μm and can be adjusted from about 2 μm to 10 μm by increasing the second anodization time. The back surface of the AAO mask, as shown in Fig. 2(c), consists of hexagonally ordered pore arrays with a pitch of about 410 nm. Figure 3 shows the cross-section and the top view SEM images of the LED chip. The highly ordered pore transferred from the AAO mask is about 140 nm in height. The remaining SiO_2 beneath the ordered

pore is about 360 nm in height, which is thick enough to protect the AZO TCL from etching. The prevention of damage to the surfaces of the electrodes during etching is important since our previous experiments of chip fabrication without the use of the SiO_2 layer during the etching process resulted in an obvious increase of the device's forward voltage. We examine the surfaces of the p- and n-electrodes by SEM and no etching pattern is found. Therefore, the shallow patterned structures are located outside the current injection and spreading region, bringing the least influence to the *I*–*V* characteristic.

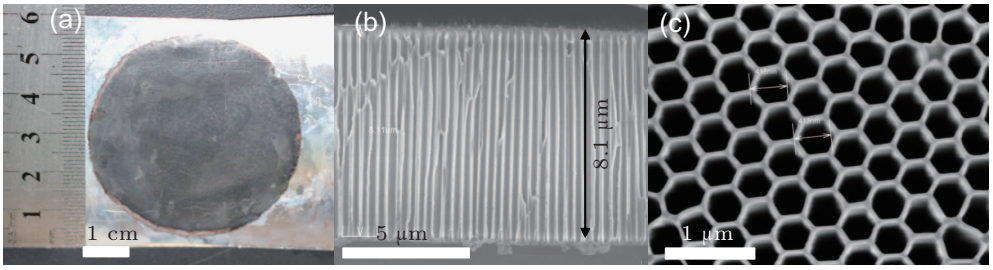


Fig. 2. (color online) (a) Photograph, (b) cross-section SEM image, and (c) top view SEM image of the two-inch diameter transparent through-pore AAO membrane.

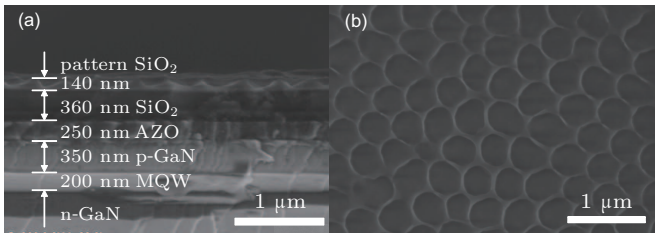


Fig. 3. (a) Cross-section SEM image and (b) top view SEM image of the surface patterned LED chip with AZO-TCL.

Figure 4 shows the results of the voltage–current–light output power (*V*–*I*–*L*) measurement of LEDs with periodic patterned SiO_2 layer (patterned LEDs) compared to those of the conventional planar LEDs (C-LEDs). Compared to that of the C-LEDs, the forward voltage of the patterned LEDs is increased by about 0.05 V at 20 mA and 0.1 V at 100 mA, corresponding to the increased series resistance of 2–3 Ω at 20 mA and 1 Ω at 100 mA. These results are acceptable as they indicate a slight influence on the electrical performance of the patterned LEDs. The increased forward voltage in our experiment is smaller than most of the other reported values for GaN based LEDs with patterned structures.[9,12,18,19] The light output power of the LEDs was measured by integrating the power over the spectrum of the detected light. The light output power of the patterned LEDs is obviously higher than that of the C-LEDs. The light output power of the patterned LEDs is 22.7 mW at 20 mA, which is increased by 18.5% compared to that of the C-LEDs. We also note that the light output power could be as high as 85.1 mW at 100 mA, which is enhanced by 55.7% compared to that of the C-LEDs. The improvement of light extraction is attributed to the diffraction and scattering of the periodic texture, which both benefit the outcoupling of the guided modes above the light line. In addition, the patterned SiO_2 layer introduces a grading refractive index profile between air and the active layer, which also benefits the light extraction. The much larger enhancement of the light output power for the patterned LEDs at larger current might be due to the increased ratio of the emitting surface area to the unemitting one (mainly the area of the electrode). When under a small injection current, light only emits in the adjacent region of the electrode and hence a large amount of light is lost due to the electrode absorption. While, due to the current spread, the effective emitting area is increased with the increase of the current density, resulting in an increased ratio of the emitting area to the unemitting one. Since a larger patterned surface is utilized at a higher current density (as long as it does not reach the *I*–*V* droop), greater light output enhancement is obtained. Our results above suggest that the incorporation of a regular patterned SiO_2 layer on top of the LED chip could achieve enhanced light extraction while causing very slight electrical change.

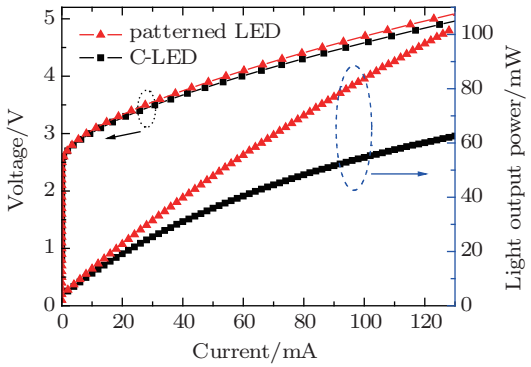


Fig. 4. (color online) The voltage–current–light output power (*V*–*I*–*L*) curves of conventional LEDs and surface patterned LEDs.

Figure 5 shows the photoluminescence (PL) and electroluminescence (EL) spectra of the patterned LED and the C-LED. As shown in the PL spectra, an enhancement of the peak intensity by 45% compared to that of the C-LED is observed,

together with the disappearance of the interference fringes in the spectrum of the patterned LED. The EL peak intensity of the patterned LED at 20 mA is enhanced by about 14% compared to that of the C-LED, as shown in Fig. 5(b). The enhancement of the PL spectrum is much larger than that of the EL spectrum because the PL process is not influenced by the current injection and spreading within the layers. Similar to the EL enhancement, the PL enhancement also greatly depends on the strength of excitation. A small blue shift is observed in the EL spectrum of the patterned LED, which is very likely to be originated from the wavelength fluctuation within the same wafer. The results of PL and EL confirm that an effective light extraction enhancement can be obtained by using the LED chip with top regular textured SiO_2 layer as an optical structure or as a complete device.

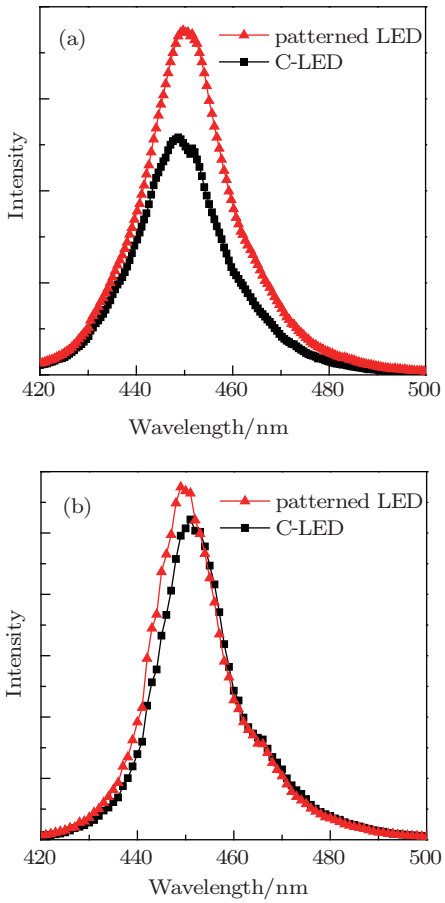


Fig. 5. (color online) (a) Photoluminescence and (b) electroluminescence spectra of the conventional LEDs and the surface patterned LEDs.

4. Conclusion

We demonstrate the low-cost and large-area fabrication of a regular pattern on the top SiO_2 layer of LEDs with AZO as TCL. The 2 inch highly-ordered transparent through-pore anodic aluminum oxide (AAO) membrane was fabricated by the conventional two-step anodization. Using the AAO membrane as the etching mask, the periodic pore structure with a pitch of about 410 nm was successfully transferred to the surface of the SiO_2 layer by ICP dry etching. The SEM image revealed no etching damage to the AZO layer and the electrodes, which is believed to avoid the obvious increase of the device's forward voltage. The light output power was enhanced by 19% at 20 mA and 56% at 100 mA compared to that of the conventional LED without patterned surface. The increase of the forward voltage was only about 0.05 V at 20 mA. Up to 45% enhancement in the PL peak intensity and 14% in the EL peak intensity (at 20 mA) were obtained from the patterned LED structure. The improvement of light extraction is attributed to the diffraction and scattering of the periodic texture, as well as the grading refractive index introduced by the patterned SiO_2 layer.

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