Effect of cryogenic temperature characteristics on 0.18-μm silicon-on-insulator devices*

Bingqing Xie(解冰清), Bo Li(李博), Jinshun Bi(毕津顺), Jianhui Bu(卜建辉), Chi Wu(吴驰), Binhong Li(李彬鸿), Zhengsheng Han(韩郑生), and Jiajun Luo(罗家俊)†

Key Laboratory of Silicon Device and Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, *China*

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The experimental results of the cryogenic temperature characteristics on 0.18-μm silicon-on-insulator (SOI) metal-oxide-silicon (MOS) field-effect-transistors (FETs) were presented in detail. The current and capacitance characteristics for different operating conditions ranging from 300 K to 10 K were discussed. SOI MOSFETs at cryogenic temperature exhibit improved performance, as expected. Nevertheless, operation at cryogenic temperature also demonstrates abnormal behaviors, such as the impurity freeze-out and series resistance effects. In this paper, the critical parameters of the devices were extracted with a specific method from 300 K to 10 K. Accordingly, some temperature-dependent-parameter models were created to improve fitting precision at cryogenic temperature.

Keywords: cryogenic temperature, metal-oxide-semiconductor, silicon-on-insulator, capacitance

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1. Introduction

Nowadays, cryogenic integrated circuits have aroused great interest as a result of the high enthusiasm for Lunar and Martian exploration. However, the reliability of semiconductor devices to cryogenic environment confront more serious issues. The surprisingly extreme temperature of space background as low as 3 K makes the operation of electronics system quite difficult.[1,2] Presently, spacecraft operating in the cryogenic environment of deep space carries on-board radioisotope heating units to maintain a safe operating temperature for the electronic system.[3] This is not an ideal solution since the required active thermal control system increases cost and complexity. Meanwhile, some indispensable sub-systems such as high-sensitivity cooled sensors are required to operate in cryogenic environment. Particularly, sensors in SOI MOS process show an excellent cryogenic performance compared with bulk MOS process.[4] Hence, devices capable of operation at cryogenic temperatures will not only tolerate the unamiable space environment, but also reduce the weight of craft.

The SOI MOS offers several benefits over bulk MOS technology, such as latch-up immunity, especially in the space application due to its excellent radiation hardness.[5–7] The long-recognized advantages of MOS working at cryogenic temperature have encouraged investigators in many fields all over the world since the 1970s.[8] The main advantages of MOS under cryogenic temperature are associated with an increased carrier mobility, better turn-on capabilities, higher saturation velocity, higher thermal and electrical conductivity, lower power consumption, reduced thermal noise, and decrease of junction leakage currents.[9,10] With liquid nitrogen, Jason investigated the characteristic of bulk MOS.[11] With the increasing miniaturization of microelectronic technology, the experimental results for 0.1-μm MOS were reported in 1987 for the first time.[12] Recently, the reliability of 65-nm MOS was investigated in 2015.[13] The research on SOI technology at cryogenic temperature started a little later than on bulk silicon. Young and Elewa reported the advantages of cryogenic operation of SOI MOS as far back as 1990.[14,15] For the use of sub-20-nm CMOS technology, Shin investigated the characterization of advanced FD-SOI MOS at cryogenic temperature.[16] However, some specific problems related to the cryogenic temperature, such as the impurity freeze-out and series resistance effects, make it difficult for some practical applications. So as to solve some problems, a circuit structure featured twin-gate was proved effective at very low temperature.[17] More recently, Sansen obtained an 8-bit analog-to-digital converter working from 4.2 K to 300 K, guaranteeing the reliability of circuits at cryogenic temperature.[18]

Previous work was always concentrated in the area of cryogenic *I*–*V* performance of SOI MOS.[19–21] In this work, the experimental results of cryogenic *I*–*V* and *C*–*V* performance of SOI MOSFETs with a radiation-hard architecture in a 0.18-μm process are presented. Some specific behaviors at cryogenic temperature are analyzed. More specifically, numerical models of several key parameters are described.

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†Corresponding author. E-mail: luojj@ime.ac.cn

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2. Device technology and experimental setup

Due to the excellent performance in radiation hardness, devices with H-gate are generally used in the radiation-hard application.[22] In this paper, the devices are H-gate using 0.18 μm PDSOI process as shown in Fig. 1. The gate-oxide layer is 2.9 nm. Both the silicon-film layer and buried oxide layer are 300 nm.

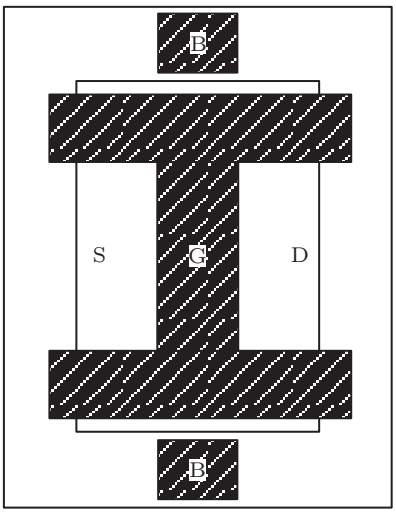


Fig. 1. Structure of H-gate.

To investigate the impact of cryogenic temperature, the gate width and length of the device in our test are both 20 μm to eliminate the effects of a short channel and narrow channel. In order to decrease the effect of noise and gate resistance in *C*–*V* test, a multiple fingers gate is utilized. In *I*–*V* test we investigated MOSFETs with gate length (L) and width (W) both of 20 μm. In *C*–*V* test, the MOSFET of which L and W are 10 μm and 100 μm respectively has 20 fingers. As shown in Fig. 2, a low-temperature probe system which can enable on-chip testing from 300 K to 6 K is used in the experiment. The devices were placed on a copper pallet cooled by liquid helium. The parameters of devices can be measured by the Keithley 4200 semiconductor characterization system.

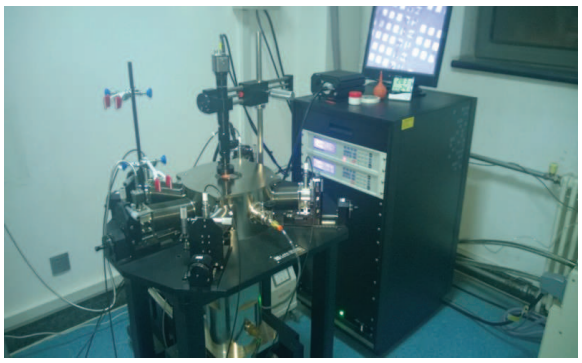


Fig. 2. (color online) Experimental setup for cryogenic measurements.

3. Experiments and results

3.1. *I*–*V* performance

The output characteristics of the NMOSFET (W = 20 μm, L = 20 μm) from room temperature to cryogenic temperature can be seen in Fig. 3(a). We can plot the saturation drain current $I_{\rm Dsat}$ derived from the saturation region, as can be seen in Fig. 3(b), and saturation drain current increases by a factor of approximately 3 when cooled to 10 K. The resistance in linear region $R_{\rm linear}$ varying with temperature can be derived from the linear region as shown in Fig. 3(c). Both $I_{\rm Dsat}$ and $R_{\rm linear}$ curves change sharply within the temperature interval from 300 K to 40 K and are flat below 40 K.

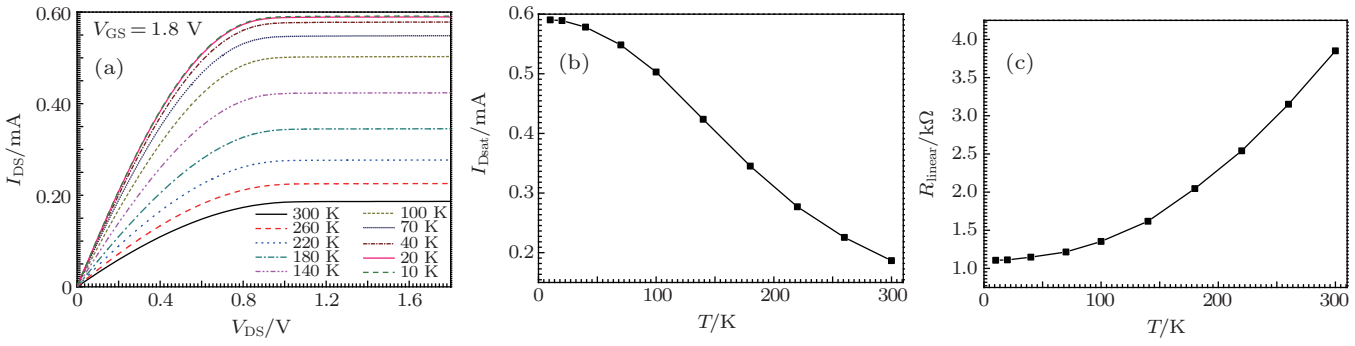


Fig. 3. (color online) (a) Drain current versus $V_{\rm DS}$; (b) saturation drain current versus temperature; (c) linear resistance versus temperature, from 300 K to 10 K.

Figures 4(a) and 4(b) show the transfer curves and transconductance varying with temperature respectively. In Fig. 4(a), we can see that the characteristics have a zero-temperature coefficient (ZTC) point in which the circuits can be stable from room temperature to cryogenic temperature.[23] This point is useful in the design of a high-precision amplifier. In consideration of IC design, transconductance ($g_{\rm m}$) is very important in that it can be used to show the ability of converting voltage (V) to obvious current (I). At the same time, $g_{\rm m}$ is a primary parameter in that it is a design guideline for analog design, and $g_{\rm m}$ can be expressed as

$$g_{\rm m} = \frac{\partial I_{\rm DS}}{\partial V_{\rm GS}}\Big|V_{\rm DS,const}. \quad (1)$$

The maximum of transconductance is about 30 μS at 300 K and the value increases to nearly 180 μS at 10 K, which is induced by the increase of mobility at cryogenic temperature.

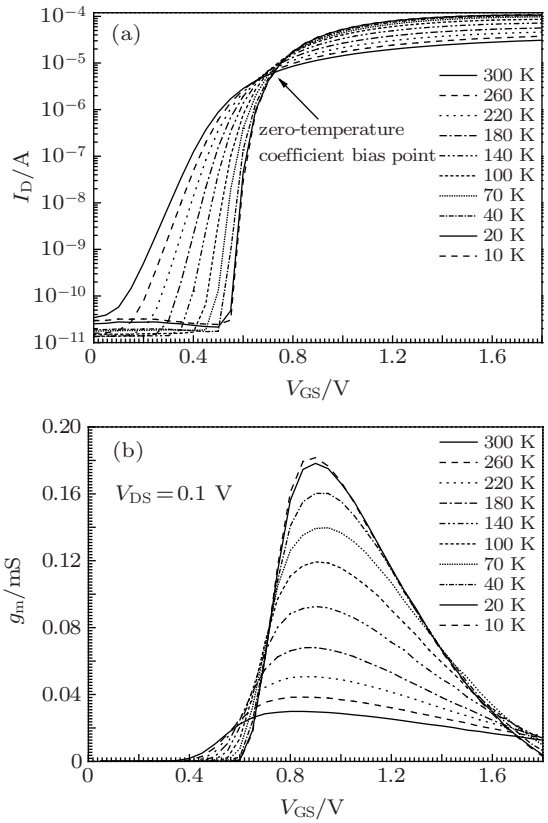


Fig. 4. (a) Drain current versus gate-to-source voltage; (b) transconductance versus gate-to-source, from 300 K to 10 K.

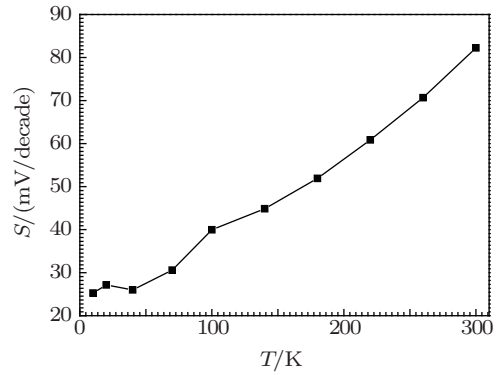


Fig. 5. (color online) Sub-threshold swing versus temperature, from 300 K to 10 K.

The sub-threshold swing S is defined as

$$S \equiv \frac{\partial V_{\rm GS}}{\partial(\log I_{\rm DS})} = \frac{2.3kTn}{q}, \quad (2)$$

where k, T, and q denote Boltzmann's constant, Kelvin temperature, and electron charge, respectively, and n is a factor mainly associated with the capacitance derived from the traps near the interface and gate-to-oxide capacitance $C_{\rm OX}$.[21] Note that in Eq. (2), S is proportional to temperature at certain n ($n \simeq 1.4$ in our test). The sub-threshold swing at 300 K is approximately 70 mV/decade to 110 mV/decade.[19] As shown in Fig. 5 at 10 K, the sub-threshold swing is reduced almost 3.3 times, which means a smaller power supply can be utilized. Meanwhile when temperature is below nearby 40 K, S is no longer proportional to temperature which may be induced by the factor n derived from change of capacitance in cryogenic environment.

3.2. *C–V* performance

It is very important to maintain the reliability of $C_{\rm OX}$. The *C–V* characteristic is universally used to measure some important parameters such as the thickness of oxide, $V_{\rm th}$, and flat-band voltage. In this paper, characterization analysis of MOS capacitors will be carried out at a high frequency of 1 MHz. The *C–V* test strategy in Keithley 4200 is implemented by applying a small alternating voltage to the MOSFET under test. Q can be derived by integrating the current over time, and C can be calculated from

$$C \equiv \frac{\Delta Q}{\Delta V}. \quad (3)$$

To get the characteristic of gate-to-bulk capacitance $C_{\rm GB}$, the nodes gate and bulk of SOI NMOSFET are connected to the semiconductor characterization system, and the node drain and source are opened. The experimental result of $C_{\rm GB}$ versus temperature is shown in Fig. 6(a). As can be seen, the capacitance varies with temperature in the

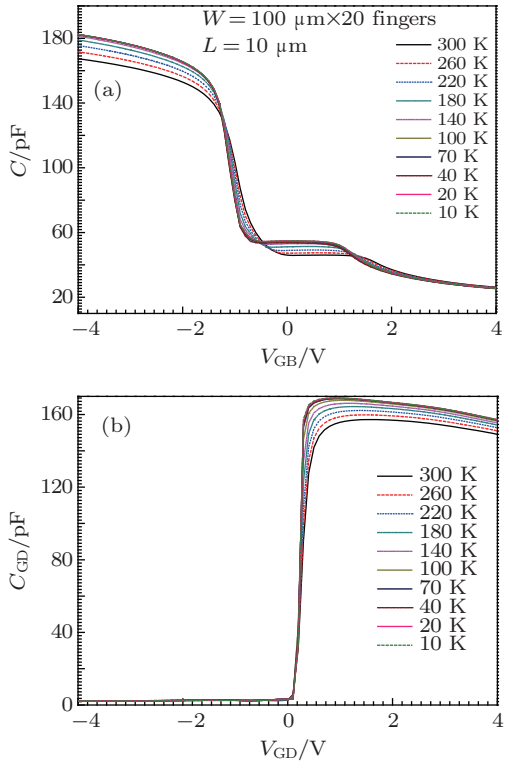


Fig. 6. (color online) (a) $C_{\rm GB}$–V; (b) $C_{\rm GD}$–V versus temperature (from 300 K to 10 K).

accumulation region that C_{GB} increases with decreasing temperature. The characteristics of oxide layer SiO_2 are considered as almost invariable with temperature. C_{GB} here cannot be recognized as C_{OX} due to the influence of series resistance. The capacitance C_{GD} and C_{GB} were also tested, and the result shows that C_{GS} is equal to C_{GD} due to the symmetrical architecture in our devices. Figure 6(b) illustrates the characteristics of C_{GD}–V_{GD} varying with temperature.

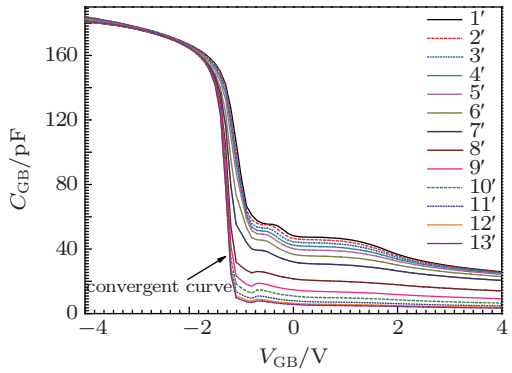


Fig. 7. (color online) Drifting of C_{GB} curve (NMOSFET) in cryogenic temperature.

Starting from about 20 K, a specific behavior was observed and the C_{GB} curves do not coincide with each other at adjacent measurement cycles and finally converge to a certain curve after some test iterations, and the same phenomenon exists in C_{GB} curve of PMOSFET, as shown in Fig. 7. The phenomenon only occurs when the interval between adjacent measurement cycles is short enough, an explanation is the charging and recharging of traps.[24]

4. Discussion

4.1. Series resistance at cryogenic temperature

The C_{OX} is commonly defined as the capacitance in a strong accumulation region. However, the series resistance R_s is unavoidable in the device of a semiconducting film on a nonconducting substrate. Series resistances in our test mainly arise from the undepleted region between the tunnel and the body tie. To measure series resistance, the simple circuit can be utilized to analyze, as shown in Fig. 8.

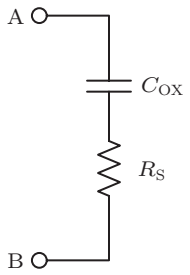


Fig. 8. Simplified model used to determine R_S in accumulation region.

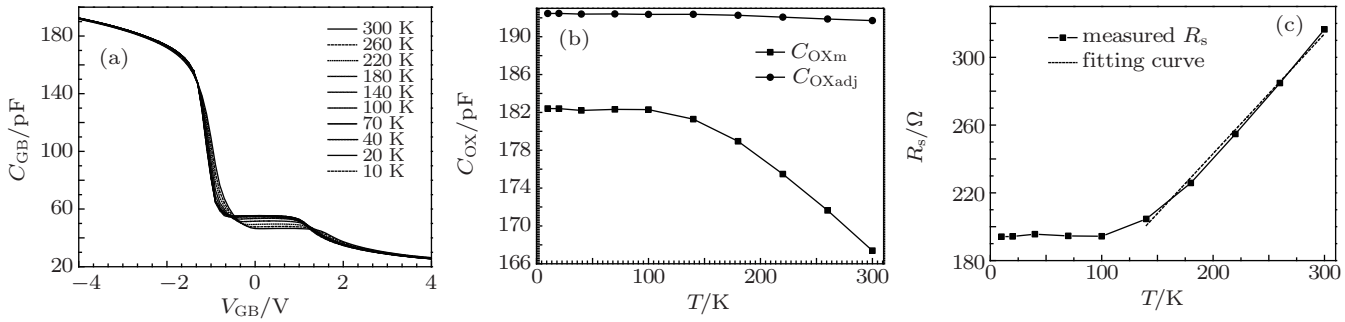


Fig. 9. (a) Corrected *C*–*V* curve versus temperature; (b) measured oxide capacitance C_{OXm} and corrected oxide capacitance C_{OXadj}; (c) calculated series resistance R_s versus temperature, from 300 K to 10 K.

The equal capacitance C_m and conductance G_m can be tested by semiconductor characterization system. The admittance Y_m across terminals A–B (see Fig. 8) in a strong accumulation region can be calculated by[25]

$$Y_m = G_m + j\omega C_m, \tag{4}$$

where j is the unit of imaginary part, and ω is the angular frequency. The series resistance can be derived from Eq. (4) as

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2}. \tag{5}$$

The measured oxide capacitance C_{OXm} is given by

$$C_{OXm} = \frac{C_{OX}}{1 + (\omega R_s C_{OX})^2}. \tag{6}$$

It is shown that C_{OXm} is smaller than the theoretical value of C_{OX} due to R_s. The corrected capacitance C_{adj} and corrected conductance G_{adj} at the frequency of interest are calculated by

$$C_{adj} = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2}, \tag{7}$$

and

$$G_{adj} = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2}, \tag{8}$$

respectively, where $a = G_m - (G_m^2 + \omega^2 C_m^2)R_s$. As shown in Fig. 9(a), C_{adj} has obvious distinctions with measured capacitance. C_{OXm} derived from Fig. 6(a) and corrected oxide capacitance C_{OXadj} derived from Fig. 9(a) are given in Fig. 9(b).

The variation of series resistance with temperature can be seen in Fig. 9(c). The R_s has a huge influence on the measurement of oxide capacitance. C_{OXadj} is nearly constant or increases slightly with temperature, which is understandable for the dielectric constant almost invariant at cryogenic temperature. Because of the increase of effective mobility, R_s is reduced by about 40% as temperature decreases from 300 K to 10 K, and that curve is almost flat below 100 K because the surface roughness depresses the increase of mobility. The numerical model of R_s from 300 K to 10 K is

$$R_s = R_{s0} + J_1\left(\frac{T}{T_{nom}} - 1\right), \quad T_{nom} = 300\ \text{K}, \tag{9}$$

where R_{s0} is the series resistance at 300 K and J_1 is the corrected constant.

4.2. Flatband voltage influenced by freeze-out effect at cryogenic temperature

Flatband voltage represents an important parameter that can be derived from flatband capacitance C_{FB}. As is well known, C_{FB} is calculated as[11]

$$C_{FB} = \frac{1}{1/C_{OX} + L_D/A\varepsilon_{si}}, \tag{10}$$

where A is the gate area, ε_{si} is the permittivity of silicon substrate, and L_D is the extrinsic Debye length defined as

$$L_D = \sqrt{\frac{\varepsilon_{si}kT}{q^2N_A}}. \tag{11}$$

However, equation (10) is under the hypothesis that impurity has been completely ionized, which means the doping N_A is assumed constant. It is not compatible with the cryogenic operation due to freeze-out effect. The C_{FB} at cryogenic temperature can be given by[27]

$$C_{FB} = \sqrt{q\varepsilon_{si}\left|\frac{d\rho_s}{d\psi}\right|_{\psi_s=\psi_b}}, \tag{12}$$

where ρ_s is the charge density at surface, ψ_s and ψ_b are Fermi energies at surface and band, respectively. Considering

$$\rho_s = q(p - n - N_A^- + N_D^+), \tag{13}$$

where n and p respectively denote concentrations of electrons and holes, N_A^- and N_D^+ ($N_D^+ = 0$ in NMOS) denote the concentration of ionized acceptor and donor, respectively.[28]

$$p = N_v\frac{2}{\sqrt{\pi}}F_{1/2}\left(\frac{E_v - E_{Fp}}{kT}\right), \tag{14}$$

$$n = N_c\frac{2}{\sqrt{\pi}}F_{1/2}\left(\frac{E_{Fn} - E_c}{kT}\right), \tag{15}$$

$$N_A^- = N_A\Big/\left[1 + g_a\exp\left(\frac{E_A - E_{Fp}}{kT}\right)\right]^{-1}, \tag{16}$$

$$N_D^- = N_D\Big/\left[1 + g_d\exp\left(\frac{E_{Fn} - E_D}{kT}\right)\right]^{-1}, \tag{17}$$

where E_c and E_v, respectively, denote the conduction and valence band, N_c and N_v are the corresponding effective density of states, g_d and g_a denote degeneracy factors of donors and acceptors, and $F_{1/2}$ denotes Fermi–Dirac operator of one-half order. The relation between various terms of Eqs. (14)–(17) may be determined by

$$E_{Fp} - E_v = \frac{Eg}{2} + \frac{3kT}{4}\ln\frac{m_p}{m_n} - \frac{kT}{q}\ln\frac{N_A}{n_i}, \tag{18}$$

$$E_A - E_{Fp} = \Delta E_A - \frac{Eg}{2} - \frac{3kT}{4}\ln\frac{m_p}{m_n} + \frac{kT}{q}\ln\frac{N_A}{n_i}, \tag{19}$$

and

$$m_n = 1.045 + 4.500\times10^{-4}T, \tag{20}$$

$$m_p = 0.523 + 1.400\times10^{-3}T - 1.480\times10^{-6}T^2, \tag{21}$$

$$E_G = 1.170 + 1.059\times10^{-6}T - 6.050\times10^{-7}T^2, \quad \text{for} \quad T \le 170\ \text{K}, \tag{22}$$

$$E_G = 1.1785 + 9.025\times10^{-5}T - 3.050\times10^{-7}T^2, \quad \text{for} \quad T > 170\ \text{K}, \tag{23}$$

where m_p and m_n is the effective mass of hole and electron, respectively, E_G denotes temperature-dependent energy gap, and ΔE_A denotes ionization energies of the impurities.[29]

The Fermi–Dirac statistics is necessary for N_A^- at cryogenic temperature, because the Fermi level E_F is higher than the acceptor level E_A when temperature is under 70 K in our calculation. As shown in Fig. 10, the concentration of ionized acceptor decreases obviously when temperature is below 70 K. However, in p-type semiconductor as Fermi level approaches the valance band, it will still remain several kT (about 6 kT in our calculation) below the top of the valance band, as discussed by Mckelvey.[30] Therefore, the Boltzmann approximation can be utilized to the holes in the valence band. For the sake of completeness, C_{FB} can be derived as

$$C_{FB} = \sqrt{(q^2\varepsilon/kT)\left(N_v\frac{2}{\sqrt{\pi}}F_{-1/2}\left(\frac{E_v - E_{Fp}}{kT}\right)\right) + N_c\frac{2}{\sqrt{\pi}}F_{-1/2}\left(\frac{E_{Fn} - E_F}{kT}\right) + \frac{4N_A\exp\left(\frac{E_A - E_{Fp}}{kT}\right)}{\left[1 + 4\exp\left(\frac{E_A - E_{Fp}}{kT}\right)\right]^2}}. \tag{24}$$

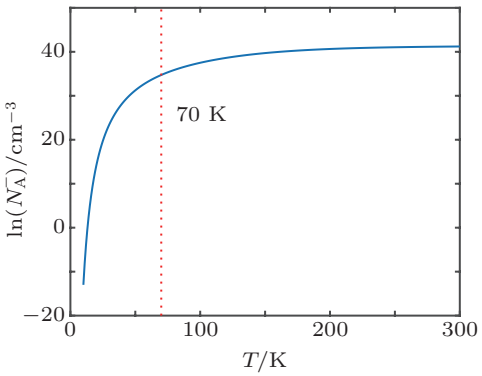


Fig. 10. (color online) Concentration of ionized acceptor versus temperature.

4.3. Threshold voltage at cryogenic temperature

As is well known, $V_{\rm th}$ is defined as the gate voltage when the surface potential $\Psi_{\rm s}$ is equal to $2\Psi_{\rm B}$, where $\Psi_{\rm B}$ is the Fermi potential of bulk. In this paper, threshold voltage is determined from the device turn-on characteristic in the linear region. For NMOSFET, threshold voltage is defined as

$$V_{\rm th} \simeq V_{\rm FB} + 2\Psi_{\rm B} + \frac{\sqrt{4\varepsilon_{\rm si} q N_{\rm A}^- \Psi_{\rm B}}}{C_{\rm OX}}, \tag{25}$$

where $V_{\rm FB}$ is the flatband voltage.[24] The Fermi potential is increased when the temperature decreases. As a result, $V_{\rm th}$ is increased as shown in Fig. 11, and the rise amplitude can be 40% as temperature is reduced from room temperature to 10 K. What should be noticed is that the $V_{\rm th}$ is nearly constant below 70 K. The variation of slope is determined by the carrier freeze-out below freeze-out temperature (nearby 70 K). In the range from 300 K to 70 K, we can get the numerical model of threshold voltage as

$$V_{\rm th} = V_{\rm th0} + K_1\left(\frac{T}{T_{\rm nom}} - 1\right), \quad T_{\rm nom} = 300\ \mathrm{K}, \tag{26}$$

where $V_{\rm th0}$ is the threshold voltage at 300 K, $V_{\rm th}$ is linear as temperature decreases from room temperature to 70 K, and K_1 is corrected constant.

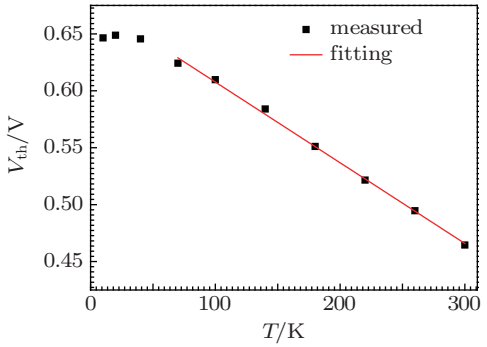


Fig. 11. (color online) Measured threshold voltage and fitting curve, from 300 K to 10 K.

Furthermore in Eq. (26), $V_{\rm FB}$ and $\Psi_{\rm B}$ are affected by temperature. The bulk potential $\Psi_{\rm B}$ can be calculated as

$$\Psi_{\rm B} = \frac{kT}{q}\ln\left(\frac{N_{\rm A}}{n_{\rm i}}\right), \tag{27}$$

where $n_{\rm i}$ is the intrinsic carrier concentration defined as

$$n_{\rm i} = \left[2\frac{(2\pi kT)^{3/2}(m_{\rm p}m_{\rm n})^{3/4})}{h^3}\right]\exp\left(-\frac{E_{\rm g}}{2kT}\right). \tag{28}$$

Using corrected $N_{\rm A}^-$, the $V_{\rm FB}$ suiting for cryogenic temperature is derived from corrected capacitance (Fig. 9(a)). However, a problem is proposed in solving Eq. (25) numerically. For simplicity, we make use of the assumptions: i) concentration of acceptor is completely ionized from 300 K to 70 K; ii) $N_{\rm A}^-$ at 50 K delegates the concentration of ionized acceptor below 70 K (see Fig. 10). The corrected $V_{\rm th}$ is shown in Fig. 12(b). As a result, the corrected $V_{\rm th}$ confirms the validity of this model.

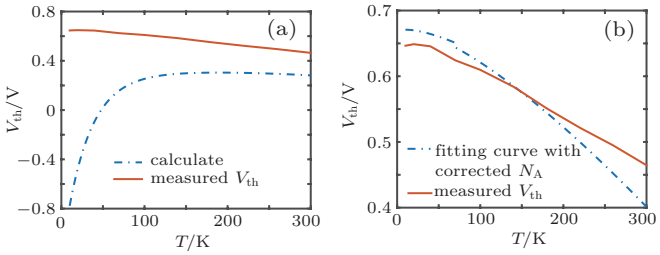


Fig. 12. (color online) Calculated and measured $V_{\rm th}$, from 300 K to 10 K (a) with complete ionization of $N_{\rm A}$; (b) with corrected $N_{\rm A}^-$.

5. Conclusion

The cryogenic characteristics of H-gate SOI MOS fabricated with 0.18-μm PDSOI process are presented in this paper. Both of the important I–V and C–V parameter variations with temperature from 300 K to 10 K are discussed. We observe an obvious decrease in sub-threshold swing S and increase in transconductance $G_{\rm m}$ at cryogenic temperature. As temperature decreases, the decrease of series resistance exerts a huge impact on the test of oxide capacitance due to higher effective carrier mobility.

The freeze-out effect should be considered at cryogenic temperature, because it can reduce the concentration of ionized impurities which have a big influence on electrical parameters. For example, it can induce the Fermi-energy drift and narrow the energy gap, thus increasing the magnitude of flatband voltage and further increasing threshold voltage $V_{\rm th}$. As a result, the current of MOS will be changed.

Furthermore, the comparison of different structures (traditional straight-gate and H-gate) will be done in later work. The significant I–V and C–V performance of SOI MOSFETs at cryogenic temperature provides an immense potential in the deep space application.

Acknowledgment

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