Depositing aluminum as sacrificial metal to reduce metal–graphene contact resistance*

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(Received 11 December 2015; revised manuscript received 15 March 2016; published online 27 May 2016)

Reducing the contact resistance without degrading the mobility property is crucial to achieve high-performance graphene field effect transistors. Also, the idea of modifying the graphene surface by etching away the deposited metal provides a new angle to achieve this goal. We exploit this idea by providing a new process method which reduces the contact resistance from 597 $\Omega\cdot\mu$m to sub 200 $\Omega\cdot\mu$m while no degradation of mobility is observed in the devices. This simple process method avoids the drawbacks of uncontrollability, ineffectiveness, and trade-off with mobility which often exist in the previously proposed methods.

Keywords: graphene, field effect transistor, contact resistance

PACS: 81.05.ue, 73.22.Pr, 73.40.–c, 72.80.Vp **DOI:** 10.1088/1674-1056/25/7/078103

1. Introduction

Graphene, a single layer of carbon atoms, with a honeycomb structure, has attracted wide attention among scientists since 2004 due to its unique properties. Its application covers a wide range of areas, including energy storage,[1] flexible touch screen,[2] radio frequency (RF) devices,[3] supercapacitors,[4] and biosensors.[5] Owing to graphene's extremely high electron mobility, the graphene field effect transistor (GFET) has been proposed as a candidate electronic device in the post silicon era.[6] However, due to the lack of bandgap in graphene, the GFET cannot be turned off completely. Hence, much attention has recently shifted to the use of graphene in RF transistors, where the OFF-current is less critical than that in a digital circuit. One of the figures of merit of GFET in RF domain is the cutoff frequency ($f_{\rm T}$) and the previous studies have shown that the cutoff frequency can be significantly improved by reducing the contact resistance.[7–11] Hence, various teams have introduced different methods to reduce the contact resistance. Low power O_2 plasma treatment[12] and UV/ozone treatment[13] are employed to eliminate the residues at the contact area and create a certain degree of defects on graphene for a better contact. But the demanding control of the experimental conditions limits its popularity and validity since an overtime treatment might increase the contact resistance instead of improving it and the treatment time and conditions could vary from lab to lab. Annealing in vacuum or H_2/Ar atmosphere above 300 °C can also eliminate the resist residues on graphene[14] but with a drawback of deteriorating the properties of graphene in the channel by inducing increased coupling between graphene and the substrate.[14–16] Other methods like the current annealing,[17] electrostatic force cleaning,[18] and mechanical force cleaning via atomic force microscopy (AFM)[19] are all unsuitable for large scale fabrication. Using a metal as a protective layer is another alternative to prevent the contamination of residues, but the results are not good enough with the contact resistance ranging 200–500 $\Omega\cdot\mu$m[7] and 500 $\Omega\cdot\mu$m,[20] and the protective metal deposited on the channel can create defects in graphene during the metal etching process.[21] Using nickel-catalyzed etching[22] to form edge contacts and H-plasma anisotropic etching to form multilayer contacts[23] are methods both aimed at treating the contact area and the channel differently. But these works focused on the exfoliated sample, and samples from chemical vapor deposition (CVD) method need further investigation. So herein, we provide a simple method to reduce the contact resistance by depositing a thin layer of aluminum (5 nm) on the contact area after development and etching it away while keeping the graphene in the channel intact. Aluminum is rapidly etched in an alkaline solution, which contains tetramethylammonium hydroxide (TMAH). The fast etching process functions as a cleaning process and modifies the surface of graphene by alleviating the doping from the photoresist in the contact area. After this treatment, we deposit the final contact metal Pd/Au followed by a lift-off process. Palladium is chosen as the contact metal due to its good wettability[24] on graphene. Due to the protection of photoresist on the graphene channel, the trade-off between decreasing the contact resistance and deteriorating the property of the GFET such as mobility on the channel will not happen compared to the other methods.

*Project by the National Science and Technology Major Project, China (Grant No. 2011ZX02707.3), the National Natural Science Foundation of China (Grant No. 61136005), the Chinese Academy of Sciences (Grant No. KGZD-EW-303), and the Project of Beijing Municipal Science and Technology Commission, China (Grant No. Z151100003515003).

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2. Experiment

The schematic drawing of this method is shown in Fig. 1(a). The graphene film used in this work was grown on a copper foil by the CVD method and then transferred onto a SiO_2/Si substrate by using poly (methyl methacrylate) (PMMA) as a support layer. The thermally grown silicon oxide on the substrate has a thickness of 100 nm while serving as the dielectric layer of the GFET device. The PMMA was removed by acetone at a temperature of 60 °C after the completion of the transfer process. The channel region was defined by a standard UV-photolithography process and the graphene outside the transfer length measurement (TLM) pattern was etched in an O_2 plasma etching system. After that, the photoresist was removed by 60 °C acetone, rinsed in IPA, and blown dry in N_2, then the device was spin coated with image reversal photoresist Az5214. The contact area was defined after the reversible exposure and development process. In the conventional situation, the contact metal will be deposited onto the contact area followed by a lift-off process, but now, instead of directly depositing the contact metal, a 5-nm thin layer of aluminum was deposited by e-beam evaporation after a hard bake process. The hard bake was performed in order to increase the chemical stability of the pattern in the subsequent etching process. The thickness of 5 nm was chosen because this thickness was sufficient to completely cover the graphene and did not require extra etching time to remove. Then aluminum was etched away in a solution containing TMAH in 1 min without damaging the pattern. After this treatment, we deposited the ultimate contact metal Pd/Au (20 nm/80 nm) by e-beam evaporation followed by the conventional lift-off process.

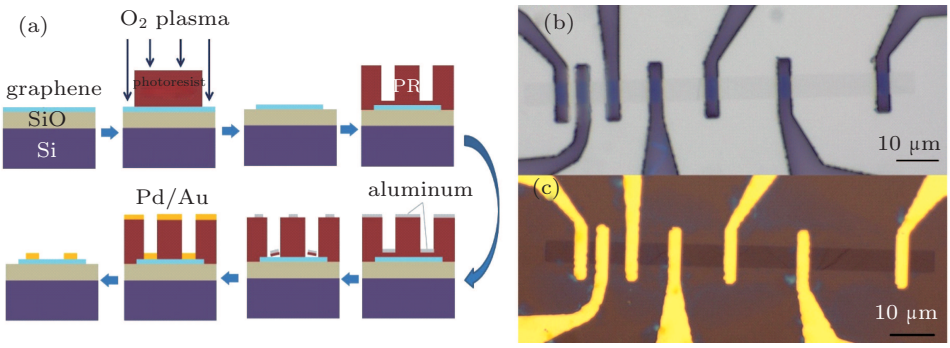


Fig. 1. (color online) (a) Schematic illustration of the fabrication process of graphene FET devices. (b) Optical image after etching the aluminum layer. (c) The TLM structure after depositing the final metal pad.

3. Results and discussion

The optical image after etching the aluminum layer is shown in Fig. 1(b). After the lift-off process of Pd/Au, the ultimate TLM structure is shown in Fig. 1(c). These images show that the aluminum etching process does not damage the pattern after treating the contact area. The effect of depositing metal and etching it away on graphene could be explained as a cleaning procedure proposed by Joiner *et al.*[25] The aluminum in this procedure behaves like a sticky tape which is similar to the demonstration of Dimiev *et al.*[26] Aluminum is etched quickly in the solution containing TMAH which shows a strong alkaline property.[7,27] Moreover, we think that the treatment might introduce some edge contacts by creating some defects[21] in the contact area, which is helpful to reduce the contact resistance,[28] but this needs further investigation.

To verify the cleaning effect on graphene, Raman spectroscopy was performed before and after the aluminum treatment, the results are shown in Fig. 2. The "before treatment" results are for the graphene sample gone through the whole processing steps without the deposition of aluminum, while the "after treatment" results are for the sample with a 5 nm-thin layer of aluminum deposited on graphene and then etched away. In order to illustrate the effectiveness of the treatment, a Raman mapping of 8×6 points with a step of 1 μm on a graphene strip was also conducted. A comparison of the Raman results before and after the treatment is shown in Fig. 2(a). Before the treatment, the high intensity of the G band and its blue shift to 1594 cm^{-1} are indications of high doping in graphene.[29] After the treatment, the G band position moves back to 1587 cm^{-1} and the G band intensity decreases which is shown as an increase of the intensity ratio (I(2D)/I(G)) from 1.10 to 1.86. The Raman mapping results of the intensity ratio (I(2D)/I(G)) and the statistic results of the G band position are shown in Figs. 2(b)–2(d), respectively, which show a similar trend to the results in Fig. 2(a). From the Raman spectra, we find that the treatment has mitigated the doping of graphene, which could be attributed to the removal of organic residues such as PMMA and other photoresists.[12,13] The removal of the residues could also be verified by the AFM results, which are shown in Fig. 3. A graphene strip of 4 μm width was measured via AFM before and after the treatment. The height of graphene is reduced from nearly 8.86 nm to 2.53 nm after the treatment, indicating a cleaning effect through the treatment, which is consistent with the discussion of the Raman results.

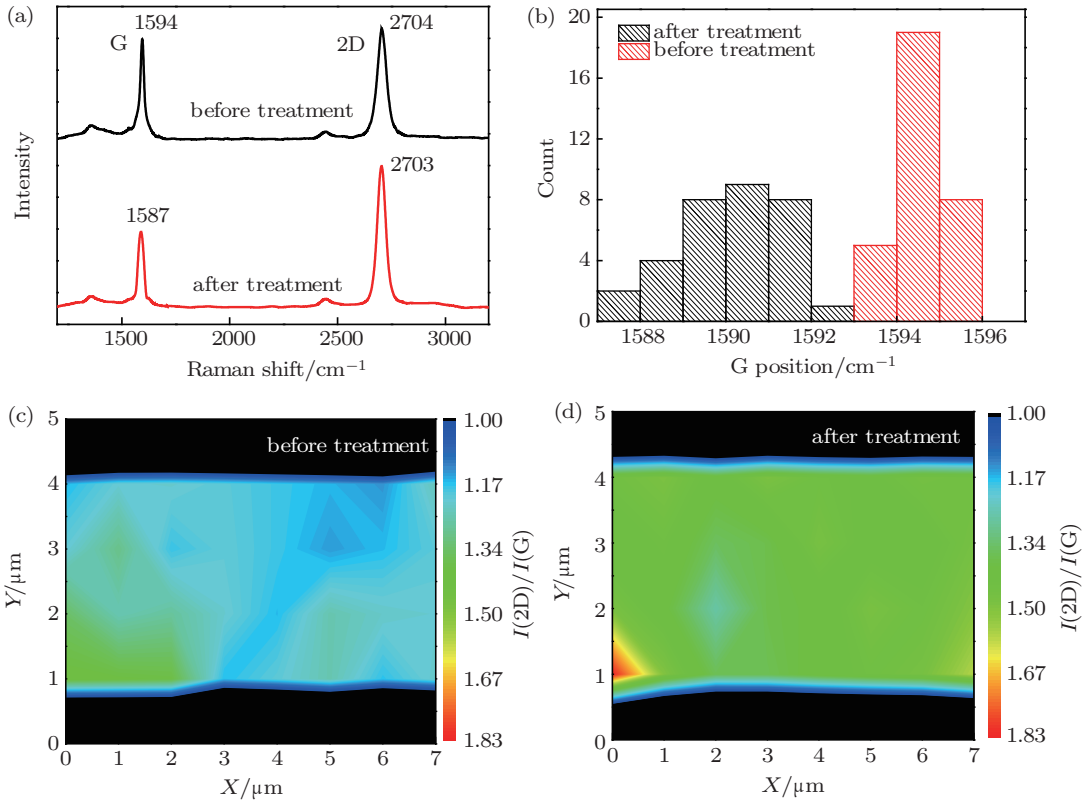


Fig. 2. (color online) (a) The Raman spectra before and after the proposed treatment at the same position. Two distinct bands can be observed, which are designated as G band and 2D band. (b) The histogram of the G band position from the mapping data before and after the treatment. (c), (d) The Raman mapping of the band intensity ratio I(2D)/I(G) before and after the treatment, respectively. The mapping was performed on a graphene strip, where the black area represents the edge outside the graphene.

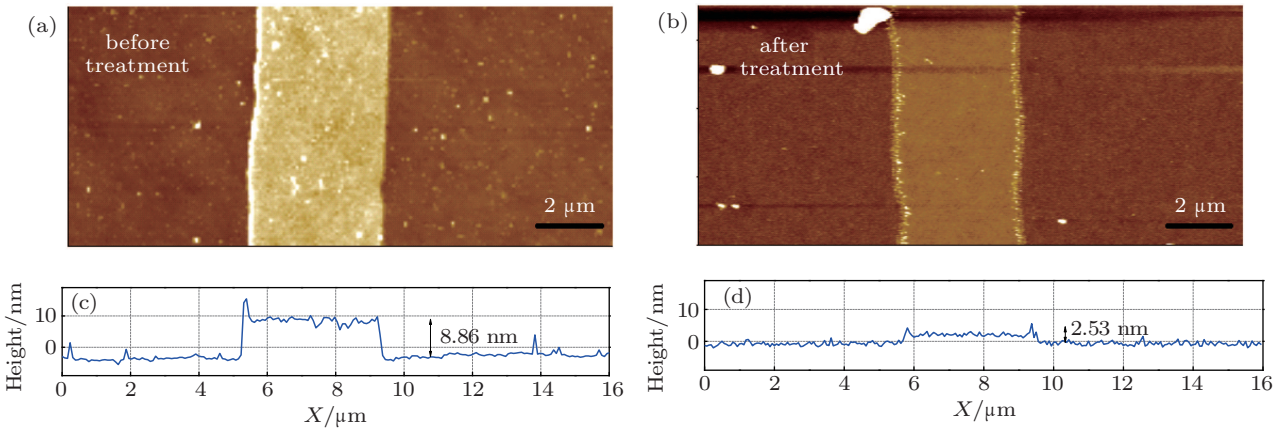


Fig. 3. (color online) (a), (b) AFM topography results before and after the treatment, respectively. (c), (d) Corresponding height profiles of the surface before and after the treatment. AFM was performed on a graphene strip with a width of 4 μm.

Since we focused on reducing the contact resistance, the TLM structure was fabricated to compare the results. In a TLM array, the total resistance between two metal pads consists of three components[20]

$$R_{\mathrm{T}} = 2R_{\mathrm{m}} + 2R_{\mathrm{c}} + R_{\mathrm{gr}}, \tag{1}$$

where R_{m} and R_{c} are the resistances from the contact metal and the metal/graphene interface, and R_{gr} is the intrinsic resistance of graphene which increase linearly with the channel length. The resistance of a single contact would be $R_{\mathrm{m}} + R_{\mathrm{c}}$. However, in most cases, the resistivity of the metal is so low that $R_{\mathrm{c}} \gg R_{\mathrm{m}}$, and R_{m} can often be ignored. So when plotting the relationship between the total resistance and the channel length, the intercept on the resistance axis equals twice the value of the contact resistance. Since different channel width will result in different extracted contact resistance, for the comparison between different research teams, the contact resistivity is used instead. In the TLM structure, the relation between the contact resistivity (ρ_{c}) of the graphene/metal interface and the contact

resistance (R_c) can be written as[13,30]

$$R_c = \rho_c/(WL_T)\coth(L_c/L_T), \tag{2}$$

where L_c and W are the length and width of the electrode contact, and L_T is the transfer length defined by the distance at which the current drops to 1/e from the contact edge. In most cases, L_T ranges between tens and several hundred nanometers,[8,30] and $L_c \gg L_T$, so $R_c \approx \rho_c/(WL_T)$. Also, because L_T is so small, it is more convenient to use $R_c \cdot W$ with the unit of $\Omega \cdot \mu$m to compare the findings.

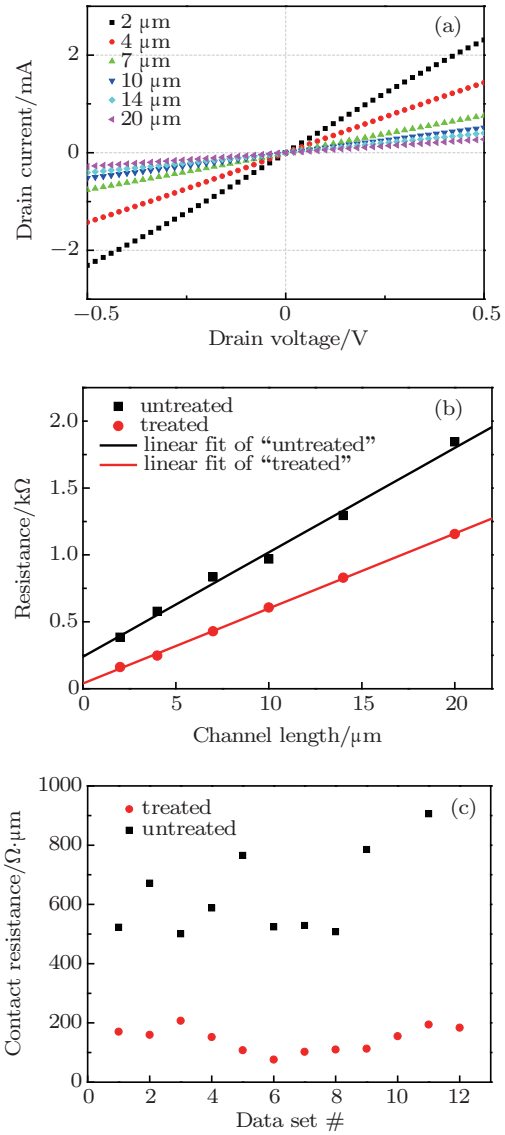


Fig. 4. (color online) (a) Linear *I*–*V* characteristics of different channel lengths. (b) Contact resistance derived using TLM at room temperature. (c) Distributions of the contact resistance for the treated and untreated devices.

We design the TLM structure with the width of 5 μm and the length of $L_1 = 2$ μm, $L_2 = 4$ μm, $L_3 = 7$ μm, $L_4 = 10$ μm, $L_5 = 14$ μm, $L_6 = 20$ μm. The electrode pad length ($L_c = 3$ μm) is much larger than the transfer length. Figure 4(a) shows the dependence of the *I*–*V* curve on the channel length. The *I*–*V* characteristics are linear over a large applied voltage range, indicating that the contacts are ohmic. The total resistance was extracted from the *I*–*V* curve and its dependence on the channel length is shown in Fig. 4(b). The aluminum cleaned set is shown as "treated" while "untreated" represents the set which comes from the same graphene material and has gone through the same fabrication process except for the aluminum treatment procedure. Due to the larger absolute errors in extracting the contacting resistance when the gate bias is around V_{Dirac},[8] which is indicated as the minimum conductance point, we choose to compare the treated and untreated samples at the same back-gate bias of −40 V. According to the data, the graphene devices without the treatment show a larger contact resistance around 597 $\Omega \cdot \mu$m with a larger standard deviation due to the non-uniformly distributed photoresidues. On the other hand, the devices gone through aluminum cleaning have a smaller contact resistance of 98.73 $\Omega \cdot \mu$m and a smaller standard deviation. Several devices were tested and a distribution of sub 200 $\Omega \cdot \mu$m for the treated devices is shown in Fig. 4(c). With the smallest value reaching to 75 $\Omega \cdot \mu$m, the results are better than the previous reported ones.[7,20]

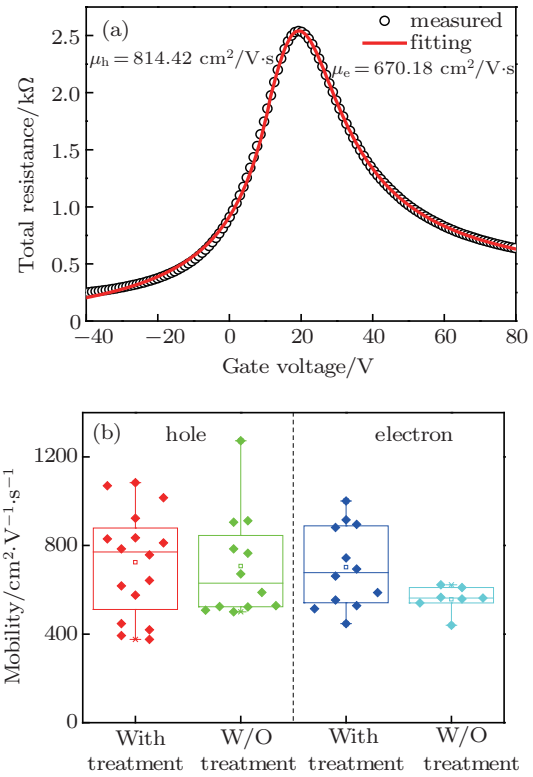


Fig. 5. (color online) (a) Mobility extraction using Kim's model with the measured and fitting data of total resistance versus gate voltage. (b) Distributions of the hole and electron mobilities of the devices with and without the proposed treatment.

We have to mention that this treatment only influences the contact area, and the channel area is protected by photoresist. So compared to the method of depositing an aluminum layer onto the whole graphene surface shown by Allen Hsu *et al.*,[7] this method will not deteriorate the device's other properties such as motility as a trade-off.[7] To extract the mobility of the

graphene devices, the transfer characteristic curve was measured by applying a gate voltage ranging from −40 V to 80 V to the back-gate substrate while applying a drain–source voltage of 5 mV. The R_{tot}–V_g curve shown in Fig. 5(a) was fitted by the model proposed by Kim.[31] The extracted hole mobility is 814.42 $cm^2/V{\cdot}s$ and the extracted electron mobility is 670.18 $cm^2/V{\cdot}s$. Although the fitting is good, there are still some discrepancies on the hole branch, we attribute this to the imprecise value of gate capacitance[32] and the mobility variation near the Dirac point and away from the Dirac point.[32,33] To testify that there is no degradation using this method, we compare the mobility distributions of the treated and untreated samples in Fig. 5(b). The treated and untreated samples both have a mobility in the range of 400–1000 $cm^2/V{\cdot}s$. There is a slight increase for the treated samples and we attribute this enhancement to the decrease of the intrinsic carrier concentration induced by charged impurities.[34] This result meets the expectations: decreasing the contact resistance while preserving the mobility of the channel.

4. Conclusion

We have proposed a method to clean the contact area to reduce the contact resistance without degrading the channel mobility. Raman spectroscopy and AFM were used to show the cleaning effect and the TLM structure was fabricated to extract the contact resistance and we obtained an average value of 125 $\Omega \cdot \mu m$. The extracted mobility through the transfer characteristic measurement showed no degradation of mobility after the process. By depositing a thin aluminum layer and etching it away, this method provides a simple way to improve the contact performance in fabricating the GFET devices.

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