Improving breakdown voltage performance of SOI power device with folded drift region*

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A novel silicon-on-insulator (SOI) high breakdown voltage (BV) power device with interlaced dielectric trenches (IDT) and N/P pillars is proposed. In the studied structure, the drift region is folded by IDT embedded in the active layer, which results in an increase of length of ionization integral remarkably. The crowding phenomenon of electric field in the corner of IDT is relieved by the N/P pillars. Both traits improve two key factors of BV, the ionization integral length and electric field magnitude, and thus BV is significantly enhanced. The electric field in the dielectric layer is enhanced and a major portion of bias is borne by the oxide layer due to the accumulation of inverse charges (holes) at the corner of IDT. The average value of the lateral electric field of the proposed device reaches 60 V/μm with a 10 μm drift length, which increases by 200% in comparison to the conventional SOI LDMOS, resulting in a breakdown voltage of 607 V.

Keywords: interlaced dielectric trenches, folded drift region, breakdown voltage, N/P pillars

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1. Introduction

For the conventional silicon-on-insulator (SOI) high-voltage device, high breakdown voltage (BV) needs a long drift region, which inevitably leads to a high specific on-resistance and a serious manufacture cost of SOI integrated circuit.[1,2] An effective method of increasing BV is to introduce an oxide trench in the drift region,[3–5] and the trench technology has been widely used in the design of the devices.[6,7] The oxide trench in the drift region can decrease the high electric field near the gate and increase length of ionization integral, resulting in a high BV and mini cell pitch.[8–10] However, it is still difficult to obtain the satisfactory result in present oxide trench devices.

In this letter, a novel SOI device with the drift region folded by IDT and N/P pillars parallel to the oxide trenches is proposed to improve the characteristic of BV. The IDT is introduced to fold the drift region and increase the length of ionization integral multiply. The enhancing dielectric layer field (ENDIF) effect is presented by the N/P pillars. A higher vertical BV is obtained by the holes existing at the interface of BOX. Thus, the BV characteristic is improved in this novel structure with little cell pitch.

2. Device structure and operation

The schematic cross-sectional view of the ENDIF IDT LDMOS is shown in Fig. 1(a). An array of N/P pillars in the region I are parallel to the IDT and located in the corner. The N/P pillars have the same length T, the doping concentration of N/P pillars N_{p1}, P_{p1} respectively. In order to optimize the electric field further, an N pillar is introduced in the region II at the corner of the dielectric trench with the length t and doping concentration N_{p2}. N_d, t_d, and L_d are the doping concentration, thickness, and length of the drift region, respectively. H, W, and D are the height, width, and spacing of the IDT, respectively. The thickness of BOX is t_{ox}.

Figure 1(b) shows that the ionized donors and acceptors at the silicon/oxide interface contribute to a rapid rise in electric field strength without affecting the field strength inside the silicon layer. Thus, in order to obtain the high BV, N/P pillars parallel to the oxide trenches are proposed. Moreover, the BV is approximately expressed as Eq. (1), showing that the BV is limited by the lower value between lateral BV and vertical BV. This novel structure improves both lateral BV and vertical BV for the enhancing dielectric layer field, leading to the high BV,

$$\mathrm{BV} = \min\{V_{\mathrm{lat}}, V_{\mathrm{ver}}\}. \quad (1)$$

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In the reverse blocking state, the drift region is folded by IDT and the effective length sustaining the bias is multiplied. The electric field in the drift region is improved by the N/P pillars, thus the blocking behavior is improved.

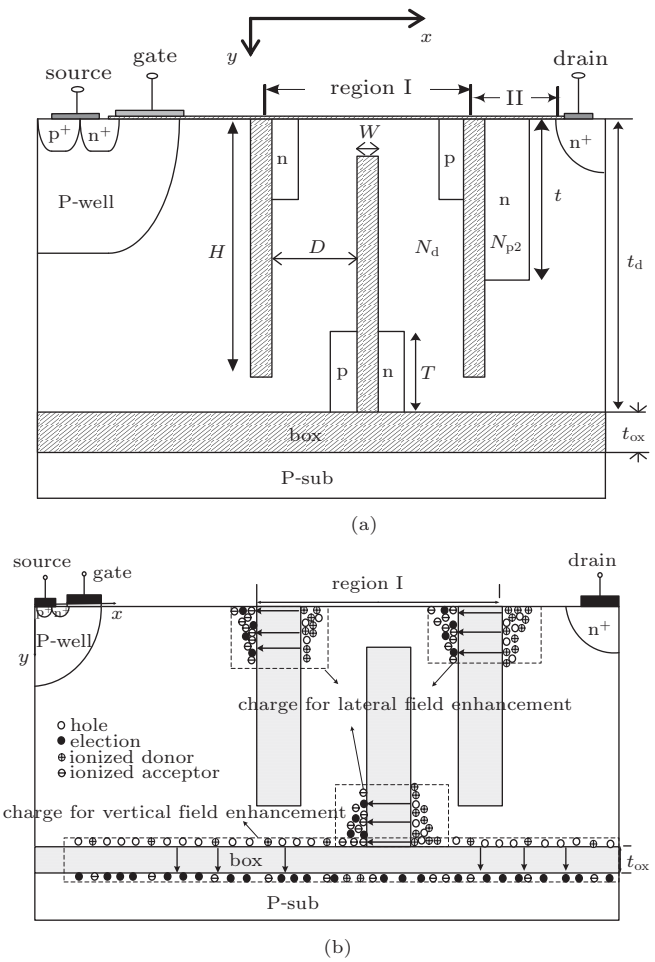


Fig. 1. (a) Schematic cross-section view of the ENDIF IDT LDMOS; (b) schematic of charge distributions.

The interdigital oxide trenches with P/N pillars in the drift region can be fabricated through the following process: trenches etching in silicon wafer → ions implanting (P/N pillars on lower interface) → oxidation → silicon bonding → trenches etching in SOI → ions implanting (P/N pillars on upper interface) → oxidation. When $T = t$, the fabrication cost can be decreased.

3. Results and discussion

The surface electric field and potential distributions of ENDIF IDT LDMOS and IDT LDMOS, conventional LDMOS (C-LDMOS) are compared in Fig. 2(a). There are a number of new electric field peaks in the IDT LDMOS and ENDIF IDT by the dielectric trenches. The average surface lateral electric fields are raised in the drift region compared to C-LDMOS. The electric field in the dielectric trench of ENDIF IDT is increased from 8×10^5 V/cm of the IDT LDMOS to 12.5×10^5 V/cm. The N/P pillars can provide more positive and negative charges, and the electric flux densities of ENDIF IDT are increased. The potentials of three devices are different in the dielectric trench due to the electric field strengthened in the IDT, and the potential in the silicon increases slowly. The potential in the C-LDMOS is linearly and slowly varied in the whole drift region, which causes degradation of breakdown voltage. The 3D electric field distribution of ENDIF IDT LDMOS is shown in Fig. 2(b), the electric field is significantly strengthened because of the electric field modulation effect in the oxide trench, and the electric field of the BOX reaches 3×10^6 V/cm by the holes accumulated at the surface of the BOX.

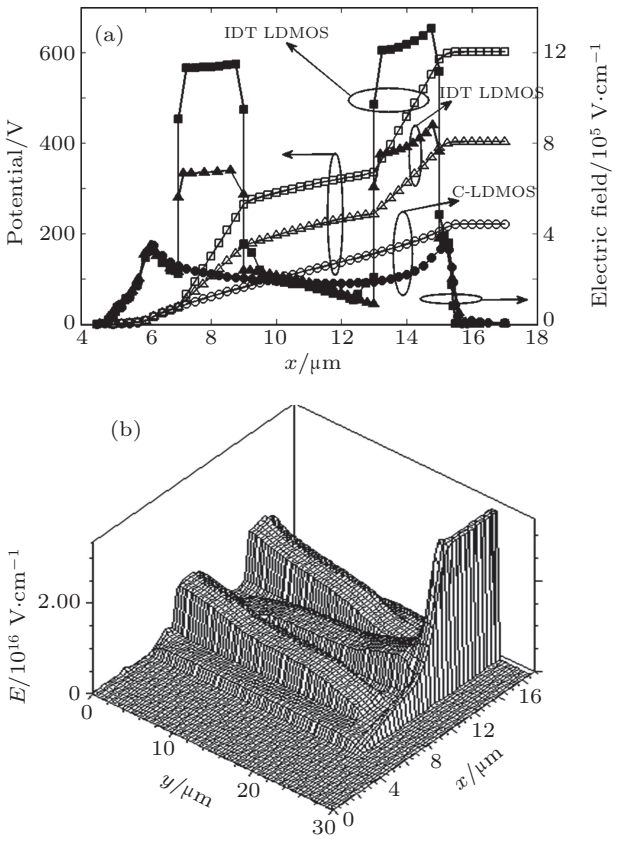


Fig. 2. (a) The surface electric field and potential distribution. (b) 3D electric field distribution of ENDIF IDT LDMOS.

Based on the Gauss theory on the Si/oxide interface, the electric field must satisfy

$$E_{\mathrm{Si}}\varepsilon_{\mathrm{Si}} + Q_{\mathrm{I}} = E_{\mathrm{ox}}\varepsilon_{\mathrm{ox}}, \tag{2}$$

where $\varepsilon_{\mathrm{Si}}$ and E_{Si} are the permittivity and electric field of silicon layer, $\varepsilon_{\mathrm{ox}}$ and E_{ox} are the permittivity and electric field of oxide. Q_{I} is the charge in the interface between silicon and oxide layer. It means that the charges in the surface of oxide Q_{I} can increase E_{ox}.

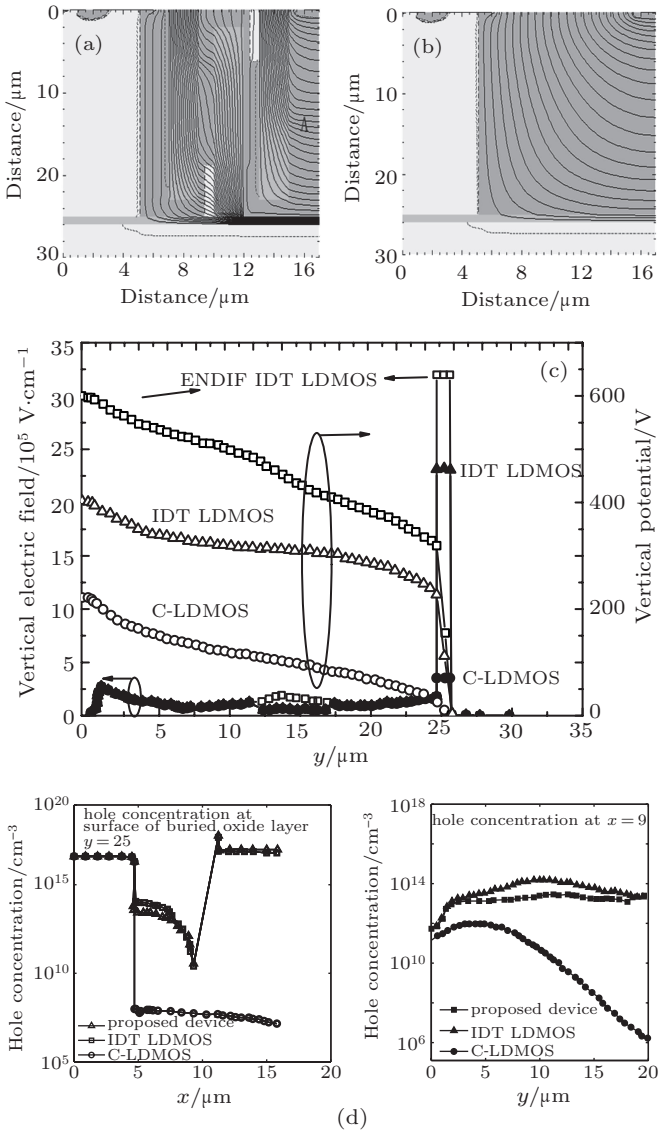


Fig. 3. Equipotential contours at breakdown for (a) ENDIF IDT LDMOS (607 V), (b) C-LDMOS (221 V), (c) the vertical electric field and potential distribution ($x = 16.5$ μm) of the three devices (d) hole profile at surface of BOX layer ($y = 25$ μm) and surface of the oxide trench ($x = 9$ μm).

The equipotential contour in the proposed ENDIF IDT LDMOS is more uniform than that of C-LDMOS in Figs. 3(a) and 3(b). The BV of IDT LDMOS reaches 402 V by the reshaping effect of the electric field compared to 221 V in the C-LDMOS. In addition, the N/P pillars are inserted in the drift region to relieve the intensive electric field in the corner and enhance the electric field distribution in ENDIF IDT and its BV is 607 V. The vertical electric field and potential distribution ($y = 16.5$ μm) of the three devices at breakdown is given in Fig. 3(c). The electric field in the BOX layer of the ENDIF IDT LDMOS is higher than that of the other two devices. More than 325 V of vertical potential is borne by the BOX for the ENDIF IDT LDMOS, while only 236 V for the IDT LDMOS and only 35 V for the C-LDMOS. Figure 3(d) shows the hole density at the surface of BOX layer and surface of the oxide trench ($x = 9$ μm). The inverse charge (hole) densities of ENDIF IDT and the IDT LDMOS are higher than that in C-LDMOS. The holes are collected on the corner of IDT and BOX surface, thus the electric field is increased in the BOX. The electric field is 325 V/μm in the ENDIF IDT, which is much higher than 240 V/μm in the IDT LDMOS and 35 V/μm in the C-LDMOS.

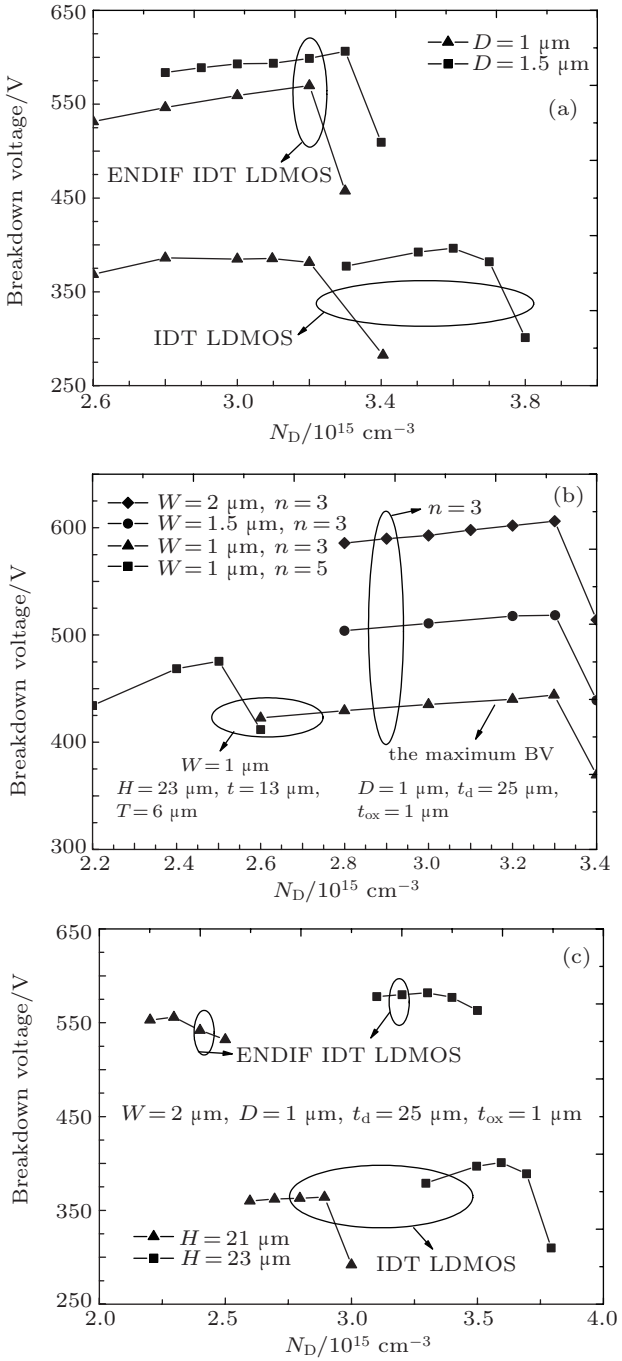


Fig. 4. (a) Dependences of BV on N_d and D; (b) dependences of BV on N_d and W; and (c) dependences of BV on N_d and H.

The maximum BV increases with the decrease of spacing D of the IDT in Fig. 4(a). The denser IDT can strengthen the modulation effect of the electric field, which improves the breakdown characteristics of the ENDIF IDT. The interaction between IDT is strengthened with decrease of D, resulting in

the improvement of electric field. In Fig. 4(b), the BV is augmented with the increase of W of the IDT. The increase of D could expand the area of the oxide layer, which leads to a higher BV. The BV as a function of the H and N_d is shown in Fig. 4(c). With the increase of H, the BV is increased in the optimized condition. The height of the dielectric trenches modulates the length of ionization integral. Therefore, the BV is enhanced by increasing H. It is clear that the BV characteristic of the ENDIF IDT LDMOS is significantly improved compared with that of the IDT LDMOS.

The BV as a function of the N/P pillars' concentrations is shown in Fig. 5(a). The BV of ENDIF IDT LDMOS increases first and then decreases with the increase in the N/P pillars' concentrations. The positive and negative charges on the side of the dielectric trenches could improve the electric field in the oxide layer and Si/oxide interface. Figure 5(b) shows the influences of T (the length of the pillars in the region II) on the BV with different H, and the BV of the proposed device increases first and then decreases with increasing T. The optimized T decreases with the increase in H.

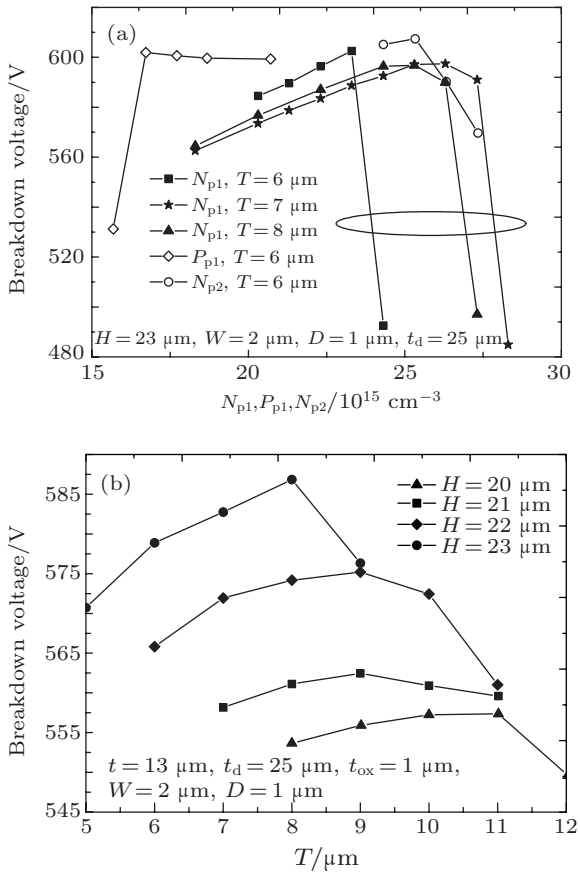


Fig. 5. Variation of BV with (a) the highly doped N/P pillars' concentrations N_{p1}, P_{p1}, and N_{p2}, and (b) the length of the pillars.

The variation of BV with t (length of the N pillar beside the drain) is shown in Fig. 6(a). The optimized t does not change with H. When $T = t$, a trade-off between BV and the cost of fabrication would be met. Figure 6(b) shows the vertical electric field distribution under the drain ($x = 16$ μm) for the three structures, an electric field peak P_A appears at the end of N pillar which had marked the point A in Fig. 3(a). The vertical electric field under the drain of the ENDIF IDT LDMOS is more uniform than that of IDT LDMOS and C-LDMOS.

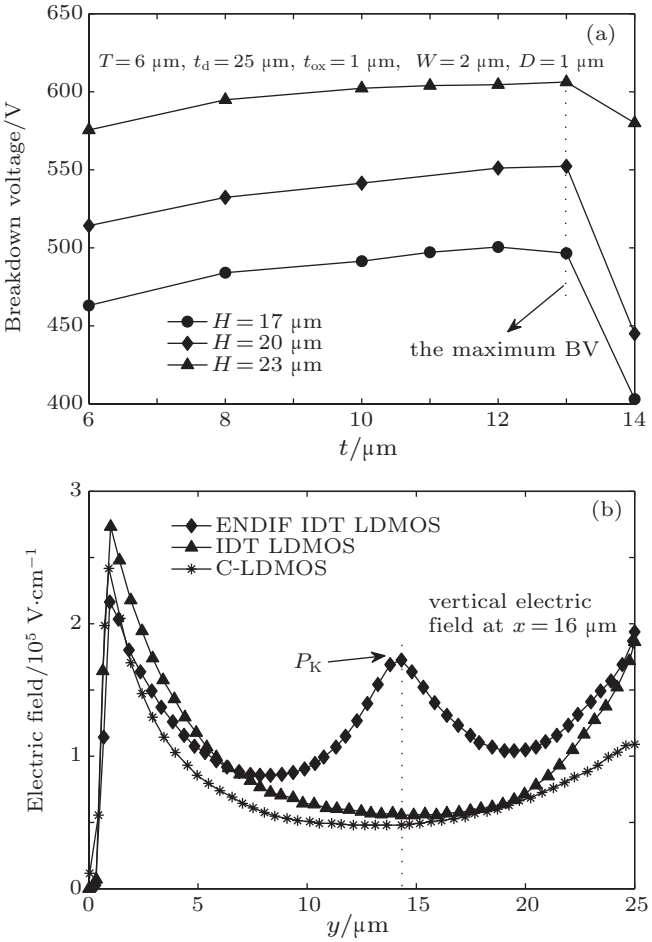


Fig. 6. (a) Variation of BV with t (length of the N pillar beside the drain) and (b) the vertical electric field distribution under the drain ($x = 16$ μm).

Figure 7(a) shows the influences of N_d and t_{ox} on BV. The BV of the ENDIF IDT LDMOS increases first and then decreases with increase t_{ox} and the maximum BV is obtained with $t_{ox} = 1$ μm. The holes are formed at the top interface of the BOX layer and decreases with the increase in t_{ox} for the self-adaption of the BOX layer. The electric fields of the BOX are enhanced with decreasing t_{ox}. Figure 7(b) provides the results of the electric field distributions in the BOX layer ($x = 16$ μm) with different t_{ox}. The electric field of the BOX layer increases from 151 V/μm to 577 V/μm when t_{ox} decreases from 2 μm to 0.5 μm. In Fig. 7(c), the breakdown characteristic of the ENDIF IDT LDMOS is strengthened with the increase in t_d. In general, the thicker the epitaxial layer is, the higher BV will be. The length of ionization integral increases with the increase in the thickness of epitaxial layer due to the folding effect of the drift region.

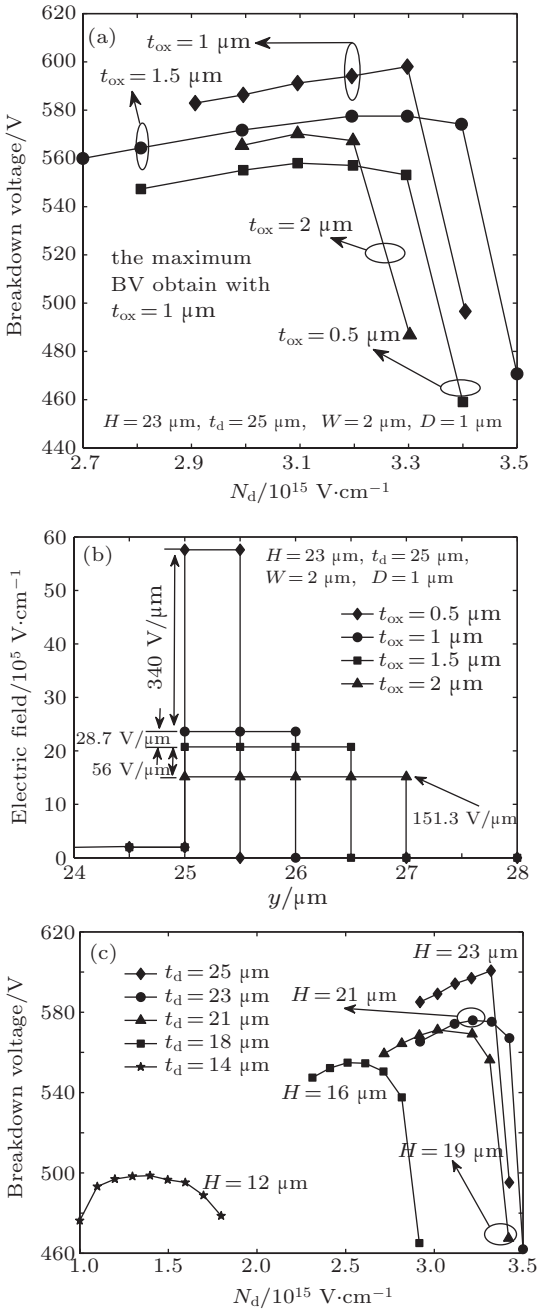


Fig. 7. (a) Variation of BV versus t_{ox}; (b) electric fields of the BOX layer ($x=16$ μm) at breakdown with different t_{ox}; (c) variation of breakdown voltage versus t_d.

Table 1 compares the blocking performances between proposed ENDIF IDT LDMOS and other SOI LDMOS with trench-buried oxide layer. The comparative parameter is defined as t_d and L_d. Thinner silicon layer and smaller devices size are the development trend of the semiconductor device. When BV reaches 600 V, the comparative parameter of the proposed LDMOS is less than that of ENBULF LDMOS. The on-resistance of IDT is much higher than that of ENDIF IDT device.

Table 1. Comparison of blocking performances between the proposed ENDIF IDT LDMOS and the other SOI LDMOS with trench-buried oxide layer.

Device	Reference	t_d/μm	L_d/μm	BV/V	$R_{on,sp}$/mΩ·cm^2
SOI NBL TLDMOS	[3]	4	6	166	2.5
ENDIF IDT LDMOS	Present work	25	23	810	212
ENBULF LDMOS	[4]	25	15	684	58
SOI DT LDMOS	[6]	7.5	6.5	233	3.3
IDT LDMOS	[2]	25	23	596	232
C-LDMOS	Present work	25	23	380	93
DENDIF LDMOS	[8]	6	4	107	3.7

With the increase of the width W of the IDT, the on-resistance of the device increases due to the decrease of conductive path area in Fig. 8(a). The on-resistance decreases with the rise of H, because the optimal doping concentration in the drift region is increased, leading to the descent of on-resistance in (see Fig. 8(b)). The breakdown and on-state characteristic of the three structures are shown in Fig. 8(c). Compared with the C-LDMOS, the BV of the ENDIF IDT LDMOS increases from 375 V to 807 V, and the on-resistance increases little. It is clear that the proposed device has acceptable values in both the BV and on-state performances.

Figure 9 illustrates the surface temperature distributions at optimized conditions with the same drain current. It can be seen that the peak temperature of ENDIF IDT LDMOS is located in the interlaced dielectric trenches because of the low thermal conductivity of the buried oxide layer and higher on-resistance. The ENDIF IDT LDMOS on partial SOI substrate

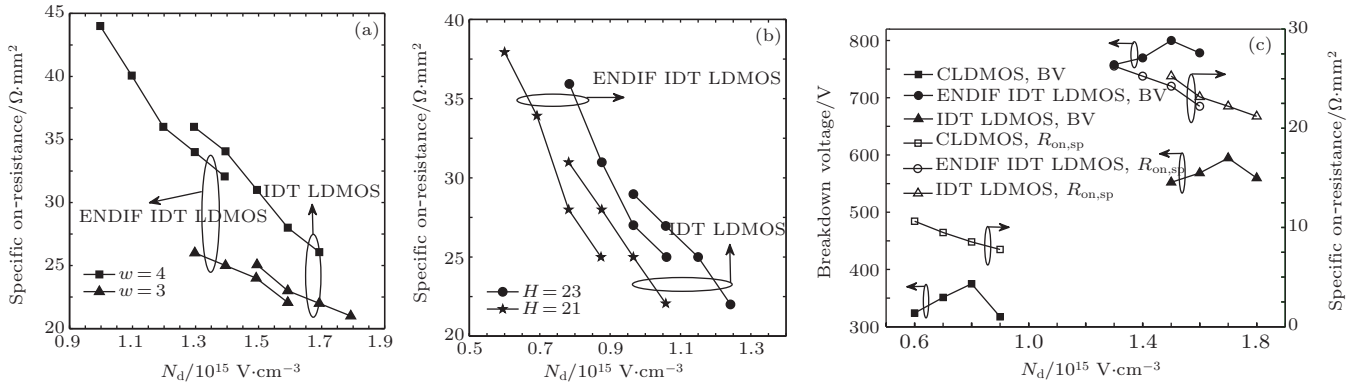


Fig. 8. On-resistance as a function of (a) N_d and W; (b) N_d and H; (c) BV and on-resistance as a function of N_d ($L_d=23$ μm).

(PLDMOS) has obtained the lowest temperature, because the buried oxide is patterned to have a silicon window that connects the active region to the substrate offering a heat conduction path, thereby resulting in reduced self-heating. The CLDMOS gets a medium temperature due to the lowest on-resistance, leading to the decreasing self-heating.

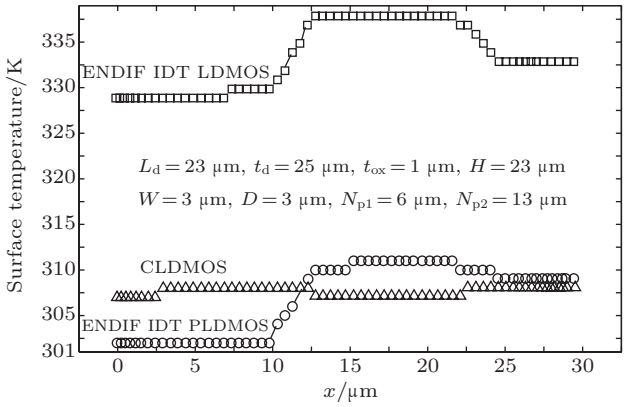


Fig. 9. Surface temperature distribution with same drain current (the substrate temperature and the drain current are 300 K and 30 mA/mm in the simulation, respectively).

4. Conclusion

A novel higher BV SOI power device with the IDT and N/P pillars is proposed and investigated in this work. In this structure, the drift region is folded by embedding IDT in the active layer, so the length of ionization integral is increased multiply. The electric field is improved in the drift region by N/P pillars from enhanced dielectric layer field effect. The ENDIF IDT LDMOS exhibits a BV of 607 V with a 10 μm drift length, which is increased by 200% in comparison to that of C-LDMOS.

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