Electronic transport properties of silicon junctionless nanowire transistors fabricated by femtosecond laser direct writing*

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Silicon junctionless nanowire transistor (JNT) is fabricated by femtosecond laser direct writing on a heavily n-doped SOI substrate. The performances of the transistor, i.e., current drive, threshold voltage, subthreshold swing (SS), and electron mobility are evaluated. The device shows good gate control ability and low-temperature instability in a temperature range from 10 K to 300 K. The drain currents increasing by steps with the gate voltage are clearly observed from 10 K to 50 K, which is attributed to the electron transport through one-dimensional (1D) subbands formed in the nanowire. Besides, the device exhibits a better low-field electron mobility of 290 $cm^2 \cdot V^{-1} \cdot s^{-1}$, implying that the silicon nanowires fabricated by femtosecond laser have good electrical properties. This approach provides a potential application for nanoscale device patterning.

Keywords: junctionless nanowire transistor, femtosecond laser lithography, electron mobility, quantum transport

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1. Introduction

The rapid downscaling of metal–oxide–semiconductor field-effect transistors (MOSFETs) has posed increasing challenges such as short channel effect and degenerated carrier mobility. In particular, the ultrasharp pn junction with extremely high doping gradients becomes difficult to manufacture as the gate length is reduced down to 10 nm or even less. The junctionless nanowire transistor (JNT) has been recently proposed as a promising alternative to a new generation of transistors.[1,2] The doping concentration of JNT is uniform through the source, channel and drain. The current flows through the bulk of the channel as opposed to just along the surface in comparison with junction-based inversion-mode MOSFET. Consequently, JNT exhibits more excellent electrical performances. The key to fabricating JNT is the formation of an ultra-narrow channel to ensure the full depletion of carriers under zero gate voltage.

For decades, photolithography has been the predominant method of fabricating MOSFETs. Photolithography uses light to transfer a patterned feature from a photomask to photoresist on semiconductor wafer. Since the cost for lithographic equipment and photomask sets keeps rising with each technology generation, alternative cheaper patterning techniques are urgently required. The nanofabrication utilizing laser as an energy source has a multitude of advantages including maskless, three dimensions, high resolution and rapid prototyping,[3,4] providing an attractive method for nanoscale patterning applications. Early experimental results showed that the nanostructures fabricated by laser ablation always have thermal damages. However, femtosecond laser lithography can transform the photoresist by absorbing one or multiple phonons, which will dramatically reduce the thermal damages. In this approach, the focused femtosecond laser is directly used to write the desired image into the photoresist without lithographic mask. Thus, it offers great flexibility due to its maskless and discretionary nature. Previous theoretical and experimental results have proved that the multiphoton nanofabrication has the potential to exceed the diffraction limit.[5] Besides, the interaction between the femtosecond laser and the material occurs only in the vicinity of focal spot, leaving material surface intact. This manufacturing technique has been successfully utilized to fabricate nanoscale dot arrays and lines in silicon wafers.[6,7]

In this paper, we demonstrate the experimental results of JNT fabricated by femtosecond laser two-photon lithography. Two laser beams are focused by an optical lens system to be a writing spot on the wafer surface, which provides the optical energy for transforming the photoresist. Two dry etching processes are implemented to transfer the desired image from the negative SCR500 resin onto the top silicon layer. The fabricated JNT exhibits good gate control ability, large electron mobility, and good low-temperature instability.

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2. Device fabrication

The starting material was a (100)-oriented SOI wafer with a 55-nm-thick top silicon and a 145-nm-thick buried oxide. Two laser beams with the peak wavelengths of 800 nm and 400 nm were utilized to fabricate the device. The pulse width and repetition rate were 100 fs and 82 MHz, respectively. The top silicon layer was uniform heavily doped by phosphorus ion implantation with a dose of 5×10^{13} cm^{-2}, leading to a doping concentration of 1×10^{19} cm^{-3}. It was followed by depositing a 50-nm-thick SiO_2 layer on the top of SOI substrate. The SiO_2 layer was chosen to minimize the standing wave effect of the femtosecond laser.[8] Afterwards, femtosecond laser lithography with optimized laser powers of 3.38 mW for 800 nm laser and 2.02 μW for 400 nm laser was utilized to linearly pattern twin nanowires connecting two pads, as illustrated in Fig. 1(a). The speed of transportation of the sample in this process was 80 μm/s. The laser beams focused by an objective lens with a numerical aperture of 1.45 were scanned onto the substrate covering negative SCR500 resin by adjusting the position of translational stage. The photoresist was exposed via two-photon absorption in the area where the laser beams scanned across the photoresist. Figure 1(b) shows the scanning electron microscopy (SEM) image of the patterned photoresist mask. The desired image was transferred from the negative photoresist onto top silicon layer by two-step inductively coupled plasma (ICP) etching process. First, the deposited SiO_2 layer was etched with the exposed photoresist as hard mask. Afterwards, the top silicon layer was etched with SiO_2 as hard mask. The patterned SiO_2 mask is shown in Fig. 1(c). After the etching step, SiO_2 layer was removed by 5% HF. The SEM image presented in Fig. 1(d) shows that the width of nanowire with smooth surface is about 75 nm on average and the length of nanowire is 500 nm. The transfer line width after etching top silicon layer reduced 8 nm in comparison with the exposed line width on the photoresist. Then the sample was oxidized in dry oxygen at 900 °C for 1 h, resulting in the formation of silicon fin with a height of 28 nm (H) and width of 55 nm (W). The thickness of SiO_2 gate dielectric formed by thermal oxidation was about 22 nm. The length of patterned heavily arsenic doped poly-silicon gate was 320 nm (L).

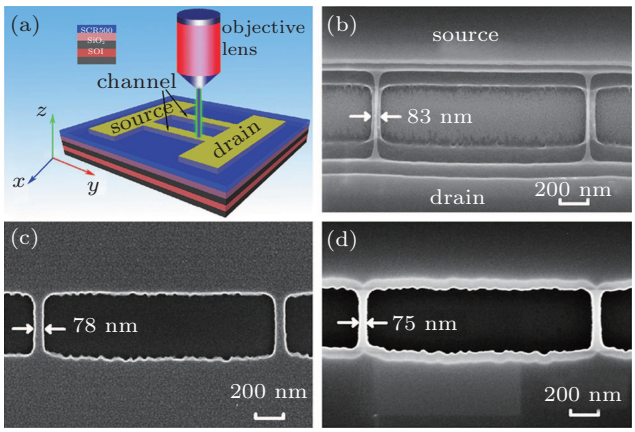


Fig. 1. (color online) (a) Schematic diagram of femtosecond laser process, (b) SEM image of the photoresist patterns, (c) SiO_2 patterns, and (d) silicon patterns after removing SiO_2 mask of the twin-channel JNT.

3. Results and discussion

3.1. Electrical properties at room temperature

The electrical characteristics of JNT are characterized by Agilent B1500 semiconductor parameter analyzer. Low temperature characterizations are carried out by Lakershore-340 temperature controller under high vacuum. At room temperature, the silicon JNT exhibits good transfer and output characteristics. The curves of drain current I_{DS} versus gate voltage V_{GS} in Fig. 2(a) show that the fabricated JNT operates as a normally-off device with a low gate leakage current of several pA. The SS and the threshold voltage (V_{th}) are 140 mV/dec and 0.68 V, respectively. The on/off current ratio is large than 1×10^7.

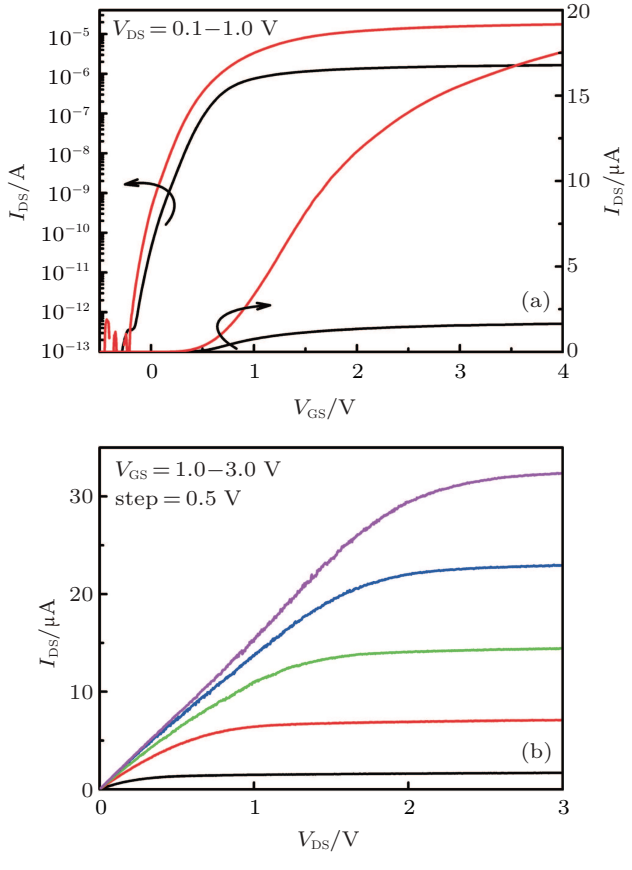


Fig. 2. (color online) Measured drain current characteristics at room temperature, showing (a) drain current versus gate voltage for drain voltages of 0.1 V and 1.0 V, and (b) drain current versus drain voltage for different gate voltages.

The plot of the extracted transconductance ($g_m = \partial I_{DS}/\partial V_{GS}$) versus V_{GS} from transfer characteristics at $V_{DS} =$ 10 mV is shown in Fig. 3. The low-field electron mobility μ_0 is extracted in linear part by using $Y = I_{DS}/\sqrt{g_m}$ method, which

is independent of the series resistance and mobility attenuation factor, and expressed by[9]

$$I_{DS}/\sqrt{g_m} = [(W_{eff}/L)C_{ox}\mu_0 V_{DS}]^{1/2}(V_{GS} - V_{th}). \quad (1)$$

Here C_{ox}, is the gate capacitance per unit area and estimated to be 1.56×10^7 F/cm^2 for 22-nm-thick gate oxide layer, L is the gate length, and $W_{eff} = 2(W + 2H)$ is the effective width for twin silicon nanowires. The inset of Fig. 3 shows the corresponding plot of the $I_{DS}/\sqrt{g_m}$ as a function of V_{GS}. The extracted low-field mobility at $V_{DS} = 10$ mV is 290 cm^2·V^{-1}·s^{-1}. This suggests that the femtosecond laser lithography can impede damages normally introduced by high thermal density in laser ablation process, resulting in enhanced electron mobility in JNT.

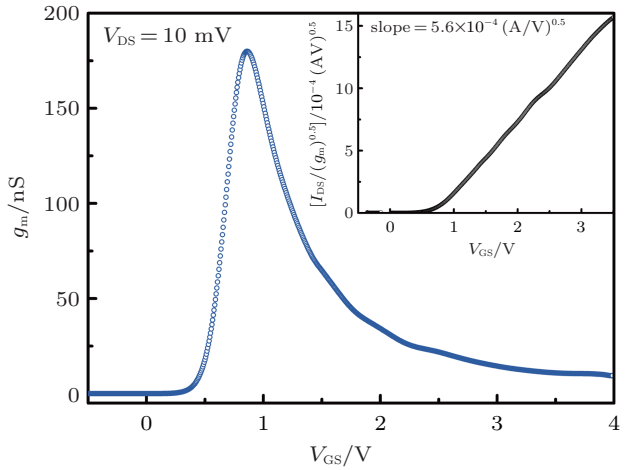


Fig. 3. (color online) Plot of transconductance g_m versus V_{GS} at $V_{DS} = 10$ mV, with the inset showing the corresponding $I_{DS}/\sqrt{g_m}$ plot for the device.

3.2. Temperature-dependent transfer characteristics

Next, we focus on the temperature-dependent transport of JNT. When the temperature is reduced, the interesting electrical results are observed. Figure 4(a) shows the measured transfer characteristics of JNT with $V_{DS} = 10$ mV at different temperatures. The I_{DS} decreases with temperature decreasing. Significantly, the transfer characteristic exhibits stepwise features below temperature ~ 50 K, as a result of the Fermi energy E_f being tuned through the density of states (DOS) peaks of 1D subbands.[10] However, the step-like feature is found to be smeared out with the thermal smearing of 1D energy levels above 50 K. This is because the thermal broadening (k_BT) at 50 K are too large to distinguish the energy separation between quantized subbands, where k_B is the Boltmann constant.[11] Figure 4(b) shows the transfer curve and the corresponding transconductance g_m as a function of V_{GS} at the low temperature of 10 K. The black arrows mark the fixed gate voltage positions for the g_m valleys. The positions correspond to the gate voltages of 1.27 V, 1.41 V, 1.56 V, and 1.74 V. The dotted lines mark the corresponding conductance heights. The height ratio of four current steps is 0.70:2.00:2.34:1.00. The heights of the first and fourth current step are approximately half the second step and half the third step, respectively, which infers that the second and third subband are two-fold degenerate with respect to the other two subbands. The interesting observation can be ascribed to the splitting of equivalent valley in silicon conduction band. The six valleys of silicon are split into twofold degenerate valleys and fourfold degenerate valleys according to the effective mass.[12,13] A noticeable point is that the step-like current is not evident above a gate voltage of 1.8 V. It infers that 1D electron confinement effect is more obvious at the initial stage of the transfer characteristics. In n-type JNT, electron transport regime is surrounded by a high-depleted potential barrier under flatband condition, leading to a more remarkable quantum confinement effect than that under the above flatband condition. The result is in good agreement with the theoretical result.[14]

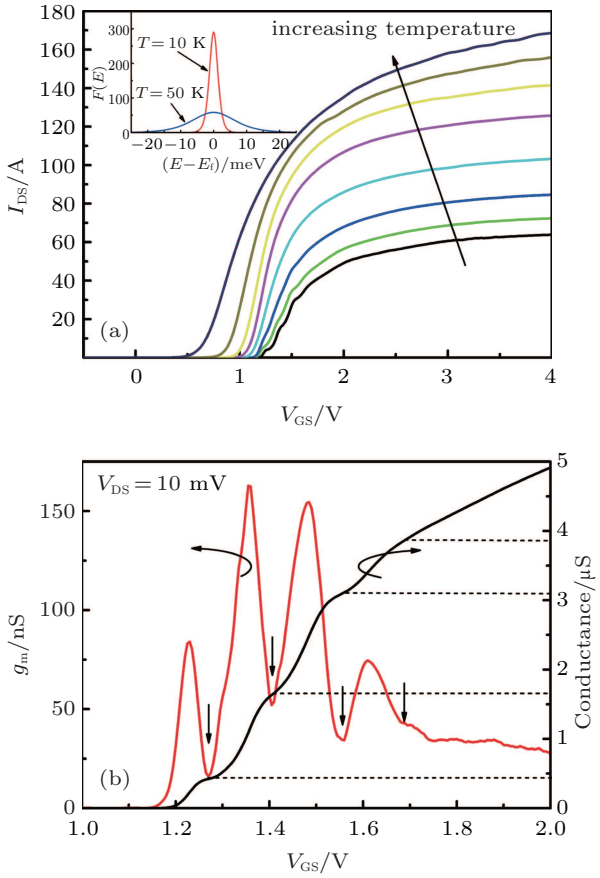


Fig. 4. (color online) (a) Plots of measured I_{DS} versus V_{GS} at different temperatures (10 K, 20 K, 50 K, 100 K, 150 K, 200 K, 250 K, and 300 K) and $V_{DS} = 10$ mV. The insert shows thermal broadening functions[15] at 10 K and 50 K. The energy distribution of electrons at 10 K is significantly narrower. (b) Conductance and transconductance characteristics of JNT measured at 10 K with $V_{DS} = 10$ mV.

3.3. Temperature-dependent electrical parameters

Any variation of temperature will induce the change of electrical parameters of JNT device, such as the threshold voltage, flatband voltage, subthreshold swing and electron mobility. Temperature instabilities of some electrical parameters are

investigated in a temperature range from 50 K to 300 K.

The left curve of Fig. 5(a) shows the variation of maximum transconductance $g_{m,max}$ with temperature in the predicated value. Since $g_{m,max}$ is a measure of the peak effective mobility, the variation of $g_{m,max}$ with temperature reflects the variation of electron effective mobility with temperature. The measured result shows that the electron mobility increases in a temperature range from 50 K to 175 K, because impurity coulomb scattering is dominant in the scattering rate for the heavily doped channel at low temperatures. While the electron mobility decreases in a temperature range from 175 K to 300 K, which can be ascribed to the enhancement of phonon scattering at higher temperatures. Our data are in agreement with the reported results in Ref. [16]. The SS follows the theoretical expression $SS = n(k_BT/q)\ln(10)$, where n is the body effect coefficient. The value of n equals 1 in the ideal condition. The right plot in Fig. 5(a) shows the temperature dependence of SS. It almost presents a linear decrease in a temperature range from 300 K to 150 K and the average value of n is 2.8, which stems from the existence of traps around Si/SiO_2 interface and in the poly-silicon gate. However, the shift slope of SS with temperature becomes slightly smaller than the predicted value at temperatures lower than 100 K due to the nonuniform distribution of traps,[17] which is mainly induced by etching and thermal oxidation procedure.

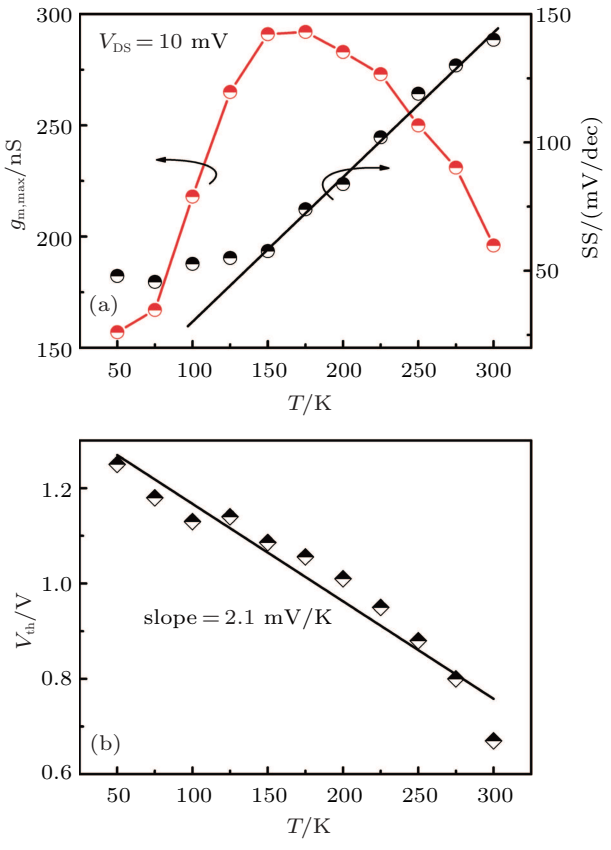


Fig. 5. (color online) (a) Temperature-dependent SS and the maximum g_m. (b) Experimental V_{th} of JNT as a function of temperature. The applied V_{DS} equals 10 mV.

Figure 5(b) shows the evolution of V_{th} with temperature. It can be seen that V_{th} is negatively shifted with temperature increasing. The experimental negative shift of V_{th} is 2.1 mV/K. From Ref. [18], the variation of V_{th} with temperature is expressed as

$$\frac{dV_{th}}{dT} = \frac{k_B}{q}\ln\left(\frac{N_d}{n_i}\right) - \frac{k_BT}{q}\frac{1}{n_i}\frac{dn_i}{dT}, \tag{2}$$

where n_i and N_d denote intrinsic carrier density and the doping concentration, respectively. The theoretical value of dV_{th}/dT is 0.45 mV/K, which is much smaller than the experimental value of 2.1 mV/K. We attribute this phenomenon to the influence of thermal activation of traps.[19,20]

4. Conclusions

In this work, the JNT with the physical channel cross-section area of 28 nm×55 nm is fabricated by femtosecond laser lithography. The extracted low-field electron mobility is 290 $cm^2 \cdot V^{-1} \cdot s^{-1}$, inferring that this method can well impede the damage of the crystalline structure of silicon. Besides, the increase of current steps with gate voltage is clearly observed at a temperature of 10 K, which is attributed to the electron transport through degenerated 1D subbands formed in the nanowire. The mobility is phonon limited at temperatures larger than 175 K, while it appears to be limited by impurity scattering below that temperature. The slope of threshold voltage shift with the temperature is 2.1 mV/K due to the influence of interface traps. These results help us better understand the transport mechanism in JNT at low temperatures. The development of this novel maskless lithography has tremendous potential for opening a new market in nanoscale device fabrication. The low cost and high resolution process is expected to provide an accurate, repeatable and efficient means of creating nanoscale structures for device applications.

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References

[1] Colinge J P, Lee C W, Afzalian A, Akhavan N D, Yan R, Ferain I, Razavi P, O'Neill B, Blake A, White M, Kelleher A M, McCarthy B and Murphy R 2010 *Nat. Nanotechnol.* **5** 225
[2] Ionescu A M 2010 *Nat. Nanotechnol.* **5** 178
[3] Zhang Y L, Chen Q D, Xia H and Sun H B 2010 *Nano Today* **5** 435
[4] Nakata Y, Okada T andMaeda M 2002 *Appl. Phys. Lett.* **81** 4239
[5] Kawata S, Sun H B, Tanaka T and Takada K 2001 *Nature* **412** 697
[6] Juodkazis1 S, Mizeikis1 V, Seet K K, Miwa M and Misawa1 H 2005 *Nanotechnology* **16** 846
[7] Tan D, Li Y, Qi F, Yang H and Gongb Q 2007 *Appl. Phys. Lett.* **90** 071106
[8] Carvalho E J, Alves M A, Braga E S and Cescato L 2006 *Microelectr. J.* **37** 1265
[9] Ghibaudo G 1988 *Electron. Lett.* **24** 543

[10] Wang H, Han W H, Ma L H, Li X M and Yang F H 2014 *Chin. Phys. B* **23** 088107

[11] Yuan T, Mohammed R S, Jesse M K, Dong L, Michael J M, Richard L J Q, Hong J G and Xuan P A G 2012 *Nano Lett.* **12** 6492

[12] Ma L H, Han W H, Wang H, Yang X and Yang F H 2015 *IEEE Electron Dev. Lett.* **36** 941

[13] Kim R and Lundstrom M S 2008 *IEEE Trans. Nanotechnol.* **7** 787

[14] Duarte J P, Kim M S, Choi S J and Choi Y K 2012 *IEEE Trans. Electron Dev.* **59** 1008

[15] Philip F B and Terry P O 1989 *Phys. Rev. B* **40** 1456

[16] Souza M de, Pavanello M A, Trevisoli R D, Doria R T and Colinge J P 2011 *IEEE Electron Dev. Lett.* **32** 1322

[17] Colinge J P, Floyd L, Quinn A J, Redmond G, Alderman J C, Xiong W, Cleavelin C R, Schulz T, Schruefer K, Knoblinger G and Patruno P 2006 *IEEE Electron Dev. Lett.* **27** 172

[18] Jeon D Y, Park S J, Mouis M, Barraud S, Kim G T and Ghibaudo G 2013 *Solid State Electron.* **80** 135

[19] Kordoš P, Donoval D, Florovič M, Kováč J and Gregušová D 2008 *Appl. Phys. Lett.* **92** 152113

[20] Zhang Y M, Feng S W, Zhu H, Gong X Q, Deng B and Ma L 2014 *J. Semicond.* **35** 104003