Numerical simulation study of organic nonvolatile memory with polysilicon floating gate

Zhao-wen Yan(闫兆文), Jiao Wang(王娇), Jian-li Qiao(乔坚栗), Wen-jie Chen(谌文杰), Pan Yang(杨盼), Tong Xiao(肖彤), and Jian-hong Yang(杨建红)†

Institute of Microelectronics, Lanzhou University, Lanzhou 730000, *China*

(Received 26 November 2015; revised manuscript received 31 January 2016; published online 20 April 2016)

A polysilicon-based organic nonvolatile floating-gate memory device with a bottom-gate top-contact configuration is investigated, in which polysilicon is sandwiched between oxide layers as a floating gate. Simulations for the electrical characteristics of the polysilicon floating gate-based memory device are performed. The shifted transfer characteristics and corresponding charge trapping mechanisms during programing and erasing (P/E) operations at various P/E voltages are discussed. The simulated results show that present memory exhibits a large memory window of 57.5 V, and a high read current on/off ratio of $\approx 10^3$. Compared with the reported experimental results, these simulated results indicate that the polysilicon floating gate based memory device demonstrates remarkable memory effects, which shows great promise in device designing and practical application.

Keywords: organic floating gate memory, polysilicon floating gate, programing and erasing operations, device simulation

PACS: 71.15.–m, 73.22.–f, 73.50.–h, 74.20.Pq **DOI:** 10.1088/1674-1056/25/6/067102

1. Introduction

Organic nonvolatile floating gate memory (ONFGM) devices based on organic thin film transistors (OTFTs) with typical physical structures and unique working mechanism have been widely investigated recently due to their nondestructive read-out, simple preparation process and single transistor realization.[1–4] Meanwhile the performance of the ONFGM device was greatly improved by optimizing the physical structures and memory materials.[5,6] Relevant researches have demonstrated that high k dielectric materials because of their excellent capacitance ratio usually served as the gate dielectric layer to scale down operating voltage, and metallic nanoparticles were imbedded within the gate dielectric interface acting as charge trapping sites to reduce the stress-induced leakage current by precisely controlling the size and trap density of metallic nanoparticles.[7–12] It has also been demonstrated that memory performances could be improved with light assisted program.[13] Recently, Yi *et al.* demonstrated that light illumination and electrical stress can act as an independent programming/erasing operation method, by which the stable ambipolar memory properties were observed and a large memory window, excellent retention time and high ON/OFF current ratio of the ambipolar memory device were obtained to be 70 V, 10^4 s and 10^4, respectively.[14] Tseng *et al.* improved the characteristics of the memory device, and their researches mainly focused on introducing a double-floating gate monolayer, which included a diacetylenic (DA) unit as a hole carrier trap and a naphthalenetetracarboxyldiimide (ND) unit as an electron carrier trap.[15] The memory device with the double-floating gate monolayer exhibited a larger memory window, longer retention time and rather stable device characteristics than with the single-floating gate. Kim *et al.* placed a graphene oxide layer between two polystyrene (PS) layers as charge storage medium, and their work demonstrated the multilevel characteristics of nonvolatile floating-gate memory devices.[16] In addition, Jung *et al.* investigated the particle size effects on the memory performance by using semiconducting cobalt ferrite nanoparticles as charge trap sites.[17] Nevertheless, up to now it has remained a significant challenge of improving the data retention property and scale down operating voltage of ONFGM devices, simultaneously. Clearly, the memory effects are strongly dependent on the floating gate trapping and detrapping charge carriers at an external gate voltage. It is actually difficult to measure the variations of charge stored in a floating gate in the P/E process. While research about multilevel characteristics of the ONFGM device with a sandwiched poly-silicon (Poly-Si) floating gate between two oxide layers, in particular the variations of charge stored in the floating gate, have been scarce. Hence, it is highly needed to have an insight into the operating mechanism and the shifted effects of transfer curves at different programming and erasing voltages (V_P/V_E).

In this work, simulation for the electrical characteristics of the ONFGM device is developed by employing poly-Si as a floating gate. Because poly-Si has widely been studied in inorganic memory devices and the relevant results show that poly-Si effectively increases charge traps.[18] In particular, the shifted effects of transfer curves and the corresponding varia-

†Corresponding author. E-mail: yangjh@lzu.edu.cn

© 2016 Chinese Physical Society and IOP Publishing Ltd

tions of charge stored in the floating gate during P/E operations are discussed in detail by the simulated results and the energy band diagrams. In addition, simulation on dynamic memory switching behavior is also carried out.

The rest of the present paper is organized as follows. In Section 2, the device structure and relevant simulating models are introduced. The numerical simulation process is also given. In Section 3, the numerical simulation for the electrical characteristics including output and transfer curves and memory features of ONFGM are discussed in detail. Finally, some significant conclusions are drawn from the present studies in Section 4.

2. ONFGM device structure and simulation

2.1. ONFGM device structure

Taking into consideration the sequence of thermal treatment process and the excellent performance the memory exhibits, the configuration of device in this work is designed into bottom-gate, top-contact p-channel ONFGM as shown in Fig. 1. In this cross-sectional structure model, pentacene with high hole-mobility[19,20] is covered on the tunneling insulator as an active layer and polysilicon is inserted into the oxide layer as a charge storage medium. Gold with a high workfunction is used as the source/drain contact which is propitious to injection and extraction of holes between the metal electrode and the organic semiconductor channel. The control gate directly contacts the heavily doped n-type silicon. The detailed physical and structural parameters are listed in Table 1.

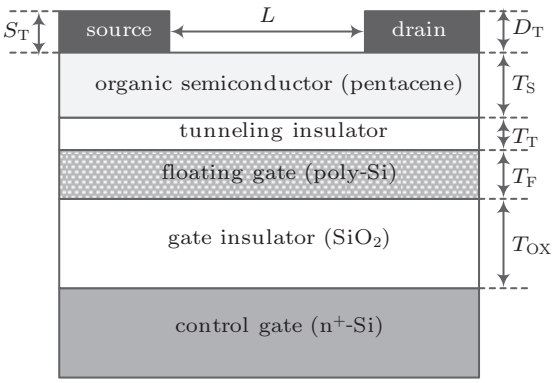


Fig. 1. Schematic cross section of ONFGM based on pentacene with a bottom-gate, top-contact structure.

Table 1. Physical and structural parameters used for device simulation.

Parameter	Symbol	Value
Channel length	L/μm	10, 20, 30
Channel width	W/mm	2
Thickness of source and drain electrode (Au)	S_T, D_T/nm	40
Thickness of organic semiconductor	T_S/nm	60
Thickness of tunneling insulator	T_T/nm	10
Thickness of floating gate	T_F/nm	20
Thickness of gate insulator	T_{OX}/nm	300
Dielectric constant of gate insulator (SiO_2)	ε_s	3.9
Dielectric constant of organic semiconductor		3
Schottky barrier height	φ_B/eV	$0.1 \sim 0.3$
Band gap of organic semiconductor	E_g/eV	$1.8 \sim 2.2$
Work function (Au)	W_F/eV	$5.10 \sim 5.47$
Impurity concentration of gate region	n^+/cm^{-3}	1×10^{19}
Lowest unoccupied molecular orbital level of pentacene	LUMO/eV	–3.2
Highest occupied molecular orbital level of pentacene	HOMO/eV	–5.0

2.2. Simulation for device

The geometry of the ONFGM device resembles that of OTFT except the tunneling insulator and floating gate that are sandwiched between the organic semiconductor and the gate insulator. Based on the investigation of p-channel OTFTs,[21,22] the charge carriers transporting mechanism is strongly dependent on the temperature, electric field and holes traps between the organic semiconductor channel, electrode and gate dielectric layer.[23,24] Therefore, the simulations for the charge carrier transport of the ONFGM device are carried out by solving Poisson's equation, continuity equation and holes drift-diffusion equation, which are described as follows:[25–28]

$$\nabla(\varepsilon_0\varepsilon_S\nabla\varphi) = q(n - p + N_t - P_t), \tag{1}$$

$$\nabla \cdot J_p = q(G - R), \tag{2}$$

$$J_p = q\mu_p(E)E - qD_p\frac{\partial p}{\partial x}, \tag{3}$$

$$D_p = \mu_p(E)\frac{k_0 T}{q}, \tag{4}$$

where φ is the electrostatic potential, N_t and P_t are the densities of trapped electrons and holes respectively, n and p are the electron and hole's concentration, J_p is the hole current density, G is the hole generation rate strongly dependent on the hole potential barrier, R is the recombination rates, E is the

electric field, and D_p is the hole diffusion coefficient. According to the Einstein equation (4), J_p is expressed as

$$J_p = q\mu_p(E)\cdot\left(E - \frac{k_0T}{q}\cdot\frac{\partial p}{\partial x}\right), \tag{5}$$

here, k_0 is the Boltzmann constant, T is the absolute temperature (300 K), and $\mu_p(E)$ is the Poole–Frenkel mobility given by[29]

$$\mu_p(E) = \mu_{p0}\exp\left[-\frac{E_{h0}}{k_0T} + \left(\frac{\beta}{k_0T} - \gamma\right)\sqrt{E}\right]. \tag{6}$$

In this model, μ_{p0} is the low field mobility and E_{h0} represent the activation energy for hole ($E = 0$) which is equal to 0.018 eV, β is the hole Poole–Frenkel factor, and γ is the fitting parameter. For obtaining prominent simulation results, the contact between electrode and organic semiconductor are regarded as a Schottky barrier (0.1 eV$\sim$0.3 eV). Moreover, in an organic semiconductor material, the effective density of states at the lowest unoccupied molecular orbital (LUMO) level is considered to be the same as that at the highest occupied molecular orbital (HOMO) level.[30,31] In addition, the hot carrier injection and Fowler–Nordheim (FN) tunneling model are utilized for simulating holes injected into or extracted from the floating gate during P/E operation. The thermal emission current J and tunneling current J_{FN} are respectively given as follows:[32,33]

$$J = A^*T^2\exp\left(-\frac{\varphi_T - \sqrt{q^3E}/4\pi\varepsilon_{OX}}{k_0T}\right), \tag{7}$$

$$J_{FN} = \frac{q^3E^2m_0}{8\pi h\varphi_T m_p^*}\exp\left(\frac{-4\sqrt{2m_p^*}\varphi_T^{2/3}}{3hqE}\right), \tag{8}$$

where J and J_{FN} are influenced mainly by E, T, and φ_T (φ_T is defined as the interface barrier height between semiconductor and tunneling insulator (programing) or tunneling insulator and floating gate (erasing)), A^* is Richardson constant expressed as $A^* = 4\pi qm_p^*k_0^2/h^3$, with m_p^* being the effective hole mass and h being the Planck constant, and m_0 being the free hole mass.

Based on the models above, the electrical characteristics of the ONFGM device are simulated and calculated reasonably through Newton's iteration method. Figure 2 shows the flow chart of numerical simulation.

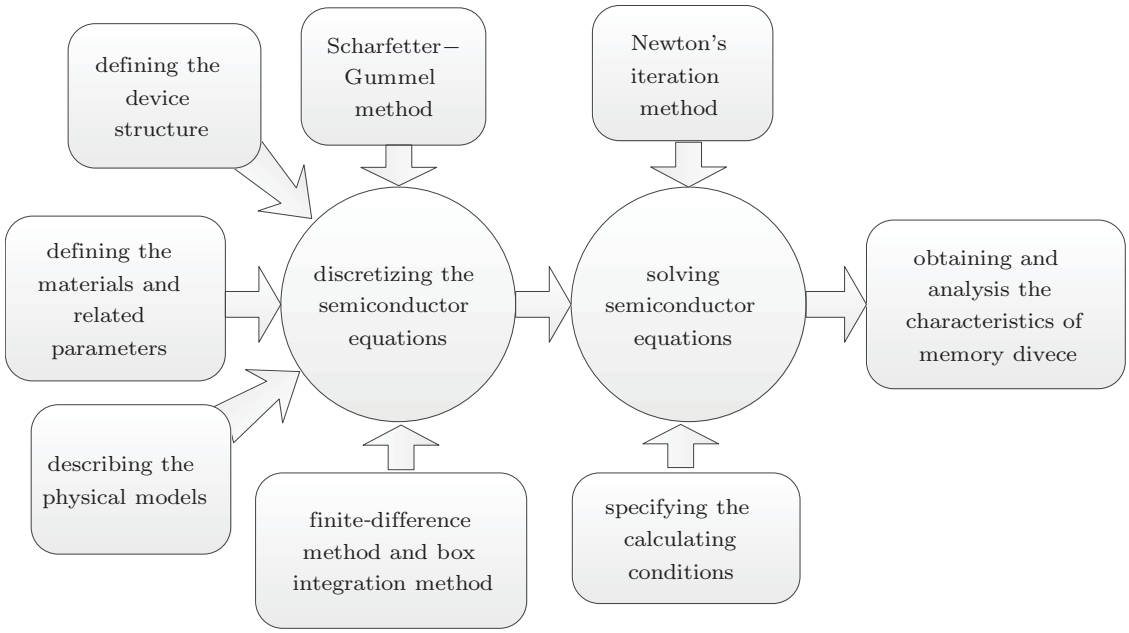


Fig. 2. Flow chart of numerical simulation.

3. Simulation results and discussion

3.1. Output and transfer characteristics of ONFGM device

The simulations of the output and transfer characteristics of our present ONFGM device are performed, and the simulated results indicate that the device features typical p-channel field-effect behavior in hole-accumulation mode during V_{DS} ranging from 0 V to −20 V and V_{GS} from 0 V to −20 V in steps of −5 V as shown in Fig. 3(a). In comparison with the experimental data,[34] the simulated results of output curves are in the appropriate order of magnitude and the current values are superior to that of Au-nanocrystal memory within a certain voltage range. Figure 3(b) shows the simulated transfer curves for the channel length (L) ranging from 10 μm to 30 μm. The regulation effect of gate on channel current increases with channel length decreasing from 30 μm to 10 μm. The inset shows the behavior of a small fraction of holes accumulating at the channel in the case of low-ranging V_{GS} which is possibly attributed to the induced weak electric field of trapped

charge carriers generated from the floating gate. This behavior is in good agreement with that in the literature.[35]

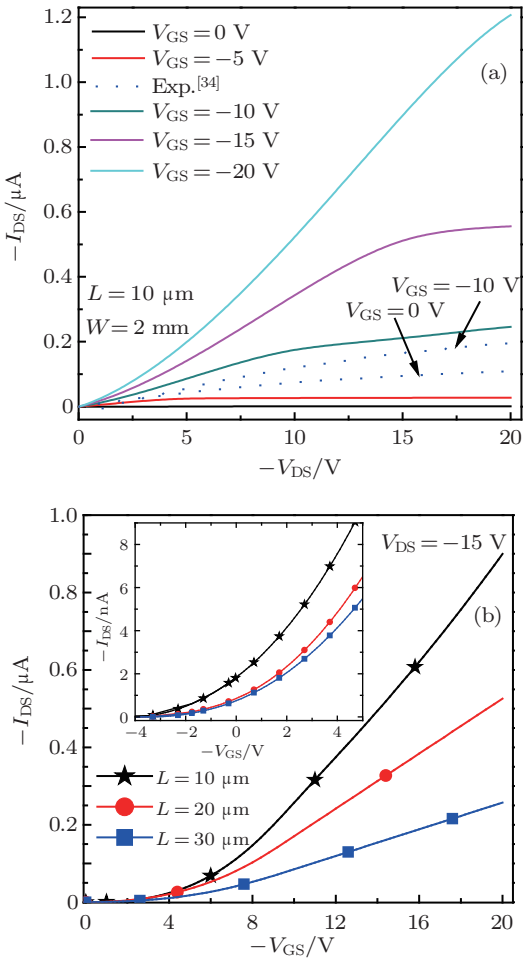


Fig. 3. (color online) (a) Output characteristic curves of ONFGM with a channel length of 10 μm. (b) Comparison of the transfer characteristic curves with different channel lengths. The inset shows the transfer curves at low gate voltages.

3.2. Electrical memory characteristics of ONFGM device

According to the above analysis, by employing the hot hole injection model and the FN tunneling model, the (P/E) characteristics of the present ONFGM are simulated and the effects associated with shifts in transfer curves are examined through a series of P/E operations in a sequence of programing voltages (V_P) and erasing voltages (V_E), respectively. For all of the P/E operations, the drain-source voltage (V_{DS}) is maintained at 0 V and the P/E time is set to be 5 s, holes are majority charge carriers in the present ONFGM which is operated in the p-channel as mentioned in Subsection 3.1.

Figure 4(a) shows the energy level of the present ONFGM device, where E_0 is the vacuum energy level, LUMO and HOMO are the lowest unoccupied molecular orbital level and the highest occupied molecular orbital level of pentacene, which are −3.2 eV and −5.0 eV, respectively.[36] During programing operations, a high negative voltage is applied to the gate, holes accumulate at the interface between channel and SiO_2, and the energy band of the ultrathin SiO_2 layer is extremely bended so that holes are injected from the channel into the poly-Si floating gate (Fig. 4(b)). Once holes are injected in the floating gate, a shift towards the threshold voltage (ΔV_T) will be induced as depicted in Fig. 5(a).

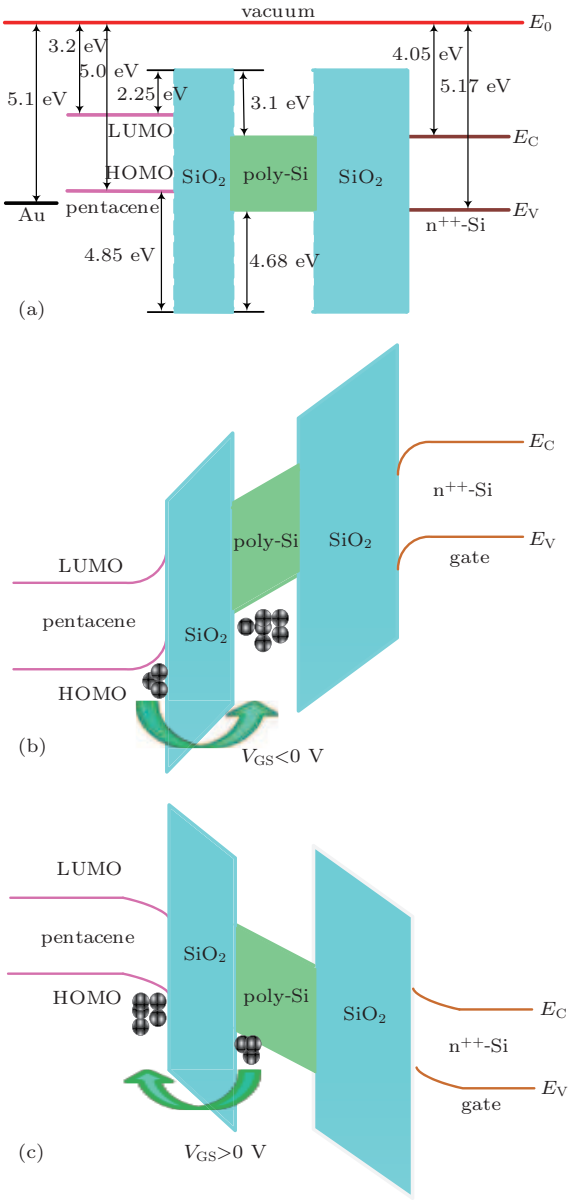


Fig. 4. (color online) (a) Energy level diagram of ONFGM without applying voltage, (b) energy band diagrams of ONFGM during programming, and (c) erasing operations.

It is clearly revealed that the transfer curves shift rapidly in the negative direction with the increase of V_P from −45 V to −60 V, and then more slowly as V_P increases from −60 V to −70 V. To further confirm that the shift effect of the transfer curve is attributed to the trapped holes in the floating gate, the variations of poly-Si floating gate charge are simulated as shown in Fig. 5(b) (logarithmic coordinates). The variations of poly-Si floating gate charge show that the holes injected from the channel to the poly-Si floating gate first increase rapidly with the increase of V_P, and then gradually increase slowly as V_P increases from −60 V to −70 V which is consistent with

the shifted effect of the transfer curve. This also demonstrates that the charge stored in the floating gate will not increase even though the programing time is very long. Based on the equation $\Delta n = \Delta Q/e$ (where Δn is the number of transferred charge carriers, ΔQ is the total charge quantity of transferred charge carriers and e is the elementary charge), the number of transferred holes is $\approx 10^{11}$ which is slightly inferior to that of $CoFe_2O_4$ NPs-structure memory in Ref. [17].

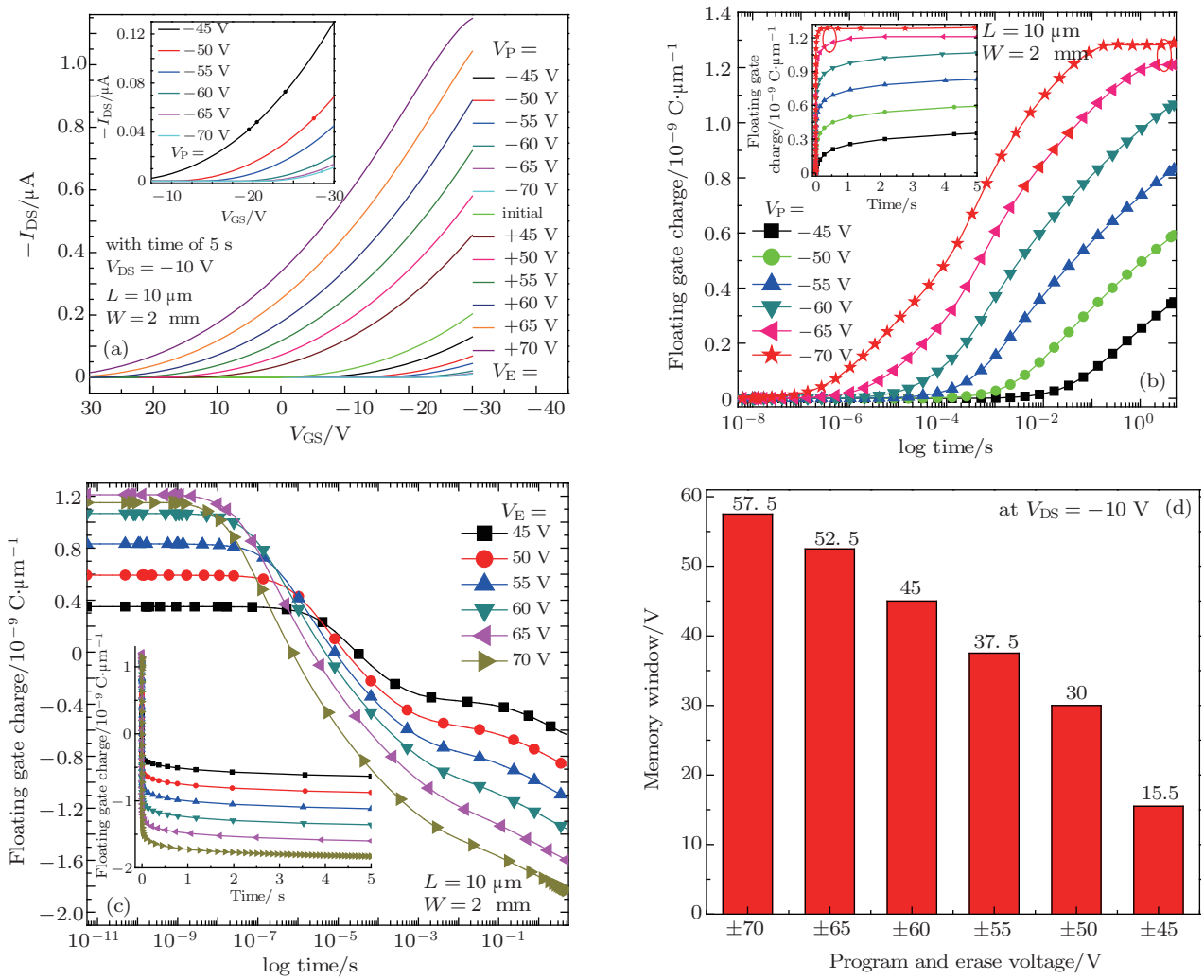


Fig. 5. (color online) (a) Transfer curves of the ONFGM device in the initial and a series of post-P/E operations at various of V_P/V_E voltages in a time of 5 s. The inset shows the shifts in transfer curves during P operations at V_{GS} ranging from −5 V to −30 V. (b) Corresponding variations of charge stored in the poly-Si floating gate in logarithmic coordinates and the inset in linear coordinates during P operation and (c) E operation. (d) Memory windows for various V_P and V_E voltages.

After a series of programing operations, a series of erasing operations are performed. As depicted in Fig. 5(a), it is obviously observed that the transfer curves shift towards the positive direction rather than return to the initial state with the V_E increasing from 45 V to 70 V. Moreover, after erasing operations, the values of the shifts in transfer curves towards the positive direction are larger than towards the negative direction in the case of post-programing operations. These phenomena also result from the variations of charge carriers stored in the poly-Si floating gate. As depicted in Fig. 5(c), holes are gradually extracted from the poly-Si floating gate to the channel, which induces a shift of transfer curves towards the positive values. It is notable that the value of charge stored in the poly-Si floating gate decreases to zero with the erasing time increasing from $\times 10^{-5}$ s to 1×10^{-4} s, which suggests that the transfer curves should return to the initial state. However, it is interesting that the value of charges changes into a negative value with the increase of erasing time, by which the transfer curves continually shift towards the positive direction. Owing to a high barrier height of 1.9 (eV) between the LUMO of pentacene (3.2 eV) and the work function of Au (5.1 eV), electrons are limited to be injected into the channel.[37] In this case, the holes stored in the floating-gate are first ejected from the floating-gate to the channel at large positive gate voltage, and then electrons at the interface between organic semiconductor and SiO_2 layer transfer from the LUMO (lowest unoccupied molecular orbital) level of pentacene to the conduction band of the polysilicon floating-gate by tunneling through a thin SiO_2 layer. Although the electrons are minority carriers in the p-type pentacene active layer, the energy barrier

(2.25 eV) for electron transport between the LUMO level of pentacene and the conduction band of SiO_2 is lower than that (4.85 eV) for holes transport between the HOMO (highest occupied molecular orbital) level and the valence band of SiO_2. Therefore, the above behavior is possibly explained by the fact that the electrons at the interface between the organic semiconductor and the SiO_2 layer are injected into the channel by high positive V_E. Moreover, due to the fact that the barrier (4.68 eV) between the poly-Si floating gate and the SiO_2 tunneling insulator in the case of erasing operations is slightly lower than the barrier (4.85 eV)[38] between the HOMO level of pentacene and the poly-Si floating gate in the case of programing operations, it is easier for holes to be ejected from the poly-Si floating gate to the channel during erasing operations than from the channel to the poly-Si floating gate during programing operations. In contrast, the obvious shifts of transfer curves towards the positive and negative direction by P/E operations are matched correctly with those in the literature.[39] As a result, a large memory window (ΔV_T) of 57.5 V is obtained at V_P/V_E of ± 70 V in a time of 5 s. Figure 5(d) shows the values of V_T at different V_P/V_E voltages.

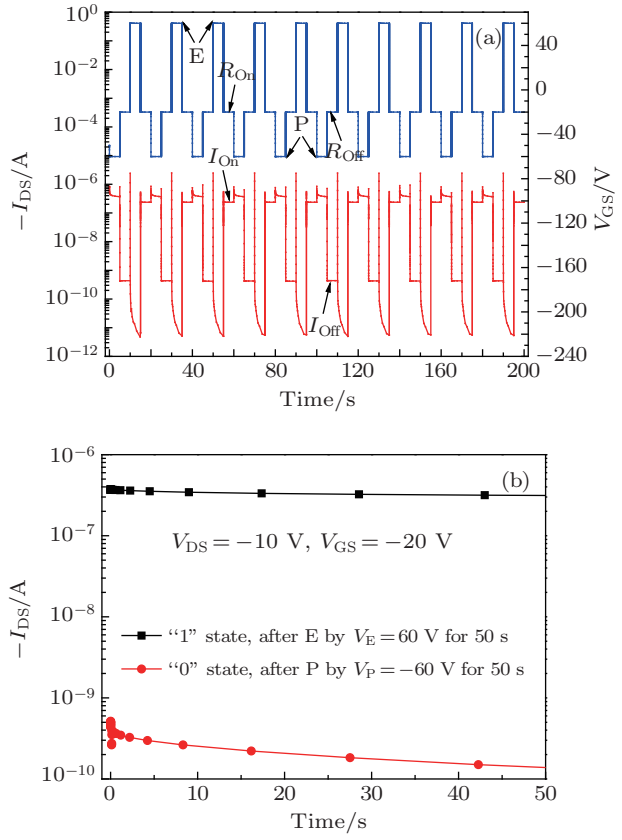


Fig. 6. (color online) (a) Switching behavior for the ONFGM device with poly-Si floating gate (E: erase, P: program, R_{On}: read-on state, and R_{Off}: read-off state), and (b) the drain currents of ON state and OFF state after erase and program.

In the present ONFGM device, the drain current responses for program, read, erase, and read cycles, which are called dynamic memory switching behaviors, are also simulated at sequential and repeated gate voltages of -60, -20, 60, and -20 V in an interval time of 5 s as shown in Fig. 6(a). Meanwhile, the ON/OFF memory current ratio is calculated to be about 10^3 as shown in Fig. 6(b).

4. Conclusions

In this work, simulations for the present ONFGM device by sandwiching polysilicon between oxide layers as a floating gate are performed through basic organic transporting, hot holes injection, and FN tunneling models. The simulated results demonstrate that the poly-Si floating gate based ONFGM device exhibits remarkably memory effects which include a large memory window of 57.5 V, excellent switching behavior, and a high read I_{On}/I_{Off} of $\approx 10^3$. In addition, the values of shifts in transfer curves towards the positive direction after erasing operations are larger than towards the negative direction after programing operations. It is of great value that employing the simulations for the variations of charge stored in the floating gate during P/E operations examines and explains the shifted effects of transfer curves which are attributed to the transferred charge carriers at various V_P/V_E voltages. These simulated results are significantly helpful in designing devices and understanding the storage characteristics of the ONFGM device.

References

[1] Leong W L, Mathews N, Tan B, Vaidyanathan S, Dötz F and Mhaisalkar S 2011 *J. Mater. Chem.* **21** 5203
[2] Kang M, Kim Y A, Yun J M, Khim D, Kim J, Noh Y Y, Baeg K J and Kim D Y 2014 *Nanoscale* **6** 12315
[3] Gao X, Liu C H, She X J, Li Q L, Liu J and Wang S D 2014 *Org. Electron.* **15** 2486
[4] Cho I, Kim B J, Ryu S W, Cho J H and Cho J 2014 *Nanotechnology* **25** 505604
[5] Dai M K, Lin T Y, Yang M H, Lee C K, Huang C C and Chen Y F 2014 *J. Mater. Chem. C* **2** 5342
[6] Kaltenbrunner M, Stadler P, Schwödiauer R, Hassel A W, Sariciftci N S and Bauer S 2011 *Adv. Mater.* **23** 4892
[7] Gao X, She X J, Liu C H, Sun Q J, Liu J and Wang S D 2013 *Appl. Phys. Lett.* **102** 023303
[8] Sekitani T, Yokota T, Zschieschang U, Klauk H, Bauer S, Takeuchi K, Takamiya M, Sakurai T and Someya T 2009 *Science* **326** 1516
[9] Shang L, Ji Z, Wang H, Chen Y, Liu X, Han M and Liu M 2011 *IEEE Electron Dev. Lett.* **32** 1451
[10] Kang M, Baeg K J, Khim D, Noh Y Y and Kim D Y 2013 *Adv. Funct. Mater.* **23** 3503
[11] Haik M Y, Ayesh A I, Abdulrehman T and Haik Y 2014 *Mater. Lett.* **124** 67
[12] Han S T, Zhou Y, Xu Z X, Roy V A L and Hung T F 2011 *J. Mater. Chem.* **21** 14575
[13] Wang H, Ji Z, Shang L, Chen Y, Han M, Liu X, Peng Y Q and Liu M 2011 *Org. Electron.* **12** 1236
[14] Yi M D, Xie M, Shao Y Q, Li W, Ling H F, Xie L H, Yang T, Fan Q L, Zhua J L and Huang W 2015 *J. Mater. Chem. C* **3** 5220
[15] Tseng C W, Huang D C and Tao Y T 2015 *ACS Appl. Mater. Interfaces* **7** 9767
[16] Kim Y N, Lee N H, Yun D Y and Kim T W 2015 *Org. Electron.* **25** 165
[17] Jung J H, Kim S, Kim H, Park J and Oh J H 2015 *Small* **11** 4976
[18] Lee K H, Tsai J R, Chang R D, Lin H C and Huang T Y 2013 *Appl. Phys. Lett.* **103** 153102
[19] Gundlach D J, Lin Y Y, Jackson T N, Nelson S F and Schlom D G 1997 *IEEE Electron Dev. Lett.* **18** 87

[20] Jurchescu O D, Baas J and Palstra T T M 2004 *Appl. Phys. Lett.* **84** 3061
[21] Zhang X and Wu J 2012 *Curr. Organ. Chem.* **16** 252
[22] Wakayama Y, Hayakawa R and Seo H S 2014 *Sci. Technol. Adv. Mater.* **15** 024202
[23] Li T, Ruden P P, Campbell I H and Smith D L 2003 *J. Appl. Phys.* **93** 4017
[24] Ou-Yang W, Weis M, Taguchi D Chen X Y, Manaka T and Iwamoto M 2010 *J. Appl. Phys.* **107** 124506
[25] Ishikawa Y, Wada Y and Toyabe T 2010 *J. Appl. Phys.* **107** 053709
[26] Melzer K, Brändlein M, Popescu B, Popescu D, Lugli P and Scarpa G 2014 *Faraday Discuss* **174** 399
[27] Wang L and Beljonne D 2013 *J. Chem. Phys.* **139** 064316
[28] Sharifi M J and Bazyar 2011 *ACEEE Int. J. Control Sys. Instrum.* **02** 18
[29] Gill W D 1972 *J. Appl. Phys.* **43** 5033
[30] W. Brütting 2005 *Physics of Organic Semiconductors* (Weinheim: Wiley-VCH) p. 1
[31] Noda K, Wada Y and Toyabe T. 2014 *Jpn. J. Appl. Phys.* **53** 06JH02
[32] Matsumura M, Akai T, Saito M and Kimura T 1996 *J. Appl. Phys.* **79** 264
[33] Parker I D 1994 *J. Appl. Phys.* **75** 1656
[34] Zhen L, Guan W, Shang L, Liu M and Liu G 2008 *J. Phys. D: Appl. Phys.* **41** 135111
[35] Wang W and Ma D G 2010 *Chin. Phys. Lett.* **27** 018503
[36] Schroeder P G, France C B, Park J B and Parkinson B A 2002 *J. Appl. Phys.* **91** 3010
[37] Ying J, Han J, Xiang L, Wang W and Xie W F 2015 *Curr. Appl. Phys.* **15** 770
[38] Lee C, Hou T H and Kan C C 2005 *IEEE Trans. Electron Dev.* **52** 2697
[39] Han J, Wang W, Ying J and Xie W F 2014 *Appl. Phys. Lett.* **104** 013302