A G-band terahertz monolithic integrated amplifier in 0.5-μm InP double heterojunction bipolar transistor technology*

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(Received 14 December 2015; revised manuscript received 18 January 2016; published online 31 March 2016)

Design and characterization of a G-band (140–220 GHz) terahertz monolithic integrated circuit (TMIC) amplifier in eight-stage common-emitter topology are performed based on the 0.5-μm InGaAs/InP double heterojunction bipolar transistor (DHBT). An inverted microstrip line is implemented to avoid a parasitic mode between the ground plane and the InP substrate. The on-wafer measurement results show that peak gains are 20 dB at 140 GHz and more than 15-dB gain at 140–190 GHz respectively. The saturation output powers are −2.688 dBm at 210 GHz and −2.88 dBm at 220 GHz, respectively. It is the first report on an amplifier operating at the G-band based on 0.5-μm InP DHBT technology. Compared with the hybrid integrated circuit of vacuum electronic devices, the monolithic integrated circuit has the advantage of reliability and consistency. This TMIC demonstrates the feasibility of the 0.5-μm InGaAs/InP DHBT amplifier in G-band frequencies applications.

Keywords: terahertz amplifier, InP double heterojunction bipolar transistor, inverted microstrip line, monolithic integrated circuit

PACS: 84.30.Le, 07.57.–c, 85.30.De **DOI:** 10.1088/1674-1056/25/5/058401

1. Introduction

In the terahertz (0.1–10 THz) field, the vacuum electronic device (VED),[1] quantum cascade laser (QCL),[2–4] and solid state device[5,6] have received a great deal of attention. Benefiting from the robust performance, low operation voltage, room temperature operation and easy mass-production, the solid state devices have progressed very rapidly in the last several years. InP DHBT is a promising technology in the terahertz solid state device field.[7,8] Recently massive G-band (140–220 GHz) and H-band (220–325 GHz) amplifiers were presented based on 250-nm or 150-nm InP DHBT technology.[9–12] InP solid state devices show splendid prospects in imaging, radar, spectroscopy, and communication systems operating in the terahertz frequency band. Scaling the emitter length under 0.25 μm requires complex fabrication procedures such as e-beam lithography, refractory contact metal deposition, etc. Meanwhile, the 0.5-μm InGaAs/InP DHBT process just needs ordinary optical lithography, wet-etching and deposition technology. However, a larger emitter length leads to a lower cut-off frequency (f_t) and a lower power gain in a terahertz band. Therefore, the critical problem of using the 0.5-μm processing in a terahertz band is the maximum utilization of the gain resource. A precise modeling and designing method should be utilized to achieve the goal. In this paper, we present a G-band amplifier based on the 0.5-μm InGaAs/InP DHBT process. The amplifier was designed in the University of Electronic Science and Technology of China (UESTC) and made in the Nanjing Electronic Devices Institute (NEDI). The amplifier was designed with a modified Agilent-HBT model and Keysight full-wave simulation software advance design system (ADS) momentum. Measurements demonstrate a more than 15-dB gain at 140–190 GHz and a peak gain of 20 dB at 140 GHz. The saturation output powers are −2.688 dBm at 210 GHz and −2.88 dBm at 220 GHz, respectively. This is the first report on an amplifier operating in the G-band based on 0.5-μm InP DHBT technology. This MMIC demonstrates the feasibility of 0.5-μm InGaAs/InP DHBT amplifiers operating at G-band frequencies.

2. Device fabrication and process

The epitaxial layer of the DHBT is grown on a 3-inch semi-insulating InP substrate by using molecular-beam epitaxy (MBE). The layer structure is shown in Table 1.[13] A composite collector layer including a 200-nm Si-doped n^+ InGaAs sub-collector layer, a 150-nm n-type InP layer, a 50-nm δ-doping InP layer, and a 30-nm InGaAs set-back layer, is grown. The composite collector layer is designed to eliminate the conduction band spike at the B–C interface and to minimize the collector current blocking effect.[14] A 35-nm p^+ InGaAs base layer with a carbon doping level of 5×10^{19} is grown to achieve a small base sheet resistance and contact resistivity. Finally, a 200-nm n^+ InP emitter and 200-nm n^+

*Project supported by the National Natural Science Foundation of China (Grant No. 61501091) and the Fundamental Research Funds for the Central Universities of Ministry of Education of China (Grant Nos. ZYGX2014J003 and ZYGX2013J020).

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InGaAs cap layer are grown.

After material epitaxy, geometry is determined by using i-line stepper lithography. Ti/Pt/Au is used as the emitter contact. Three mesas are formed through selective wet-etching, and the etching time is accurately controlled to prevent over etching. The base contact metal is determined by using a self-aligned technique. Pt/Ti/Pt/Au is used as the base contact, for Pt can penetrate through the surface oxide layer of the InGaAs base, which is of benefit to achieving a low base contact resistivity.[15] All metals are formed through deposition and the lift-off technique. After metal posts and device isolation processes, BCB is used as a passivation and planarization layer. Finally, a metal pad is formed, and the device process is finished. DC characteristics are measured by using an Agilent semiconductor parameter analyzer as shown in Fig. 1.

Table 1. Layer structure of the InGaAs/InP DHBT.

Layers	Material	Thickness/nm	Dopant
Emitter contact	InGaAs	200	Si
Emitter	InP	200	Si
Base	InGaAs	35	C
Set-back	InGaAs	30	Si
δ-doping	InP	50	Si
Collector	InP	150	Si
Collector contact	InGaAs	50	Si
Sub-collector	InP	200	Si
Etch-stop	InGaAs	10	ud
InP substrate			S. I.

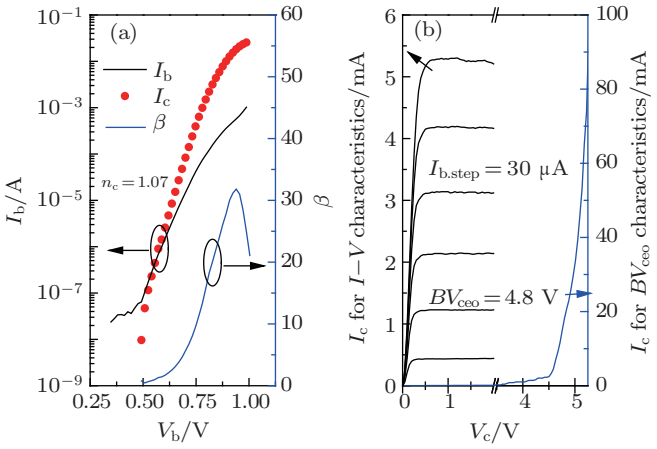


Fig. 1. (color online) DC characteristics of the InGaAs/InP DHBT: (a) gammel plot I_b (left) and current gain β (right) at $V_{cb} = 0$ V; (b) I–V characteristics (left) and BV_{CEO} measurement (right).

The area of the emitter contact is 0.5 μm×5 μm. Transmission line model (TLM) measurements show a base contact resistivity of $\rho_{bc} = 3.9\ \Omega \cdot \mu m^2$ and base sheet resistance of $R_{sh,b} = 737\ \Omega$/square, giving an estimated base resistance of 18.9 Ω. MMIC fabrication includes 2-levels of interconnect metal, metal 1 (MET1) and metal 2 (MET2), separated by 3.0-μm BCB ($\varepsilon_r = 2.7$). MIM capacitors (SiN_x, 0.3 fF/μm^2) are formed between the collector metal (CM) and capacitor metal (CAPM), and 250-Ω/square thin-film resistors (TFRes) are available. The cross section of this process is shown in Fig. 2.

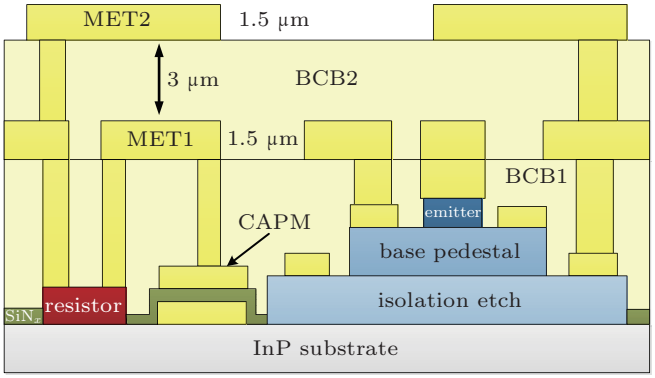


Fig. 2. (color online) Cross-section of the InP DHBT process with interconnect layers formed by BCB.

Two kinds of microstrip line are available in this process. The thin-film microstrip line (MET1 serves as the ground, and MET2 as the signal line), and inverted microstrip line (MET2 is used as the ground, and MET1 as the signal line).[16] The thin-film microstrip is close to the traditional microstrip, but the "ground" (MET1) floats on 620-μm InP substrate. In order to connect the MET1 ground to the real ground, bonding wire is necessary, which will introduce an inductive parasitic effect and deteriorates the chip performance. What is more, the large MET1 ground plane and thick InP substrate will generate a parasitic mode at high frequency such as dielectric waveguide mode or microstrip mode under MET1. On the contrary, the electromagnetic mode of the inverted microstrip is simple. No dielectric waveguide mode exists above the ground metal MET2, for the dielectric constant of air is much lower than those of the BCB and InP. The inverted microstrip configuration is convenient to the flip-chip package which requires no bonding wire, thus a large continuous ground plane is guaranteed. Therefore, the inverted microstrip has advantages in system level integration.[17]

3. Device characterizations and amplifier design

DC-67 GHz measurements are carried out after performing an off-wafer line-reflect-reflect-match (LRRM) calibration on an Agilent N5247A programmable network analyzer (PNA). The pad frame parasitic parameters are de-embedded from the measured s-parameters by the open-short method. 75–110 GHz and 140–220 GHz RF device measurements are carried out after performing an on-wafer line-reflect-line (LRL) calibration, where the two ports reference planes after calibration are set to be at the edge of the device. The on-wafer calibration kit is designed and fabricated on InP wafer.

The large signal model we proposed in Ref. [18] is utilized here for device modeling and designing. Based on the

Agilent-HBT model, the DC current function is modified to correct the heterojunction effect. The current gain β is simulated more precisely in the low current region. An RF current branch is added into an equivalent circuit to fit the non-thermal dispersion effect. The Agilent HBT model parameters are extracted from measurements at DC -67 GHz, and slightly adjusted according to high frequency measurements. The fitting results of max stable gain and max available gain (MSG&MAG) of HBT are shown in Fig. 3 under $V_c = 1.5$ V and $I_b = 100$–500 μA in steps of 100 μA. When the HBT is biased at $V_c = 1.5$ V and $I_b = 350$ μA, the highest unity-gain cutoff frequency (f_t) and power-gain cutoff frequency (f_{max}) are achieved. The -20 dB/decade extrapolation of the measured data shows that f_t and f_{max} at this bias are 350 GHz and 532 GHz, respectively.

The design presented in this paper uses an inverted microstrip line. The inverse microstrip simulated loss is 3.5 dB/mm at 300 GHz. The realizable characteristic impedances range from approximately 11.5 Ω to 53.2 Ω with signal line widths ranging from 3 μm to 30 μm.

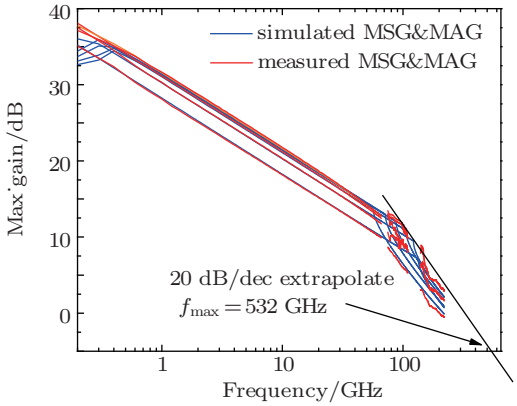


Fig. 3. Simulated (green line) and measured (red line) MSG&MAG of 0.5-μm emitter length InGaAs/InP DHBT. Measurements are carried out in three bands: 200 MHz–67 GHz, 75 GHz–110 GHz, and 140 GHz–220 GHz. Here, $V_c = 1.5$ V and $I_b = 100$–500 μA in steps of 100 μA.

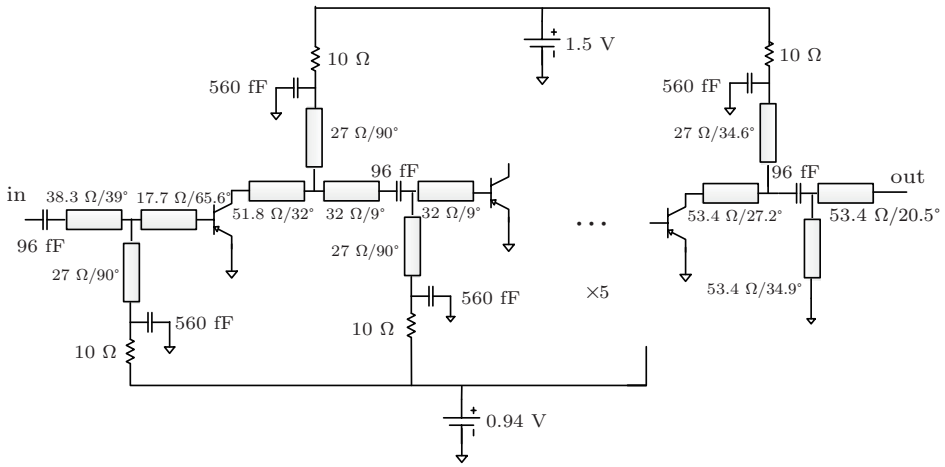


Fig. 4. Schematic of the eight-stage amplifier. The electric length and characteristic impedance are calculated at 220 GHz.

The amplifiers are primarily optimized for high gain with adequate match between input and output. Under the simultaneous match condition, the optimum source impedance and load impedance can be calculated to be $Z_{source} = 9.2 + j3.6$ Ω, $Z_{load} = 12.5 + j44.3$ Ω respectively. The matching networks are designed to obtain complex conjugate match of the input and output impedances of the device over a wide band width. To achieve a sufficient amount of gain, eight stages of HBT are cascaded. Inter-stage match also takes a complex conjugate match design. A 96-fF MIM capacitor for DC-blocking is inserted between stages. The capacitor and its parasitic effect are taken into account as a part of the matching network. The schematic is shown in Fig. 4. Each match network introduces 1.75 dB insertion loss due to the skin effect of metal and semi-insulate substrate loss. Mismatch loss also exists for the deviation of model and EM software simulation.

The DC bias is supplied through a long stub with a 560 fF decoupling capacitor. A 10 Ω series resistor is utilized to suppress low-frequency oscillation. All bias lines for the eight stages are tied together to minimize dc bond pads. The layout of the circuit is shown in Fig. 5. The total chip area is 899 μm×1171 μm.

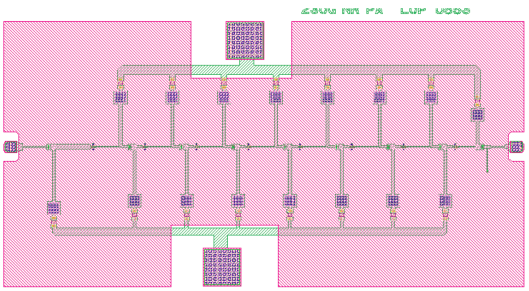


Fig. 5. Layout of the amplifier MMIC employing inverted microstrip wiring.

4. Results and discussion

The amplifier MMIC is first tested by using the cascade probe station, WR-5 waveguide RF probes, DC probe, and WR-5 waveguide frequency extenders. The chip optical micrograph is shown in Fig. 6. It is clear that in inverted microstrip topology, the signal line is shielded by the ground.

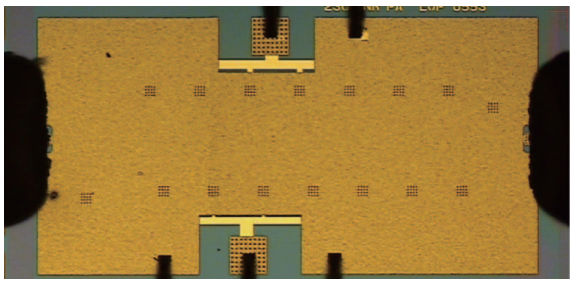


Fig. 6. (color online) The micrograph of the amplifier MMIC with RF and DC test probe.

The small-signal measurements are performed with $V_c = 1.5$ V, $I_c = 80$ mA and $V_b = 0.94$ V, $I_b = 3.2$ mA. Small-signal measurements indicate a flat gain feature with more than 15 dB at the 140–190 GHz band. At 220 GHz, the amplifier still has 6.72-dB gain. The 3-dB band width of gain is 140–200.5 GHz. Figure 7 displays the comparison between simulation and measurement. Some deviations between simulated and measured scatter parameters are observed. This can be explained from several aspects. Firstly, the process fluctuation, the model based on the previous tap-outed HBT and the HBT performance change at this batch. Secondly, EM-simulation deviation, commercial EM-simulation software cannot precisely describe the complex electromagnetic environment which contains both the electrically large structure (such as long metal transmission line) and electrically small (via, short stubs) structure. So designs with the widely fluctuating process, statistical model and tolerance analysis are necessary. EM-simulation software should be optimized based on measurement in specified frequency band.

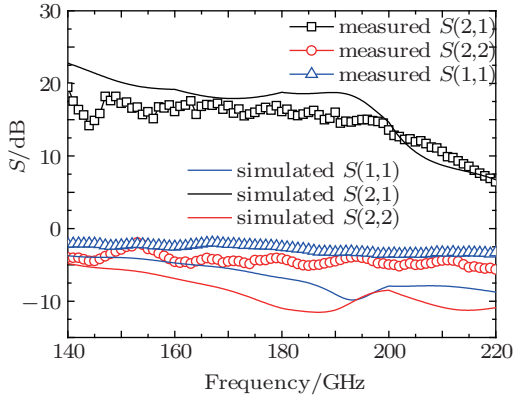


Fig. 7. (color online) Simulated (line) and measured (symbol) scatter parameters (S) of the amplifier.

Next, output power is measured by using the setup shown in Fig. 8. The input signal from an Agilent signal generator is converted with a diode 6× multiplier developed by NEDI. Driven by the signal generator, the multiplier saturation output power is around 6 dBm at 210–220 GHz. Careful calibration is taken to obtain the real input and output power of the amplifier as follows.

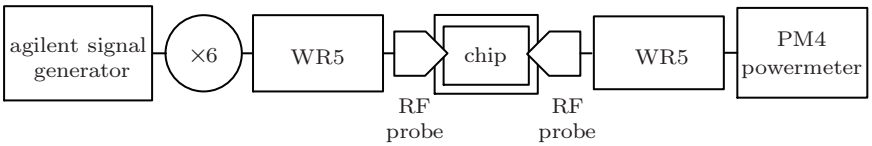


Fig. 8. Test setup for on-wafer output power measurement.

(I) Connect the power meter directly to the output of the multiplier, record each multiplier output power P_{out1} corresponding to each Agilent synthesizer output power.

(II) Insert the WR-5 waveguide, RF probe and on-chip through a kit between the multiplier and power meter, and record each WR-5 output power P_{out2}. Considering the symmetric, the insertion loss of one side waveguide and probe can be calculated as $\mathrm{IL} = (P_{out1} - P_{out2})/2$.

(III) The real input power of amplifier $P_{in} = P_{out1} - \mathrm{IL}$, and the real output power of amplifier $P_{out} = P_{meter} + \mathrm{IL}$, where the P_{meter} is the power level read on the power meter directly when the amplifier is under test.

(IV) The power gain $P_{gain} = P_{out} - P_{in}$.

The output measurement results can be found in Figs. 9 and 10. The saturation output powers are −2.688 dBm at 210 GHz and −2.88 dBm at 220 GHz driven by 2.5 dBm input power, respectively. The measurement and simulation fit to each other well, indicating that the model can describe the HBT current–voltage relation (I–V curve) and nonlinear junction capacitance precisely. The power gain drops down to below 0 dB, when input power exceeds −3 dBm. The reason is that at high frequency, the available gain of HBT is limited. Measurement indicates that the MAG at 210 GHz is 5.45 dB. Taking the mismatch loss and insertion loss of the match network into consideration, only 1-dB gain is left for each stage at 210 GHz. Driven by the large signal, HBT gain decreases, leading to a negative gain for each stage and the whole amplifier. In small signal conditions (input power = −20 dBm–

10 dBm), the amplifier demonstrates a linear power gain and output power feature, suitable for driving the amplifier or a first stage small signal amplifier of the terahertz transceiver front end.

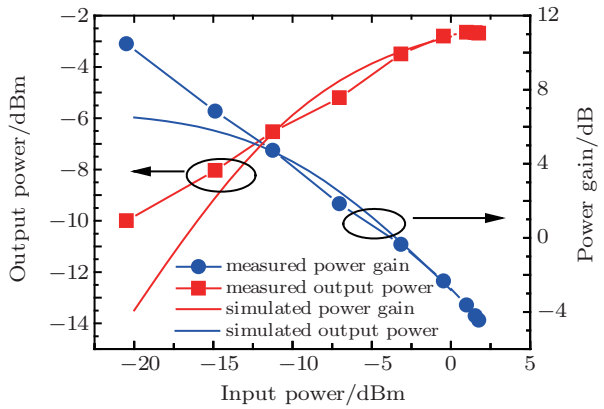


Fig. 9. (color online) Simulated (line) and measured (dotted line) power gain and output power of the amplifier at 210 GHz.

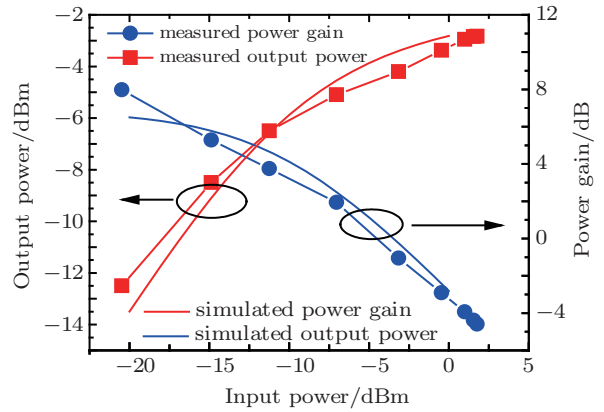


Fig. 10. (color online) Simulated (line) and measured (dotted line) power gain and output power of the amplifier at 220 GHz.

5. Conclusion and perspectives

In this work, a G-band terahertz monolithic integrated amplifier is designed and fabricated based on 0.5-μm InP DHBT technology. The measured results show a flat gain feature with more than 15 dB at the 140–190 GHz band. The 3-dB band width of gain is 140–200.5 GHz. The saturation output powers are −2.688 dBm at 210 GHz and −2.88 dBm at 220 GHz respectively. Benefiting from the robust performance, low operation voltage, room temperature operation and easy mass-production, the solid state TMIC amplifier is suitable for driving an amplifier or a first stage small signal amplifier of the terahertz transceiver front end. The simulated and measured results show a similar trend while some deviation is also observed. A more precise modeling method of the terahertz device should be developed, and the statics model is important for the tolerant analysis. High-efficiency terahertz on-chip power combining technology is also important for the development of future solid state high-power devices.

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