Developing Josephson junction array chips for microvolt applications*

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Josephson junction array chips for microvolt applications have been designed and fabricated. A voltage step as small as 1 μV has been observed for a single junction in the array when it is driven by 483.59 MHz microwave. By selecting different parts of the array, it can output a voltage from 1 μV to 256 μV. The flat region of the voltage steps is over 200 μA. This kind of array is useful for potential microvolt applications.

Keywords: Josephson junction arrays, voltage standard, niobium

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1. Introduction

The most precise voltage calibration system used today is the Josephson voltage standard system based on the integrated Josephson junction arrays. If a Josephson junction is driven at frequency f, then its I–V curve will develop regions of constant voltage at the values of $nhf/2e$, where n is an integer, e is the elementary charge, and h is the Planck constant. Recently, Josephson junction arrays for 10 V programmable Josephson voltage standard[1–3] and 1 V pulse driven Josephson voltage standard have been successfully developed.[4,5] The minimum voltage resolution of these voltage standards is about 25 μV with one junction driven at 12 GHz. Generally, such resolution can meet most of the demands of the digital voltmeter calibration. However, it is not adequate for calibrating the instruments with a work range below 20 μV, for example, the calibration of medical instruments.[6] Several groups are now developing the automated microvolt Josephson voltage system which is capable of providing accurate voltages of several microvolts[7] or nanovolts.[8] The current system in the National Institute of Metrology (NIM) is based on two programmable Josephson superconductor–insulator–normal metal–insulator–superconductor (SINIS) arrays on two voltage standard chips. The output voltage difference between the two arrays can be expressed as $\Delta V = Mh/2e(f_1 - f_2)$, where M is the number of the biased junctions, and f_1 and f_2 are the microwave frequencies of the two arrays, respectively. By choosing proper f_1 and f_2, the microvolt can be obtained. The system requires two microwave sources and the two sources have to be high-frequency (about 73 GHz) ones, which are not only expensive but also inconvenient. To solve this problem, a Josephson junction array chip based on superconductor–normal metal–superconductor (SNS) Josephson junctions which can work at MHz is designed. Each Josephson junction array on the chip is composed of 9 sections containing different numbers of junctions from 1 to 256, and the total number of junctions is 511. With a single array working at 483.59 MHz, it can output a voltage from 1 μV to 256 μV. So this design is simplified compared to the previous one and becomes much more economically efficient since only one low frequency microwave source is required. It can be used for DC microvolt calibration and also for AC microvolt calibration with a programmable method. This paper will focus on developing this kind of Josephson junction array chip for the potential applications of microvolt calibration.

2. Experiment

2.1. Design

The Josephson junctions are designed to be located in the middle line of a co-planar wave guide (CPW). The structure of the CPW is optimized according to the simulation results by using HFSS software. The array has 9 sections and each section has $n = 2^i$ number of junctions, $i = 0, 1, 2, 4, \ldots, 8$, as shown in Fig. 1. The total number of junctions in one array is 511. The output voltage can be expressed as $V_n = nV_1 = nhf/2e$. The microwave frequency used for this experiment is 483.59 MHz. So for a single junction, the output voltage V_1 can be about 1 μV. The largest part can output a voltage of 256 μV. The size of each junction is 7 μm × 7 μm. The array is in a straight line and its length is about 0.8 cm.

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2.2. Fabrication

Due to the advantages of the Nb/Nb$_x$Si$_{1-x}$/Nb Josephson junction, including easily tunable electrical parameters and etching properties, it is selected for this experiment.[9] Nb/Nb$_x$Si$_{1-x}$/Nb sandwich layers are *in-situ* deposited by DC magnetron sputtering in a chamber. There are three targets facing up to the substrate holder in the middle of the chamber, including two Nb targets and one Si target. The base pressure is about 1×10^{-8} Torr. The substrate rotation and back water cooling are available in this sputtering system.

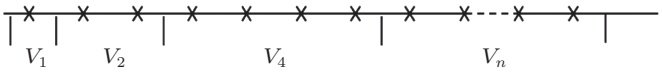


Fig. 1. Diagrammatic sketch of one Josephson junction array.

The Nb film is deposited with a sputtering power of 500 W, corresponding to a deposition rate of 0.75 nm/s. The Nb film with compressive stress of about 100 MPa and critical temperature of 9.1 K is obtained. The Nb$_x$Si$_{1-x}$ film is co-sputtered by using another Nb target and the Si target together, the Si sputtering power is 248 W and the Nb sputtering power is 37 W, which lead to a deposition rate of 0.17 nm/s. The thicknesses of the trilayer are 300 nm, 35 nm, and 200 nm, respectively.

The sample is patterned by using photo lithography for all etching and liftoff processes. The top Nb layer and the Nb$_x$Si$_{1-x}$ barrier layer are etched to have steep edges by using reactive ion etching (RIE) and inductively-coupled-plasma (ICP) etching processes with a mixture gas of SF_6 and C_4F_8.[10] A 400-nm thick SiO_2 film is used as the insulating layer of the junction and it is deposited by using a plasma enhanced chemical vapour deposition (PECVD) system. RIE with ICP is also used for Nb base electrode etching using CF_4 and O_2 gas mixture and SiO_2 etching using CHF_3 and O_2 gas mixture. An *in-situ* cleaning process by DC-biased rf etching is applied before depositing the 500-nm thick Nb wiring electrode, which enables a good contact between the upper Nb layer and the wiring electrode. For Nb wiring layer etching, only RIE is used with SF_6. The resistance layer PdAu is deposited for microwave absorption by electron beam evaporation. Then the liftoff process for the PdAu film is performed. More details about the fabrication process have been provided in our previous paper.[11] Figure 2 shows the photo of part of the Josephson junction array chips. There is a straight CPW line and the Josephson junction array is located in the middle of the CPW. The array is divided into several parts which can be seen in the picture.

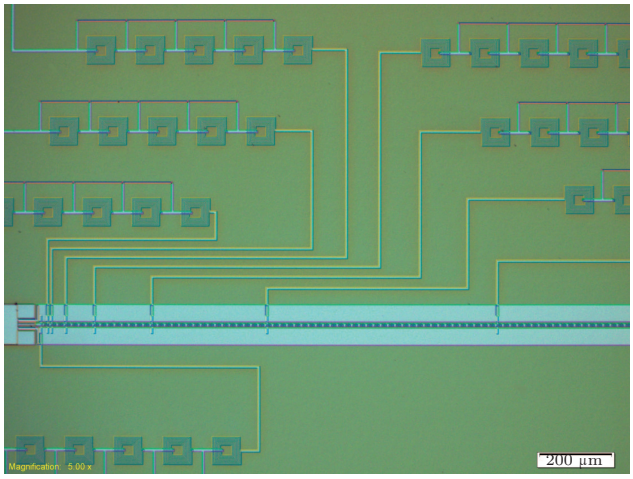


Fig. 2. (color online) Part of the Josephson junction array chips.

2.3. Measurement

The sample is mounted onto a red cooper stage and connected to a printed circuit board by using aluminum silicide bonding wires. The stage is connected to the bottom of a probe stick which can be put into a helium Dewar. So the sample can be measured in the liquid helium at 4.2 K. Since the smallest voltage step generated by this sample is only 1 μV, a precise measurement system is necessary. A DC current source is used to sweep the sample by increasing the current step by step. An Agilent 34420A is used to measure the voltage across the sample. It is found that without shielding, the critical current and the voltage step are drifting all the time. When a lead shielding is used, the characteristics of the sample become stable.

Figure 3 shows the DC *I*–*V* characteristics for different parts of the array containing different numbers of junctions. The critical current I_c for each segment of the array is uniform. So each junction has a critical current $I_c = 2.1$ mA and a characteristic voltage $V_c = I_cR_n = 13.4$ μV, where R_n is the normal junction resistance.

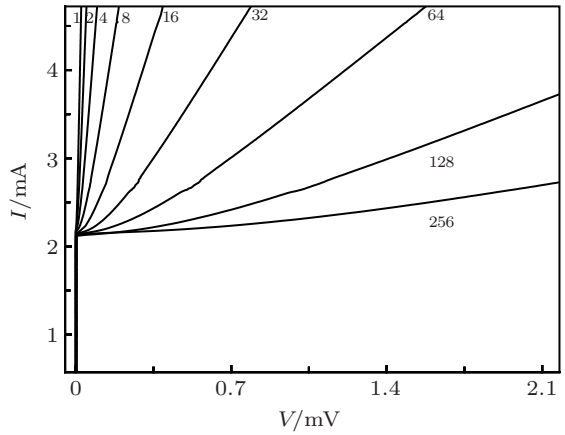


Fig. 3. The DC *I*–*V* characteristics for different numbers of Josephson junctions in series. The number of junctions is given in the figure.

Although the characteristic voltage V_c is much larger than 1 μV, we also try to use the array at 483.59 MHz. For a single

junction, it will develop constant voltage steps corresponding to integer times of one microvolt as shown in Fig. 4. We can see that the flat region of the first step is over 200 μA as denoted in the insert. According to the reports from other groups, it is useful for voltage calibrations.[12]

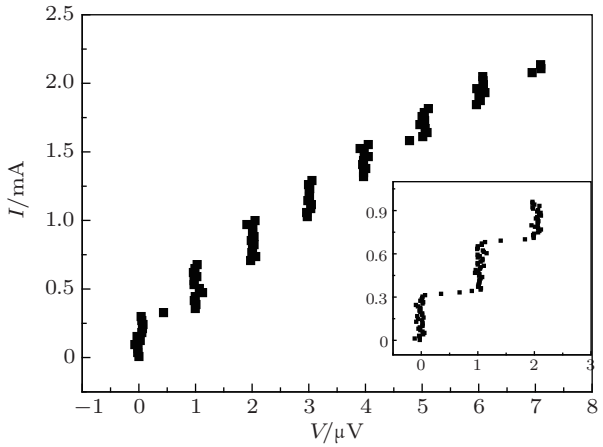


Fig. 4. The *I*–*V* characteristics for a single Josephson junction driven by 483.59 MHz microwave. Insert is the detail of the first step, showing an over 200 μA flat region.

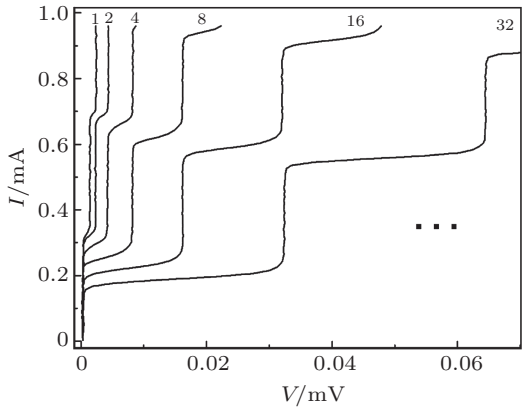


Fig. 5. The *I*–*V* characteristics for different parts of the Josephson junction array driven by 483.59 MHz microwave.

For different parts of the array, the *I*–*V* characteristics with microwave radiation are shown in Fig. 5. In order to have a good view of different parts of the array, only the measuring results of six segments are displayed in the figure. For the first step, all of the segments have a flat current region of more than 200 μA, which means that it is useful for microvolt application. By selecting different parts of the array, it can output a microvolt voltage from 1 μV to 256 μV. For the second step, the flat current region is also larger than 200 μA. So the array not only works at the first step, but also works at the second step.

3. Conclusion

For microvolt applications, a Josephson junction array chip has been designed and fabricated. The DC and AC characteristics have been measured. The results demonstrate good uniform characteristics of the junctions. A 1 μV step with over 200 μA flat region has been observed. By selecting different parts of the array, it can output a quantum voltage from 1 μV to 256 μV. It is useful for potential applications, for example, calibrations of instruments working in the microvolt range or combining with PJVS to output more precisely AC voltage waveforms. In the future, we will adjust the barrier parameters of the junctions to obtain a wider voltage step of about 1 mA at several hundred MHz.

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