Ultra-low specific on-resistance high-voltage vertical double diffusion metal–oxide–semiconductor field-effect transistor with continuous electron accumulation layer*

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A new ultra-low specific on-resistance ($R_{on,sp}$) vertical double diffusion metal–oxide–semiconductor field-effect transistor (VDMOS) with continuous electron accumulation (CEA) layer, denoted as CEA-VDMOS, is proposed and its new current transport mechanism is investigated. It features a trench gate directly extended to the drain, which includes two PN junctions. In on-state, the electron accumulation layers are formed along the sides of the extended gate and introduce two continuous low-resistance current paths from the source to the drain in a cell pitch. This mechanism not only dramatically reduces the $R_{on,sp}$ but also makes the $R_{on,sp}$ almost independent of the n-pillar doping concentration (N_n). In off-state, the depletion between the n-pillar and p-pillar within the extended trench gate increases the N_n, and further reduces the $R_{on,sp}$. Especially, the two PN junctions within the trench gate support a high gate–drain voltage in the off-state and on-state, respectively. However, the extended gate increases the gate capacitance and thus weakens the dynamic performance to some extent. Therefore, the CEA-VDMOS is more suitable for low and medium frequencies application. Simulation indicates that the CEA-VDMOS reduces the $R_{on,sp}$ by 80% compared with the conventional super-junction VDMOS (CSJ-VDMOS) at the same high breakdown voltage (BV).

Keywords: electron accumulation layer, PN junctions, low specific on-resistance, high breakdown voltage

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1. Introduction

The super-junction (SJ) VDMOS has attracted a great deal of attention owing to its improvement on the specific on-resistance ($R_{on,sp}$) and the better trade-off between the $R_{on,sp}$ and breakdown voltage (BV).[1–8] However, the $R_{on,sp}$ is still determined by the doping concentration of the drift region. For high voltage SJ VDMOS, narrowing the width of the pillars is a good choice to improve the N_n and reduce the $R_{on,sp}$, but the fabrication is hard to realize. A vertical extended gate is used to form a major accumulation layer, thus reducing the $R_{on,sp}$.[9,10] Nevertheless, the peak electric field at the bottom of the extended gate causes a premature breakdown, thus limiting the BV. In Refs. [11] and [12], a gradient oxide layer between the extended gate and drift is adopted to modulate the drift electric field distribution. The BV is thus improved to some extent. Unfortunately, the peak electric field still limits the application scope below 200 V and the gradient oxide layer is fairly difficult to fabricate.

In this paper, a novel high voltage ultra-low $R_{on,sp}$ VDMOS with continuous electron accumulation layer is proposed. It is characterized by an extended gate and two PN junctions in series within the extended gate. Owing to the electron accumulation layer in the on-state, the $R_{on,sp}$ is reduced dramatically and almost independent of n-pillar doping concentration. Furthermore, the two PN junctions within the trench gate support a high gate-drain voltage in the off-state and on-state, respectively. The 800 V-class BV is obtained. It not only breaks through the silicon limit of conventional VDMOS, but also shows superiority to the trench gate SJ VDMOS.

2. Device structure and mechanism

Figure 1 shows the structures and operation mechanisms of the CEA-VDMOS and CSJ-VDMOS. As figure 1(a) shows, the trench gate extends to the drain and includes two PN junctions. In the extended gate, the p-pillar is in touch with the P^+ gate contact region at the top. The P-region is contacted with the drain electrode at the bottom. The N^+ region is between the p-pillar and the P-region. Therefore, the D_1 and D_2 junctions are formed. The D_1 and D_2 are reverse-biased to sustain the drain–gate voltage in the off-state and the on-state respectively, maintaining a high BV. L_d is the depth of the n-pillar. W and N_n are the width and the doping concentration of the n-pillar. The width of p-pillar is $2W$. T_{fox} is the thickness of

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the gate oxide. L_{nn} and L_{pp} are the depths of the N^+ region and p-region in the trench, respectively. N_{nn} and N_{pp} are the doping concentrations of the N^+ region and P-region in the trench, respectively.

In the on-state, at $V_{GS} > V_{th}$, $V_{GD} > 0$, and $V_{DS} > 0$, the D_2 is reverse-biased (the N^+ region is not fully depleted) to sustain the V_{GD} (for N-channel VDMOS, usually, $V_{GD} < 15$ V). Owing to the equivalent metal–insulator–semiconductor (MIS) structure consisting of the p-pillar, gate oxide and n-pillar, as is marked with the red dashed rectangle in Fig. 1(a), two high-concentration electron accumulation layers are formed along the two oxide/n-pillar interfaces. Figure 1(b) shows the accumulation caused by the MIS structure. Most of the current flows through the accumulation layers instead of the neutral n-pillar, leading to continuous ultra-low on-resistance paths from the source to drain. Therefore, the $R_{on,sp}$ is reduced significantly. Moreover, the $R_{on,sp}$ is almost independent of N_n. Figure 1(c) shows the depletion effect of the CEA-VDMOS in the off-state ($V_{DS} > 0$, $V_{GS} = 0$). In the off-state, on the one hand, owing to the fact that the p-pillar and n-pillar deplete each other through the MIS structure, the depleted p-pillar and n-pillar regions ensure a high BV of drain-source. On the other hand, owing to the fact that the N^+ region is not fully depleted, the reverse-biased D_1 sustains the high drain-gate voltage.

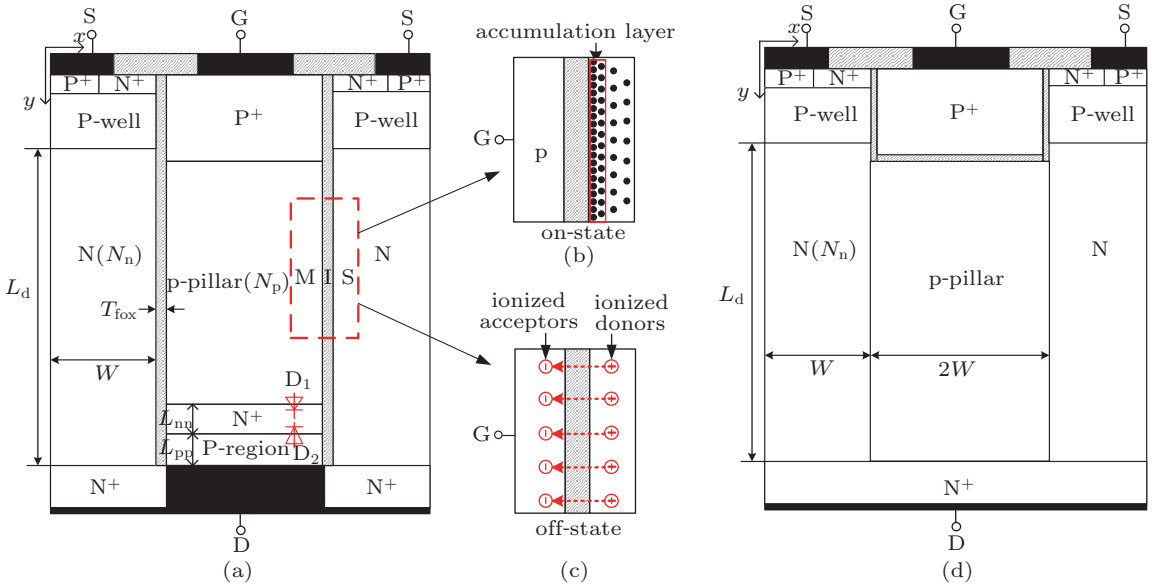


Fig. 1. (color online) (a) Schematic cross-sectional view of the proposed CEA-VDMOS, (b) accumulation effect in on-state ($V_{GS} > V_{th}$, $V_{GD} > 0$, $V_{DS} > 0$), (c) assisted-depletion effect on the n-pillar in the off-state, and (d) schematic cross-sectional view of the CSJ-VDMOS.

3. Results and discussion

In simulation, the same parameters of the CEA-VDMOS and CSJ-VDMOS (as shown in Fig. 1(d)) are set as follows: $L_d = 50$ μm, $W = 3$ μm, and $N_n = N_p = 3 \times 10^{15}$ cm^{-3}. For the CEA-VDMOS, $L_{nn} = 0.5$ μm, $L_{pp} = 1$ μm, $N_{nn} = 1 \times 10^{20}$ cm^{-3}, and $N_{pp} = 5 \times 10^{16}$ cm^{-3} are used in the simulation. The electric characteristics are investigated with simulator MEDICI and the physical models of CONSRH, AUGER, BGN, FLDMOB, SRFMOB, IMPACT.I and CCSMOB are mainly used, and the NEWTON solution method is adopted with 2 types of carriers.

Figure 2 shows the on-state electron concentrations and current densities in the n-pillar of the CEA-VDMOS and CSJ-VDMOS ($V_{GS} = 15$ V, $V_{DS} = 0.5$ V). For the CEA-VDMOS, the electron concentration accumulated at the n-pillar sidewalls is up to 5×10^{18} cm^{-3}, far higher than the doping concentration N_n of 3×10^{15} cm^{-3} as shown in Fig. 2(a). Therefore, approximately 76% of the current flows through the accumulation region and the maximum current density reaches up to 10^5 A·cm^{-2}, which is three orders of magnitude higher than that of the neutral n-pillar region as shown with the red solid line in Fig. 2(c). However, for the CSJ-VDMOS, the electron concentration along the p-pillar/n-pillar interface is far lower than N_n due to the lateral depletion effect as shown in Fig. 2(b). Therefore, the current density (as shown in Fig. 2(d)) decreases, thus limiting the decrease in the $R_{on,sp}$ of the CSJ-VDMOS. As a result, the CEA-VDMOS obtains an $R_{on,sp}$ of 4.13 mΩ·cm^2, much lower than the $R_{on,sp}$ of 20.8 mΩ·cm^2 for the CSJ-VDMOS.

The total on-state resistance of the CEA-VDMOS is composed of the accumulation layer resistance R_A and neutral n-pillar region resistance R_N in parallel. The R_A (Ω) is given as

$$R_A = \frac{L_d T_{fox}}{2\mu_A \varepsilon_0 \varepsilon_{ox} V_{GS}}. \quad (1)$$

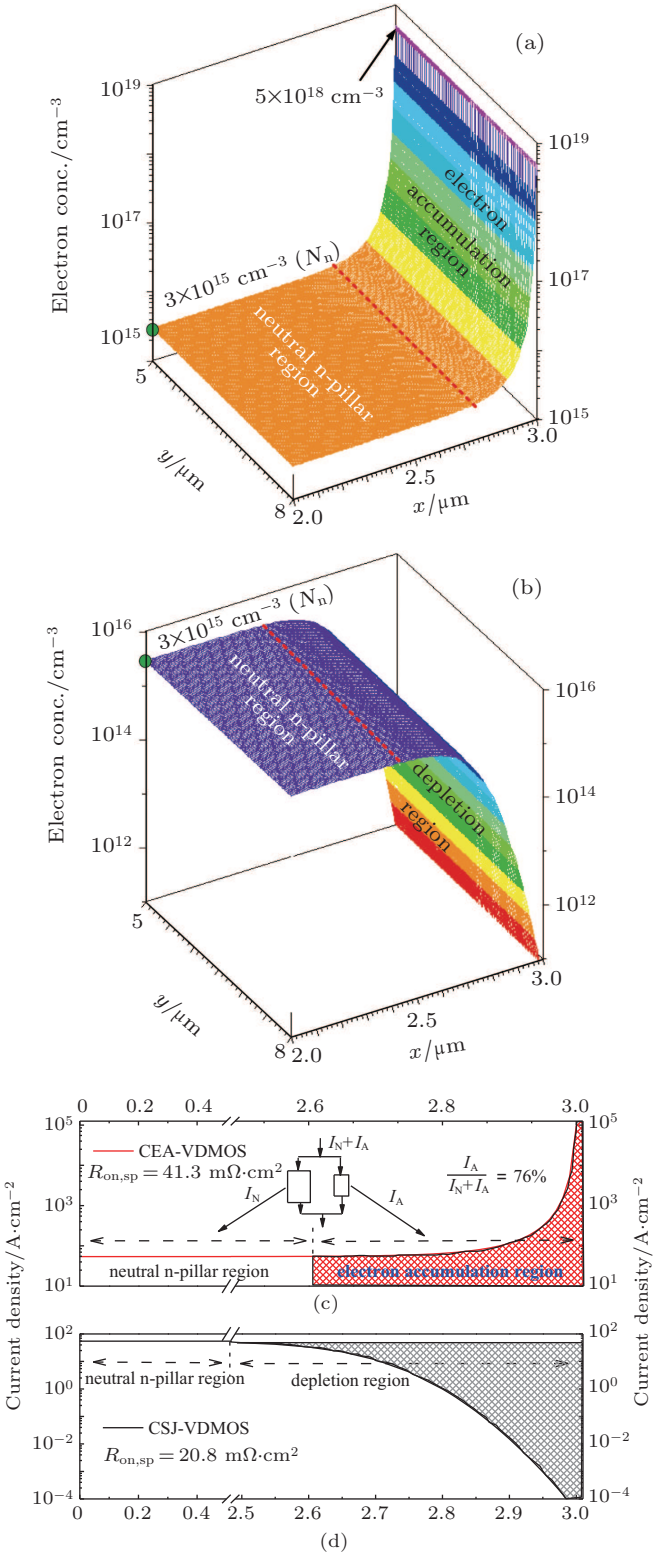


Fig. 2. (color online) In on-state, electron concentrations (conc.) of the (a) CEA-VDMOS and (b) CSJ-VDMOS, current density distributions of (c) CEA-VDMOS and (d) CSJ-VDMOS.

The R_N (Ω) is shown as follows:

$$R_N = \frac{L_d}{2q\mu_N N_n W}. \tag{2}$$

Then the total on-state resistance R is given as

$$R = R_A // R_N, \tag{3}$$

where q is the magnitude of electronic charge; μ_A and μ_N are the electron mobility in the accumulation layer and neutral n-pillar drift, respectively; ε_0 is the permittivity of the free space; ε_{ox} is the relative permittivity of the oxide layer; and V_{GS} is the gate voltage.

For the CEA-VDMOS, owing to the fact that the R_N and R_A are in parallel (from Eq. (3)) and R_A is smaller than R_N, R is mainly determined by R_A. Furthermore, the R_A is independent of N_n according to Eq. (1). Then the variation of the N_n just influences the R_N (Eq. (2)) and causes a little variation of $R_{on,sp}$. However, for the CSJ-VDMOS, the $R_{on,sp}$ is almost determined by N_n and sensitive to the variation of N_n.

Figure 3 shows the plots of $R_{on,sp}$ against N_n. As N_n decreases from 5×10^{15} cm^{-3} to 1.5×10^{15} cm^{-3}, $R_{on,sp}$ increases only 27% for the CEA-VDMOS, while it increases by 71% for the CSJ-VDMOS. It indicates that the $R_{on,sp}$ of the CSJ-VDMOS depends on N_n, while the CEA-VDMOS relieves the $R_{on,sp}$ from the strong restriction of N_n.

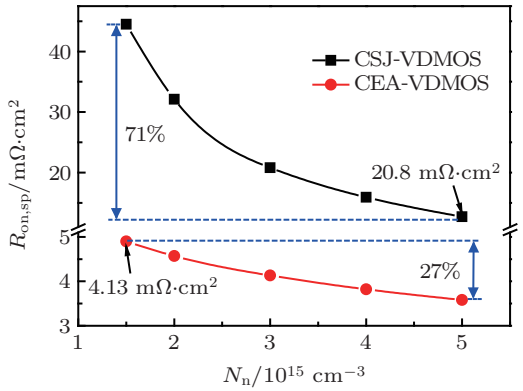


Fig. 3. (color online) Plots of $R_{on,sp}$ against N_n for the CEA-VDMOS and CSJ-VDMOS.

The I_A and I_N are the accumulation layer current and neutral n-pillar current, respectively, and η is defined as

$$\eta = \frac{I_A}{I_A + I_N}, \tag{4}$$

where I_A is mostly determined by the T_{fox} and V_{GS} according to Eq. (1), and I_N is mostly determined by the W and N_n according to Eq. (2).

Figure 4 shows the influences of W and T_{fox} on η and $R_{on,sp}$. For the CSJ-VDMOS, the increase of W reduces the optimized N_n and increases the cell pitch, resulting in the sharp increase of $R_{on,sp}$. For the CEA-VDMOS, the increase of W causes I_N to increase and η to decrease according to Eq. (1). Furthermore, owing to the most current flowing through the electron accumulation layers, i.e., $I_A \gg I_N$, the $R_{on,sp}$ does not strongly depend on N_n and then increases slightly with the increase of W. Additionally, for the CEA-VDMOS, a larger I_A is obtained for a thinner T_{fox} ($T_{fox} = 0.1$ μm) due to the enhanced accumulation effect and lowered R_A according to Eq. (1), which leads to a larger η (Eq. (1)) and smaller $R_{on,sp}$.

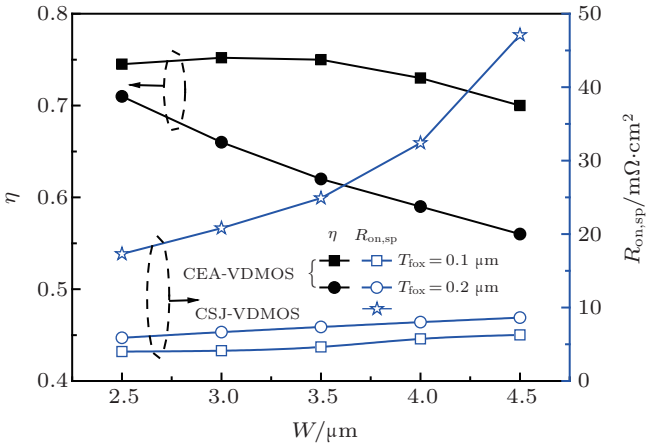


Fig. 4. (color online) Influence of the W and T_{fox} on the $R_{on,sp}$ and η.

Figure 5 shows the electric field distributions in the n-pillar (black short dashed line) and p-pillar (red line) for the CEA-VDMOS in the off-state. The electric field peak in the n-pillar is located at the p-well/n-pillar junction, and the electric field peak in the p-pillar is located at D_1 junction. Almost the same average electric field and electric field peak ensure the maximum breakdown voltage for the CEA-VDMOS.

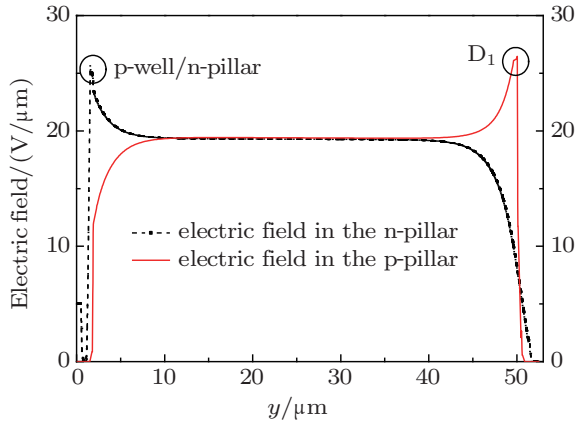


Fig. 5. (color online) Electric field distributions in the n-pillar and p-pillar for the CEA-VDMOS.

Figure 6 shows the plots of BV versus N_n for the CSJ-VDMOS and CEA-VDMOS. The simulation shows that the BV of the CEA-VDMOS is less sensitive to the variation of N_n than that of the CSJ-VDMOS. The N_n increases from 1.5×10^{15} cm^{-3} to 5×10^{15} cm^{-3}, the BV of the CEA-VDMOS decreases by only 39 V, while that of the CSJ-VDMOS decreases by 99 V. The equipotential contours at breakdown for both devices are shown by the figures in the insets. For the CSJ-VDMOS, the equipotential contours are narrowed at the bottom of the trench gate (circle A), where a high peak electric field is caused and the premature breakdown is prone to occur with the increase of N_n. However, for the CEA-VDMOS, the equipotential contours are uniform at circle B. By the way, the maximum BV of the CEA-VDMOS is a little lower than that of the CSJ-VDMOS, owing to the fact that the N^+ region in the trench stops the electric field prematurely, thus reducing the equivalent length of the voltage-sustaining region in the off-state for the CEA-VDMOS.

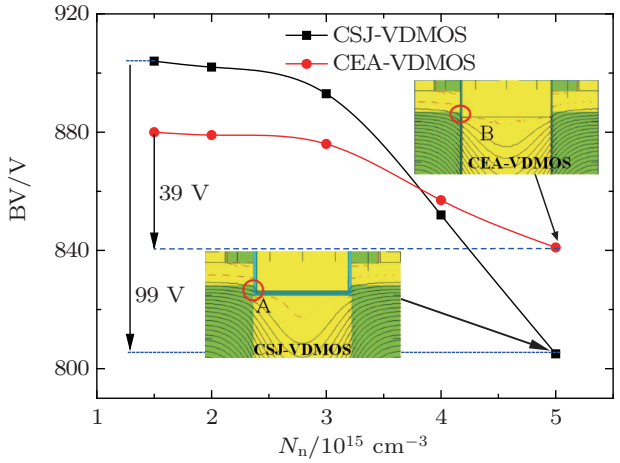


Fig. 6. (color online) Plots of BV versus N_n for the CSJ-VDMOS and CEA-VDMOS.

Figure 7 shows the comparison of switching characteristic between the CEA-VDMOS and the CSJ-VDMOS. From this figure, we can obtain that the $t_{on} = 0.8$ ns and $t_{off} = 93$ ns for the CEA-VDMOS as compared with $t_{on} = 1.2$ ns and $t_{off} = 50$ ns for the CSJ-VDMOS. The larger turn-off time for the CEA-VDMOS than that of the CSJ-VDMOS is mainly caused by a larger gate capacitance for the CEA-VDMOS. Considering the ultra-low $R_{on,sp}$ and statics power dissipation, the CEA-VDMOS is more suitable for low and medium frequencies in the power field.

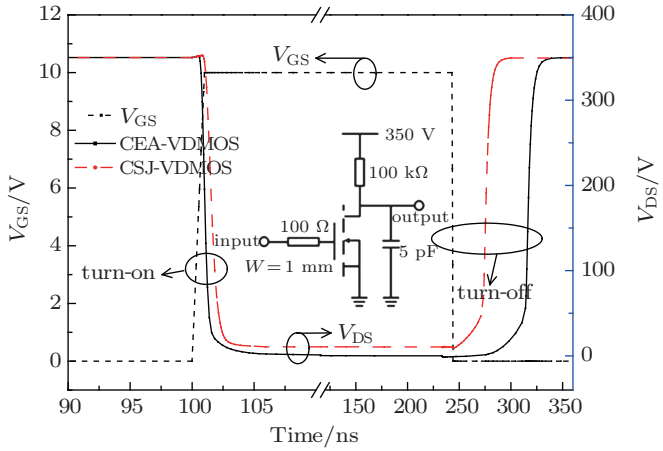


Fig. 7. (color online) Comparison of switching characteristic between the CEA-VDMOS and the CSJ-VDMOS.

Figure 8 demonstrates the relationships between the $R_{on,sp}$ and BV for the CEA-VDMOS and several power VDMOSFETs in the literature. The CEA-VDMOS obtains a much better trade-off between the BV and $R_{on,sp}$ than other VDMOS mentioned above, breaks through the silicon limit of the conventional VDMOS, and shows significant superiority to the SJ VDMOS.

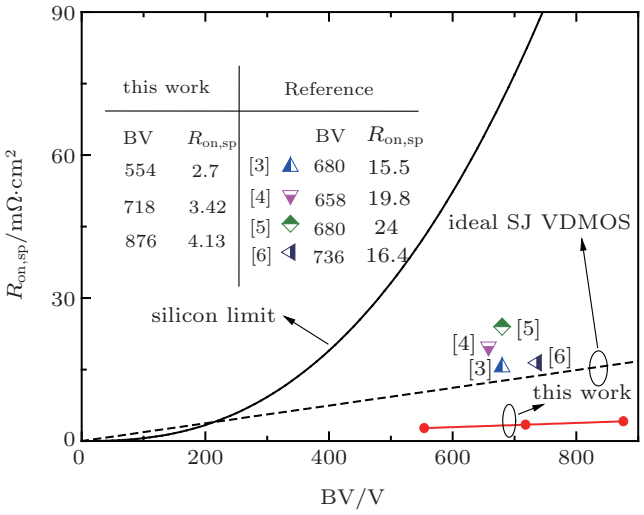


Fig. 8. (color online) Dependences of $R_{on,sp}$ on BV for several power VDMOSFETs.

Figure 9 shows the feasible key process steps to fabricate a prototype of CEA-VDMOS: etch n-type epitaxial layer to form the deep trench with a depth of 50 μm and width of 6 μm, followed by peroxidation, oxide etch (to remove the etch damage) and then thermal oxidation to form a thin oxide layer with the thickness in a range of 0.1 μm–0.2 μm (see Fig. 9(a)); selectively etch the bottom oxide (see Fig. 9(b));[13–15] fill the trench with a certain doped p-type silicon, followed by implantation to form the N^+ region (see Fig. 9(c)); choose low diffusion coefficient arsenic for accurate doping concentration and depth of the N^+ region (see Fig. 9(d)); fill the trench with P-type doped silicon (see Fig. 9(e));[12] implant to form P-wells, gate contact P^+ region and sources contact regions, then form the source/gate electrodes, followed by back-etching and forming the drain electrode (see Fig. 9(f)).

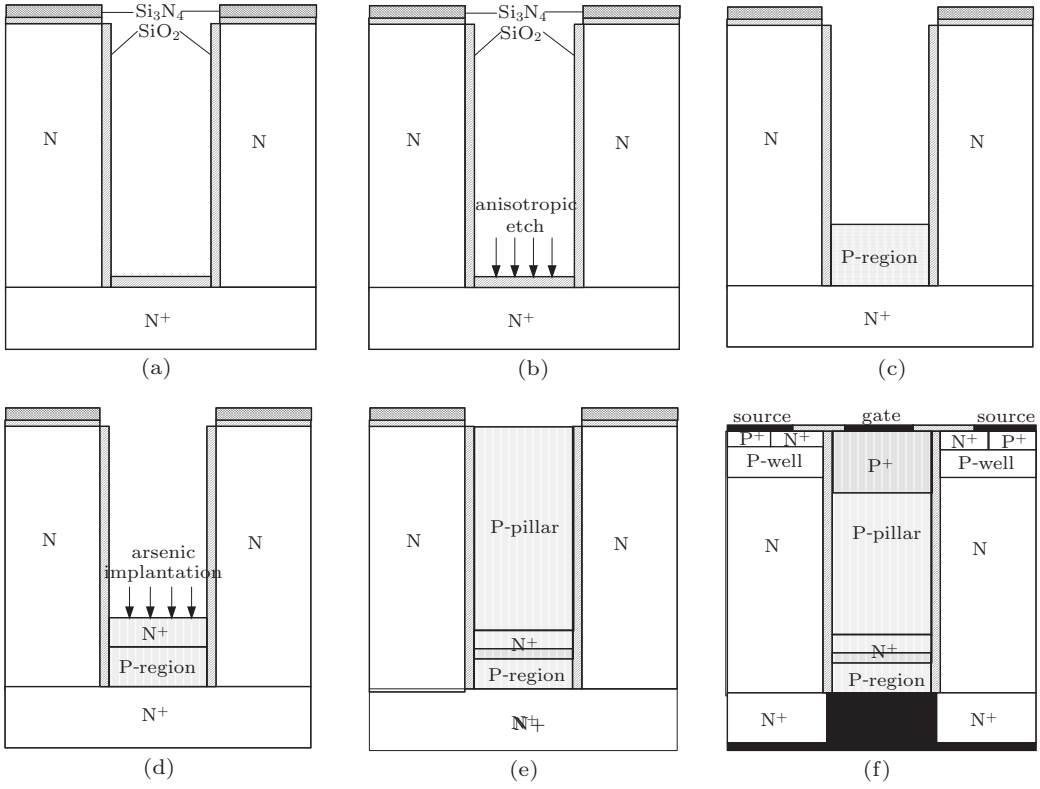


Fig. 9. Key steps to prepare the CEA-VDMOS: (a) etch a deep trench and form a thin oxide layer, (b) selectively etch the bottom oxide, (c) fill the trench with the p-type silicon, (d) implant arsenic to form N^+ region, (e) form the P-pillar, (f) form source/gate contact regions and electrodes and back-etch forming the drain electrode.

4. Conclusions

An ultra-low $R_{on,sp}$ VDMOS with continuous electron accumulation layer is proposed. The $R_{on,sp}$ is reduced dramatically and almost independent of n-pillar doping concentration. Furthermore, the depletion effect between the n-pillar and p-pillar in the off-state allows a higher n-pillar doping concentration and further reduces the $R_{on,sp}$. The simulations indicate that the CEA-VDMOS achieves an ultra-low $R_{on,sp}$ of 4.13 mΩ·cm^2, which is far lower than other SJ VDMOS, with a BV of 800-V maintained.

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