Two-dimensional models of threshold voltage and subthreshold current for symmetrical double-material double-gate strained Si MOSFETs*

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The two-dimensional models for symmetrical double-material double-gate (DM-DG) strained Si (s-Si) metal–oxide semiconductor field effect transistors (MOSFETs) are presented. The surface potential and the surface electric field expressions have been obtained by solving Poisson's equation. The models of threshold voltage and subthreshold current are obtained based on the surface potential expression. The surface potential and the surface electric field are compared with those of single-material double-gate (SM-DG) MOSFETs. The effects of different device parameters on the threshold voltage and the subthreshold current are demonstrated. The analytical models give deep insight into the device parameters design. The analytical results obtained from the proposed models show good matching with the simulation results using DESSIS.

Keywords: double-material double-gate MOSFET, strained Si, threshold voltage, subthreshold current

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1. Introduction

As metal oxide semiconductor devices have been scaled down continuously, the channel length has been shortened, and how to suppress the short channel effects (SCEs), the drain induced barrier lowering (DIBL) effect and increasing the carrier transport efficiency becomes an attractive problem.[1–3] It becomes obligatory to find out the solution of this problem to improve the device performance. Many reports show that the mobility of the charge carriers can be enhanced through the strain technology.[4,5] A strain can result in an enhanced mobility, a modified lattice constant of the material, and an energy band structure to trap carriers. Thus, strained Si (s-Si) metal–oxide semiconductor field effect transistors (MOSFETs) have received a great deal of attention.[6] However, the higher degree of impact ionization leads to the higher density of interface traps which in turn degrades both DIBL and SCEs.[7]

Double-gate (DG) and multi-material gate MOSFET structures can suppress the SCEs and DIBL in an excellent way. Many theoretical and experimental studies have reported that the DG device has excellent short-channel effect immunity, an ideal subthreshold factor, and high transconductance.[8–10] Multi-material gate MOSFET structures, like double-material gate (DMG) MOSFETs, are proposed to suppress SCEs. These structures have two or three metals in the gate with different work functions.[11] Long *et al.* first proposed the DMG MOSFET structure,[12] and demonstrated that the novel structure can increase the carrier transportation efficiency and suppress SCEs. The DMG structure can improve the device performance.

In light of these facts, for the first time, we present the two-dimensional models of threshold voltage and subthreshold current for symmetrical DM-DG s-Si MOSFET by incorporating the double-material double-gate concept into the biaxially strained channel device. By solving Poisson's equation, the surface potential can be obtained. The proposed models are derived based on the surface potential. In the channel region, Poisson's equation is solved by the parabolic approximation method with suitable boundary conditions.[13] The effects of various device parameters on the threshold voltage and the subthreshold current are demonstrated. Different length ratios are optimized to minimize the SCEs and the leakage current of the device. The derived analytical models give results that agree well with those of the 2D device simulator DESSIS.

2. Model formulation

The device structure is shown in Fig. 1. The gate is assumed to consist of two different metals, which have different work functions W_1 and W_2, known as the control gate and the

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screen gate whose corresponding lengths are L_1 and L_2. For nMOSFETs, the work function W_2 of M2 is smaller. Here, $W_1 = 4.70$ eV, $W_2 = 4.35$ eV, t_{s-Si} is the thickness of the s-Si film, t_{ox} is the thickness of the gate oxide, and gate length $L = L_1 + L_2$. The channel is divided into two different regions, region I and region II.

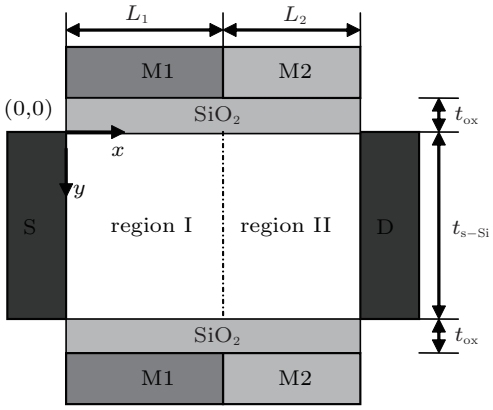


Fig. 1. Schematic diagram of symmetrical DM-DG s-Si MOSFET.

2.1. Surface potential model

The whole potential distribution is divided into the two regions in the s-Si layer. The potentials φ_1 and φ_2 belong to region I and region II, respectively. The x axis and the y axis are parallel and perpendicular to the channel, respectively. Poisson's equation in the two regions can be written as[13]

$$\frac{\partial^2\varphi_1(x,y)}{\partial x^2} + \frac{\partial^2\varphi_1(x,y)}{\partial y^2} = \frac{qN_D}{\varepsilon_{Si}}, \quad 0 \le x \le L_1, 0 \le y \le t_{s-Si}, \tag{1}$$

$$\frac{\partial^2\varphi_2(x,y)}{\partial x^2} + \frac{\partial^2\varphi_2(x,y)}{\partial y^2} = \frac{qN_D}{\varepsilon_{Si}}, \quad L_1 \le x \le L, 0 \le y \le t_{s-Si}, \tag{2}$$

where q is the electronic charge, N_D is the doping concentration in the channel, and ε_{Si} is the dielectric constant of the s-Si film.

The potential of the s-Si layer in the vertical direction can be approximated as[13]

$$\varphi_j(x,y) = \varphi_{Sj}(x) + C_{j1}(x)y + C_{j2}(x)y^2, \quad j = 1,2. \tag{3}$$

The coefficients $C_{j1}(x)$ and $C_{j2}(x)$, $j = 1,2$ are functions of x only. Due to the symmetry, we use the following boundary conditions to solve Poisson's equation.

(i) The electric flux at the interface of SiO_2/s-Si in the front gate is continuous

$$\left.\frac{\partial\varphi_j(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \cdot \frac{\varphi_{Sj}(x) - V_{GS} + (V_{FBj})_{s-Si}}{t_{ox}}, \quad j = 1,2, \tag{4}$$

where ε_{ox} and t_{ox} are the dielectric constant and the thickness of the gate oxide, respectively, $(V_{FB1})_{s-Si}$ and $(V_{FB2})_{s-Si}$ are the flat-band voltages for the control gate and the screen gate in the s-Si layer, respectively, and

$$(V_{FBj})_{s-Si} = (V_{FBj})_{Si} + \Delta V_{FB,f}, \quad j = 1,2,$$

$$(V_{FBj})_{Si} = \varphi_{Mj} - \left(\frac{\chi_{Si}}{q} + \frac{E_{g,Si}}{2q} + V_T \ln\left(\frac{N_D}{n_{i,Si}}\right)\right), \quad j = 1,2,$$

$$\Delta V_{FB,f} = \frac{-(\Delta E_C)_{s-Si}}{q} + \frac{(\Delta E_g)_{s-Si}}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right),$$

$$(\Delta E_C)_{s-Si} = 0.57Z,$$

$$(\Delta E_g)_{s-Si} = 0.4Z,$$

$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) = V_T \ln\left(\frac{m^*_{h,Si}}{m^*_{h,s-Si}}\right)^{3/2} \approx 0.075Z.$$

In the above equations, $(\Delta E_C)_{s-Si}$ is the increase value of electron affinity of silicon due to the strain, $(\Delta E_g)_{s-Si}$ is the decrease value of bandgap of silicon due to the strain, and Z is the strain of Ge mole fraction in the relaxed SiGe butter layer.[14]

(ii) The potential and the electric field at the interface of both regions are continuous

$$\varphi_1(L_1,0) = \varphi_2(L_1,0), \tag{5}$$

$$\frac{d\varphi_1(x,y)}{dx}\Big|_{x=L_1} = \frac{d\varphi_2(x,y)}{dx}\Big|_{x=L_1}. \tag{6}$$

(iii) The potentials at the source and the drain ends are

$$\varphi_1(0,0) = \varphi_{S1}(0) = V_{bi,s-Si}, \tag{7}$$

$$\varphi_2(L_1+L_2,0) = \varphi_{S2}(L_1+L_2) = V_{bi,s-Si} + V_{ds}, \tag{8}$$

where $V_{bi,s-Si}$ is the built-in voltage across the source–channel or drain–channel junctions in the s-Si layer.

By applying Eq. (4) and

$$\frac{d\varphi_j(x,y)}{dy}\Big|_{y=t_{s-Si}/2} = 0,$$

under the symmetry condition of the structure, the expression for the channel potential can be obtained. Substituting the channel potential into Eqs. (1) and (2), and setting $y = 0$, one obtains the equation of the surface potential in the two doping regions

$$\frac{d^2\varphi_{Sj}(x)}{dx^2} - \frac{1}{\lambda^2}\varphi_{Sj}(x) = D_j, \quad j = 1,2, \tag{9}$$

with

$$\lambda^2 = \frac{\varepsilon_{Si}t_{ox}t_{s-Si}}{2\varepsilon_{ox}},$$

$$D_j = \frac{qN_D}{\varepsilon_{Si}} - \frac{1}{\lambda^2}V_{GS} + \frac{1}{\lambda^2}(V_{FBj})_{s-Si}, \quad j = 1,2.$$

Equation (9) is second-order non-homogenous differential, and the solutions can be written as

$$\varphi_{S1}(x) = Ae^{x/\lambda} + Be^{-x/\lambda} - \lambda^2 D_1, \quad 0 \le x \le L_1, \tag{10}$$

$$\varphi_{S2}(x) = Ce^{x/\lambda} + De^{-x/\lambda} - \lambda^2 D_2, \quad L_1 \le x \le L. \tag{11}$$

Using the boundary conditions of Eqs. (5)–(8), the coefficients A, B, C, and D can be solved as

$$A = \frac{P_2\,\mathrm{e}^{L/\lambda} - P_1}{\mathrm{e}^{2L/\lambda} - 1}, \tag{12}$$

$$B = \frac{P_1\,\mathrm{e}^{2L/\lambda} - P_2\,\mathrm{e}^{L/\lambda}}{\mathrm{e}^{2L/\lambda} - 1}, \tag{13}$$

$$C = A - \frac{\sigma_1 - \sigma_2}{2}\,\mathrm{e}^{-L_1/\lambda}, \tag{14}$$

$$D = B - \frac{\sigma_1 - \sigma_2}{2}\,\mathrm{e}^{L_1/\lambda}, \tag{15}$$

where

$$\begin{aligned}
P_1 &= \lambda^2 D_1 + V_{\mathrm{bi,s-Si}},\\
P_2 &= (\lambda^2 D_2 + V_{\mathrm{bi,s-Si}} + V_{\mathrm{DS}}) + (\sigma_1 - \sigma_2)\cosh(L_2/\lambda),\\
\sigma_1 &= \frac{\lambda^2 q N_{\mathrm{D}}}{\varepsilon_{\mathrm{Si}}} + (V_{\mathrm{FB1}})_{\mathrm{s-Si}},\\
\sigma_2 &= \frac{\lambda^2 q N_{\mathrm{D}}}{\varepsilon_{\mathrm{Si}}} + (V_{\mathrm{FB2}})_{\mathrm{s-Si}}.
\end{aligned}$$

The control gate region which has the higher work function mainly monitors the threshold voltage of the device. So the threshold voltage is determined by $\varphi_{\mathrm{S1\,min}}$.

By solving $\mathrm{d}\varphi_{\mathrm{S1}}(x)/\mathrm{d}x = 0$ defined in Eq. (10), the position of the minimum surface potential can be calculated as

$$x_{1\,\mathrm{min}} = \frac{\lambda}{2}\ln\left(\frac{B}{A}\right). \tag{16}$$

The minimum surface potential can be estimated as

$$\varphi_{\mathrm{S1\,min}} = 2\sqrt{AB} - \lambda^2 D_1. \tag{17}$$

The electric field pattern along the channel determines the electron transport velocity. The surface electric fields in region I and region II are given respectively by

$$E_1(x) = (A/\lambda)\,\mathrm{e}^{x/\lambda} - (B/\lambda)\,\mathrm{e}^{-x/\lambda}, \tag{18}$$

$$E_2(x) = (C/\lambda)\,\mathrm{e}^{x/\lambda} - (D/\lambda)\,\mathrm{e}^{-x/\lambda}. \tag{19}$$

2.2. Threshold voltage model

The conventional definition of threshold voltage of MOSFETs is the gate source voltage at which $\varphi_{\mathrm{S\,min}} = 2\varphi_{\mathrm{F,Si}}$, where $\varphi_{\mathrm{F,Si}}$ is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level.[14] By considering the effect of strain, the threshold condition of the front gate for the present symmetrical DM-DG s-Si MOSFET is modified as[14,15]

$$\varphi_{\mathrm{S1\,min}} = \varphi_{\mathrm{th}}, \tag{20}$$

where

$$\begin{aligned}
\varphi_{\mathrm{th}} &= 2\varphi_{\mathrm{F,Si}} + \Delta\varphi_{\mathrm{s-Si}},\\
\Delta\varphi_{\mathrm{s-Si}} &= \frac{-(\Delta E_{\mathrm{g}})_{\mathrm{s-Si}}}{q} + V_{\mathrm{T}}\ln\left(\frac{N_{\mathrm{V,Si}}}{N_{\mathrm{V,s-Si}}}\right).
\end{aligned}$$

Substituting Eq. (20) into Eq. (17), we obtain the threshold voltage

$$V_{\mathrm{th}} = \frac{-b + \sqrt{b^2 - 4ac}}{2a}, \tag{21}$$

where

$$\begin{aligned}
\xi &= e^{L/\lambda},\\
a &= 4\xi(\xi-1)^2 - (\xi^2-1)^2,\\
b &= 2(\xi^2-1)^2(\sigma_1 + \varphi_{\mathrm{th}}) - 4(\xi-1)(V_1 + \xi V_2),\\
c &= 4V_1V_2 - (\xi^2-1)^2(\sigma_1 + \varphi_{\mathrm{th}})^2,\\
V_1 &= (V_{\mathrm{bi,S-Si}} + \sigma_1)\xi^2 - (V_{\mathrm{bi,S-Si}} + V_{\mathrm{ds}} + \sigma_2)\xi\\
&\quad + (\sigma_2 - \sigma_1)\xi\cosh\left(\frac{L_2}{\lambda}\right),\\
V_2 &= -(V_{\mathrm{bi,S-Si}} + \sigma_1) + (V_{\mathrm{bi,S-Si}} + V_{\mathrm{ds}} + \sigma_2)\xi\\
&\quad - (\sigma_2 - \sigma_1)\xi\cosh\left(\frac{L_2}{\lambda}\right).
\end{aligned}$$

2.3. Subthreshold current model

The diffusion phenomenon mainly determines the subthreshold current which is proportional to the carrier concentration at the position of the minimum channel potential. By applying the methodology used in Ref. [16], the subthreshold current can be expressed as

$$I_{\mathrm{DS}} = K\int_0^{t_{\mathrm{s-Si}}} \mathrm{e}^{\varphi_{1\,\mathrm{min}}(y)/V_{\mathrm{T}}}\,\mathrm{d}y, \tag{22}$$

where $K = (q\mu_{\mathrm{n}}WV_{\mathrm{T}}n_i^2/LN_{\mathrm{D}})(1 - \mathrm{e}^{-V_{\mathrm{ds}}/V_{\mathrm{T}}})$, μ_{n} is the mobility of electron,[15,17] V_{T} is the thermal voltage, and W is the width of the MOSFET. For the symmetric structure, the integral in Eq. (22) is divided into two parts along the channel thickness by the point $y_{\mathrm{m}} = (1/2)t_{\mathrm{s-Si}}$ as[16]

$$\begin{aligned}
I_{\mathrm{DS}} &= K\int_0^{t_{\mathrm{s-Si}}/2} \mathrm{e}^{\varphi_{1\,\mathrm{min}}(y)/V_{\mathrm{T}}}\,\mathrm{d}y\\
&\quad + K\int_{t_{\mathrm{s-Si}}/2}^{t_{\mathrm{s-Si}}} \mathrm{e}^{\varphi_{1\,\mathrm{min}}(y)/V_{\mathrm{T}}}\,\mathrm{d}y.
\end{aligned} \tag{23}$$

It is considered that $\varphi_{1\,\mathrm{min}}(y)$ varies linearly in both sections ($0 \le y < y_{\mathrm{m}}$ and $y_{\mathrm{m}} < y \le t_{\mathrm{s-Si}}$). After some simplifications, the subthreshold current can be written as

$$I_{\mathrm{DS}} = 2\frac{KV_{\mathrm{T}}}{E_{\mathrm{f}}}(\mathrm{e}^{\varphi_{\mathrm{m}}/V_{\mathrm{T}}} - \mathrm{e}^{\varphi_{\mathrm{m}}^{\mathrm{f}}/V_{\mathrm{T}}}), \tag{24}$$

where $E_{\mathrm{f}} = 2(\varphi_{\mathrm{m}} - \varphi_{\mathrm{m}}^{\mathrm{f}})/t_{\mathrm{s-Si}}$ represents the constant electric field, $\varphi_{\mathrm{m}}^{\mathrm{f}} = \varphi(x_{1\,\mathrm{min}}, 0)$ represents the minimum potential at the interface between s-Si film and SiO_2 layer, and $\varphi_{\mathrm{m}} = \varphi(x_{1\,\mathrm{min}}, t_{\mathrm{s-Si}}/2)$ is the minimum potential.

2.4. Results and discussion

In this paper, the analytical results obtained from the derived models are compared with the numerical simulation results using DESSIS. The doping concentration of the source–drain contact regions is $N_{DS} = 1 \times 10^{20}$ cm^{-3}. The device is simulated by using the drift-diffusion model for the carrier transport and the field-dependent mobility model because of the high electric fields in the device.

Figure 2 shows the surface potential along the channel length for different drain–source voltages. It can be observed that the minimum surface potential is located in the region under the control gate. A potential step exists near the interface of the two different gates for DM-DG MOSFET in comparison with single-material double-gate (SM-DG) MOSFET. It is the extra potential step that can increase the carrier transport. Because of the step potential, the additional drain voltage increase is absorbed under region II. In other words, region I is screened from the varied drain potential. Consequently, the drain voltage has little influence on region I. So the proposed novel structure can suppress the SCEs.

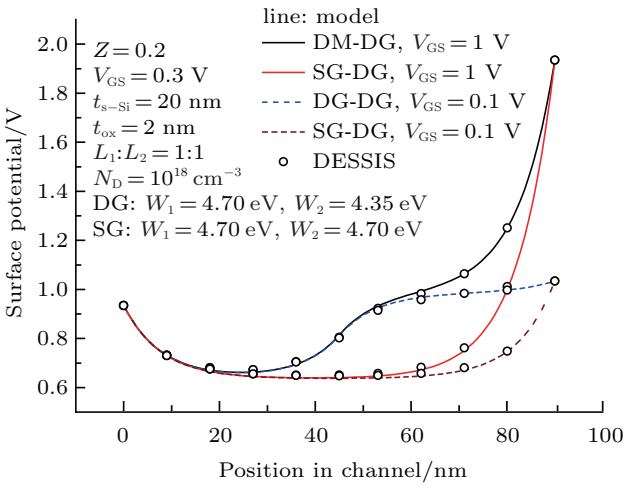


Fig. 2. (color online) Surface potentials in DM-DG and SM-DG MOSFETs with various drain voltages.

Figure 3 shows the surface electric fields in DM-DG s-Si MOSFET and SM-DG s-Si MOSFET. It can been observed that a peak electric field exists at the interface of region I and region II for the DM-DG s-Si MOSFET compared with the SM-DG s-Si MOSFET, which can increase the carrier mobility.

Figure 4 displays the threshold voltage for the proposed novel device with different strain Z. It is seen that the higher the Ge mole fraction Z, the lower the threshold voltage. The reason may be that the flatband voltage decreases, the built-in potential barrier in the source /drain-body decreases, and the inversion caused by the decrease in φ_{th} has an earlier onset. It can also be found that SCEs become apparent, and there is a sharp decrease when the channel length is below about 60 nm. This is due to the reason that the gate–source/drain charge sharing and source/drain–body depletion region becomes crucial for such short channel lengths.

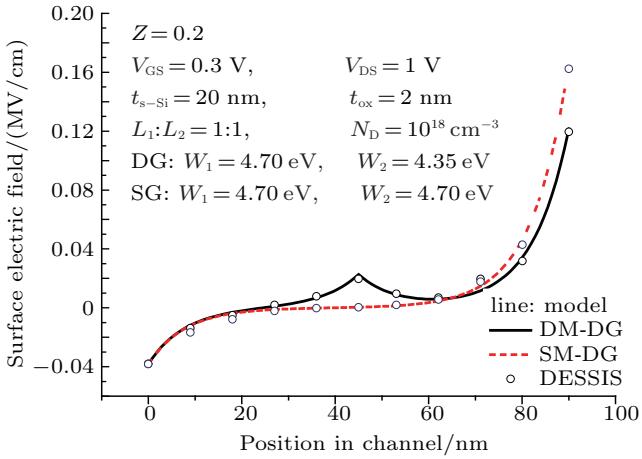


Fig. 3. (color online) Surface electric fields in DM-DG and SM-DG s-Si MOSFETs.

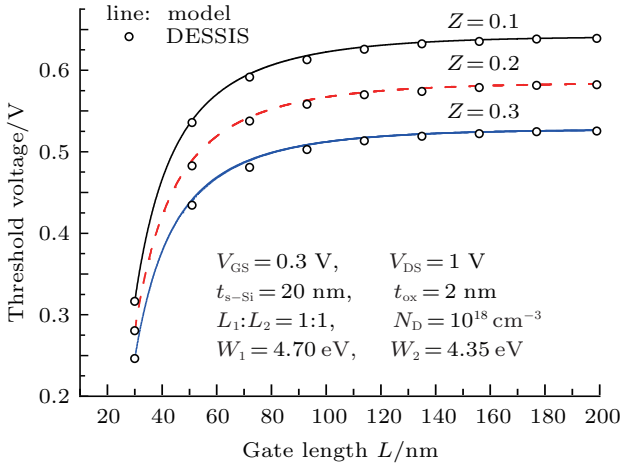


Fig. 4. (color online) Threshold voltages with different strains.

Figure 5 shows the threshold voltage against the channel length at various control-to-screen gate length ratios ($L_1 : L_2$). It can be observed that the threshold voltage increases with increasing gate length ratio. It is demonstrated that the higher gate length ratio induces the higher channel barrier height. It also validates that the device has better suppression of SCEs with a higher gate length ratio.

Figure 6 investigates the subthreshold current characteristics for different strains, keeping the other parameters constant. The subthreshold current is higher for the higher strain. It may be attributed to that the built-in potential barrier between the channel and the source decreases.[7] Note that the model is developed for the subthreshold regime only, therefore there exists a large discrepancy between the present model and the simulation results for higher gate to source voltage.

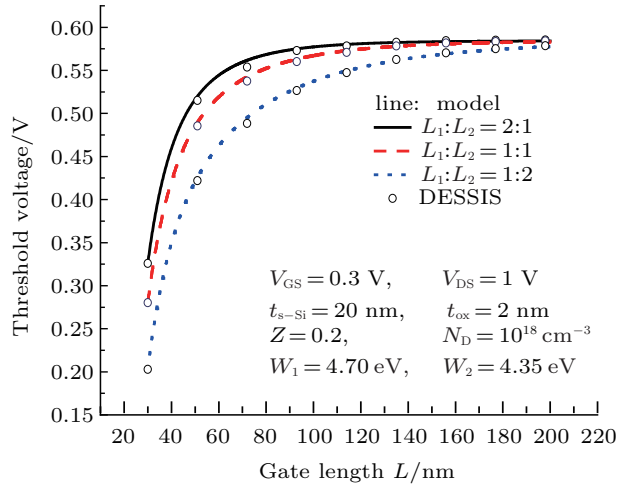


Fig. 5. (color online) Threshold voltages with different gate length ratios.

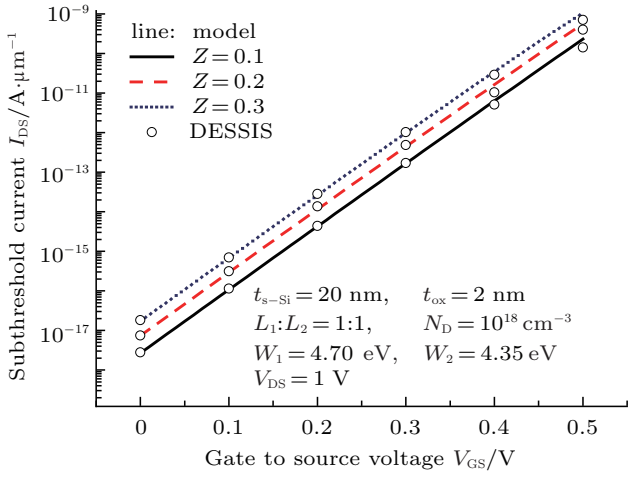


Fig. 6. (color online) Variation of subthreshold current with strain.

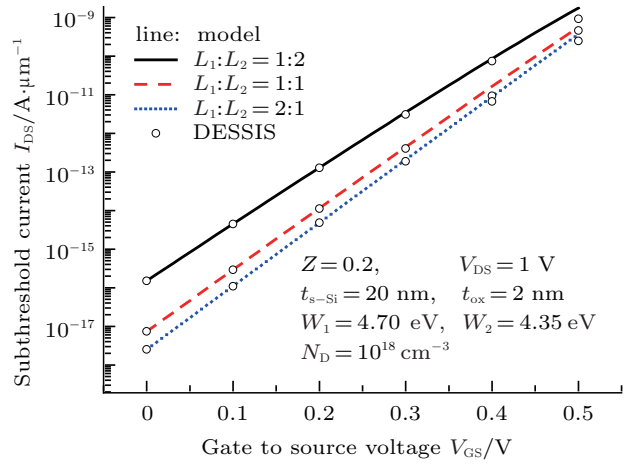


Fig. 7. (color online) Variation of subthreshold current with gate length ratio.

Figure 7 analyses the effect of gate length ratio $L_1 : L_2$ on the subthreshold current characteristics. The higher gate length ratio helps to reduce the leakage current effectively. This may be attributed to the fact that the source/channel barrier height increases with an increase in the length of the control gate. Furthermore, the higher gate length ratio can increase the slope of the subthreshold current, indicating the switching characteristics are being improved.

3. Conclusion

The two-dimensional models of threshold voltage and subthreshold current for symmetrical double-material double-gate strained Si MOSFETs have been presented. The surface potential has been obtained for a different drain voltage. A detailed analysis of the impact of various device parameters on the threshold voltage and the subthreshold current has been given. It is demonstrated that the threshold voltage decreases and the subthreshold current increases with increasing strain. The leakage current and SCEs can be controlled desirably by increasing the gate length ratio. The analytical models give accurate results as compared to the simulations. The analytical models give valuable references to the physical parameter design.

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