A uniform doping ultra-thin SOI LDMOS with accumulation-mode extended gate and back-side etching technology*

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A uniform doping ultra-thin silicon-on-insulator (SOI) lateral-double-diffused metal-oxide-semiconductor (LDMOS) with low specific on-resistance ($R_{on,sp}$) and high breakdown voltage (BV) is proposed and its mechanism is investigated. The proposed LDMOS features an accumulation-mode extended gate (AG) and back-side etching (BE). The extended gate consists of a P– region and two diodes in series. In the on-state with $V_{GD} > 0$, an electron accumulation layer is formed along the drift region surface under the AG. It provides an ultra-low resistance current path along the whole drift region surface and thus the novel device obtains a low temperature distribution. The $R_{on,sp}$ is nearly independent of the doping concentration of the drift region. In the off-state, the AG not only modulates the surface electric field distribution and improves the BV, but also brings in a charge compensation effect to further reduce the $R_{on,sp}$. Moreover, the BE avoids vertical premature breakdown to obtain high BV and allows a uniform doping in the drift region, which avoids the variable lateral doping (VLD) and the "hot-spot" caused by the VLD. Compared with the VLD SOI LDMOS, the proposed device simultaneously reduces the $R_{on,sp}$ by 70.2% and increases the BV from 776 V to 818 V.

Keywords: LDMOS, accumulation gate, back-side etching, breakdown voltage, specific on-resistance

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1. Introduction

For high voltage power metal–oxide–semiconductor field-effect transistors (MOSFETs), two major targets are to reduce the power dissipation and enhance the breakdown voltage (BV), thereby realizing the trade-off between the specific on-resistance ($R_{on,sp}$) and BV.[1,2] Many approaches including the reduced surface field (RESURF) and super junction (SJ) are used to realize the targets. However, the $R_{on,sp}$ in SJ and RESURF devices is strongly dependent on the drift doping concentration (N_d).[3–6] In order to realize high BV for the thin SOI, the variable lateral doping (VLD) and back-side etching (BE) are typical technologies by achieving a uniform lateral electric field.[7–9] However, the VLD technique leads to a "hot-spot" on the source side where the resistance is large for the low doping concentration[10] and its fabrication process needs a long-time high-temperature annealing.[11] The BE technique removes the substrate-assisted depletion effect (SAD), which results in a sharp decrease in N_d and restricts the current capability. Therefore, the BE technique was mainly applied to the IGBT with a conduction modulation effect.[9,12]

In this paper, an ultra-thin SOI LDMOS with an accumulation gate (AG) over the drift region and back-side etching (BE) (AG-BE SOI LDMOS) is proposed. Except for complex external control circuits, a high density electron accumulation layer is formed along the drift surface in the on-state.[13] This not only reduces the $R_{on,sp}$ significantly, but also makes $R_{on,sp}$ nearly independent of the doping concentration of the drift region. The BE technique allows a uniform doping concentration in the drift region to obtain high BV. The combination of the accumulation layer and the uniform doping concentration profile not only reduces the $R_{on,sp}$ and the process difficulty, but also solves the "hot-spot" problem in the ultra-thin device with the VLD technology. The MEDICI simulator is used to study the mechanism of the AG-BE SOI LDMOS. The results demonstrate that the proposed device possesses good performances.

2. Device structure and mechanism

Figure 1 shows the schematic of the cross section of the AG-BE SOI LDMOS. The novel SOI LDMOS is characterized by the AG over the drift region and BE of the substrate. Note that the AG structure consists of a P-region and two diodes (D_1 and D_2) in series, and its two ends connect with the gate electrode and the drain electrode respectively. The substrate under the drift region is etched. The x and y directions are marked. L_d is the length of the drift region; t_{top}, t_{si}, and t_{box} represent

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the thickness values of the AG layer, the drift region and the buried oxide, respectively; N_d is the doping concentration of the drift region, and N_p is the doping concentration of the P– region in the AG structure.

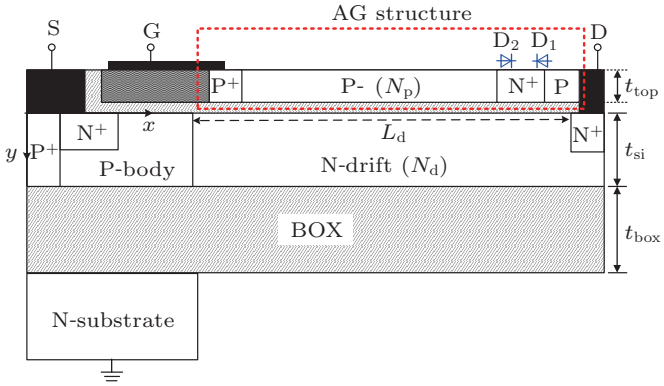


Fig. 1. (color online) Schematic diagram of cross section of the AG-BE SOI LDMOS.

Figure 2 illustrates the operation mechanism of the novel SOI lateral-double-diffused metal-oxide-semiconductor. An MIS-like structure is formed by the N-drift region, the gate dielectric layer and the P- region of the AG structure. In the on-state with $V_{GD} > 0$, the diode D_1 principally sustains the gate-drain voltage (V_{GD}), and an electron accumulation layer is formed along the surface of the N-drift region. The accumulation layer forms an ultra-low resistance current path as shown in Fig. 2(a). Therefore, most of the current flows through the accumulation layer and thus the $R_{on,sp}$ is almost independent of N_d. In the off-state, $V_{DS} = V_{DG} > 0$, the P- region of the AG and N-drift region works like an SJ with a thin oxide layer as depicted in Fig. 2(b). Then N_d increases and the $R_{on,sp}$ further decreases due to the charge compensation.[14,15] Note that the diode D_1 or D_2 is reverse-biased to sustain the gate-drain voltage drop (V_{GD}) in the on-state or off-state respectively, which ensures a lower leakage current in the top layer than that in Ref. [16].

In our simulations, the physical models of CONSRH, AUGER, BGN, FLDMOB, SRFMOB, IMPACT.I, and CC-SMOB are mainly used, and the NEWTON solution method is used with two types of carriers. The dimensional parameters of the novel structure are set as follows: $L_d = 46$ μm, $t_{top} = t_{si} = 0.2$ μm, and $t_{box} = 1$ μm.

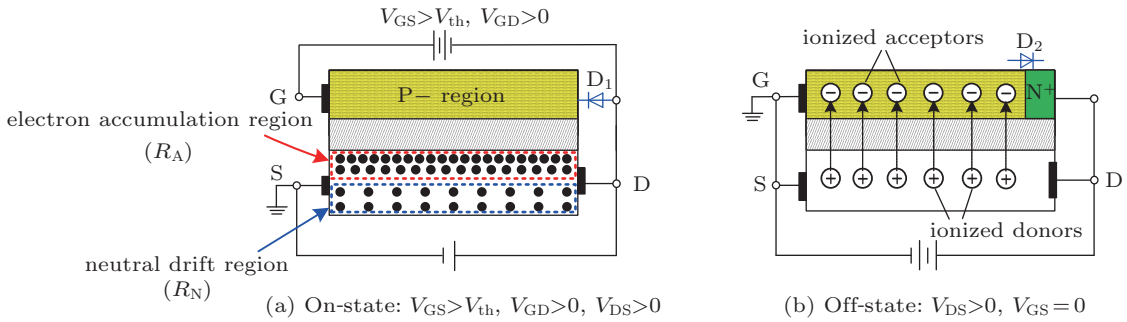


Fig. 2. (color online) Operation mechanism. (a) On-state: $V_{GS} > V_{th}$, $V_{GD} > 0$, $V_{DS} > 0$; (b) off-state: $V_{DS} > 0$, $V_{GS} = 0$, and reverse biased D_2 sustains the V_{DG}.

Figure 3 shows the equipotential contours and the lateral component of surface electric field (E_x) for the AG-BE silicon-on-insulator lateral-double-diffused metal-oxide-semiconductor, ultra-thin silicon-on-insulator lateral-double-diffused metal-oxide-semiconductor with accumulation extended gate and VLD profile in drift region (AEG-VLD SOI LDMOS),[17] ultra-thin silicon-on-insulator lateral-double-diffused metal-oxide-semiconductor with VLD profile in drift region (VLD SOI LDMOS) and conventional ultra-thin silicon-on-insulator lateral-double-diffused metal-oxide-semiconductor with a uniform doped drift region. For ultra-thin SOI devices in Figs. 3(a)–3(d), the structure with VLD or BE can generate near-ideal potential distributions in the drift region as shown in the red dashed boxes in Figs. 3(a)–3(c) respectively. The BE technique releases the equipotential lines below the buried oxide as shown in the black rectangle in Fig. 3(a); however, the equipotential contours of the VLD and AEG-VLD structure terminate in the bottom interface of the buried oxide as indicated in Figs. 3(b)–3(c). In other words, the BE removes the vertical voltage drop and avoids vertical premature breakdown, which indicates that the BV is almost independent of the thickness values of the drift region and the buried oxide. Figure 3(e) shows that E_x for the conventional device is zero in the middle, fortunately, the AG-BE or the VLD not only enhances the E_x but also makes the field distribution more uniform. Furthermore, the BE technique almost removes the electric field peak on the drain side (E_{xd}), and the AG enhances the E_x in the middle more effectively than the VLD. Therefore, the BV of the AG-BE silicon-on-insulator lateral-double-diffused metal-oxide-semiconductor increases from 776 V to 818 V for the VLD silicon-on-insulator lateral-double-diffused metal-oxide-semiconductor.

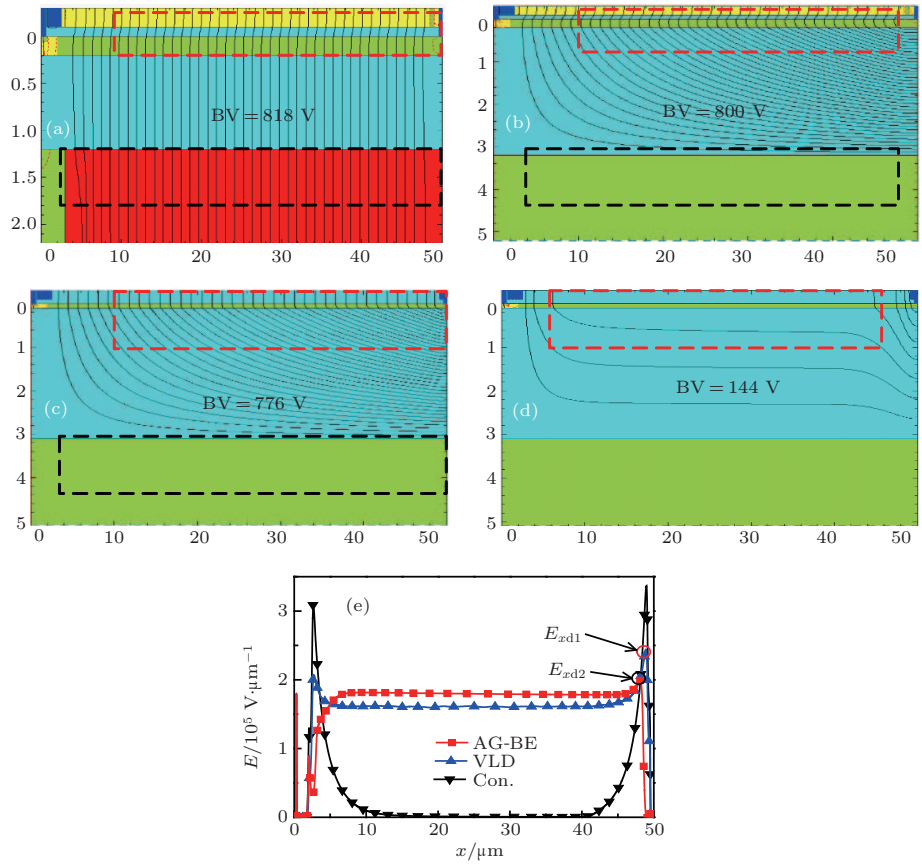


Fig. 3. (color online) Equipotential contour distributions (20 V/contour) at breakdown (optimally) for (a) AG-BE SOI LDMOS (BV = 818 V), (b) AEG-VLD SOI LDMOS (BV = 800 V), (c) VLD SOI LDMOS (BV = 776 V), and (d) conventional SOI LDMOS (BV = 144 V); (e) lateral surface electric field component.

3. Results and discussion

Figure 4 compares the on-state current densities of the AG-BE SOI LDMOS, the VLD SOI LDMOS and the JFP-BE SOI LDMOS at $x = 5$ μm. The JFP-BE SOI LDMOS features a junction field plate (JFP)[18] and BE. In the blocking state, the P-region in the JFP generates additional depletion in the N-drift region and increases the N_d, which is almost the same as the scenarios in AG-BE devices, so the same optimal $N_d = N_p = 4 \times 10^{16}$ cm^{-3} and the same BV are obtained for the JFP-BE and AG-BE devices. For the AG-BE SOI LDMOS, the resistance in the drift region (R_D) contains the accumulation layer resistance (R_A) and the neutral drift region resistance (R_N) in parallel, and $R_A \ll R_N$ because of the high density accumulation electrons. Therefore, the surface current density of the accumulation layer is three orders higher than that in the neutral drift region, and the current through the accumulation layer (I_A) is approximately 88% of the total current (I_D) as shown in Fig. 4. Owing to the same N_d, the R_N of the AG-BE device is the same as that of the JFP-BE device, and thus the current density I_N values in the neutral drift region for AG-BE and JFP-BE devices are consistent. The I_N value of the VLD SOI LDMOS is higher than those of AG-BE and JFP-BE SOI LDMOS, because the SAD effect of the VLD SOI LDMOS allows a higher N_d. Consequently, compared with the cases of the other two devices, the $R_{on,sp}$ of the AG-BE device drops significantly and is almost independent of N_d. The $R_{on,sp}$ values of the AG-BE SOI LDMOS, the VLD SOI LDMOS, and the JFP-BE SOI LDMOS are 38.1 mΩ·cm^2, 106 mΩ·cm^2, and 191 mΩ·cm^2, respectively. However, the $R_{on,sp}$ of SOI LDMOS only with the BE technique is over 5500 mΩ·cm^2 at the same cell pitch.

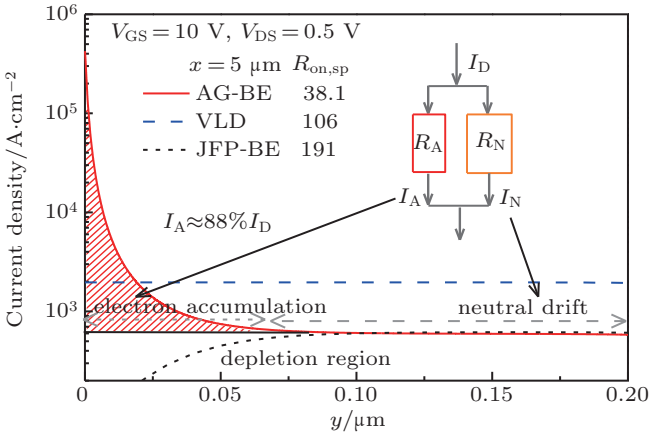


Fig. 4. (color online) Current density distributions of three devices at $x = 5$ μm.

Figures 5(a) and 5(b) show the three-dimensional (3D) temperature distributions of the AG-BE SOI LDMOS and the VLD SOI LDMOS at the same power density (P) of $P = 1$ mW/ μm, respectively. Obviously, the VLD SOI LDMOS suffers a serious "hot-spot" on the source side for the low doping concentration herein. By contrast, the AG-BE SOI LDMOS obtains a lower and more uniform temperature in the drift region due to the lower and more evenly-distributed R_D. Because of the accumulation layer and uniform drift doping, the maximum temperature of the AG-BE SOI LDMOS decreases from 359 K to 327 K of the VLD SOI LDMOS.

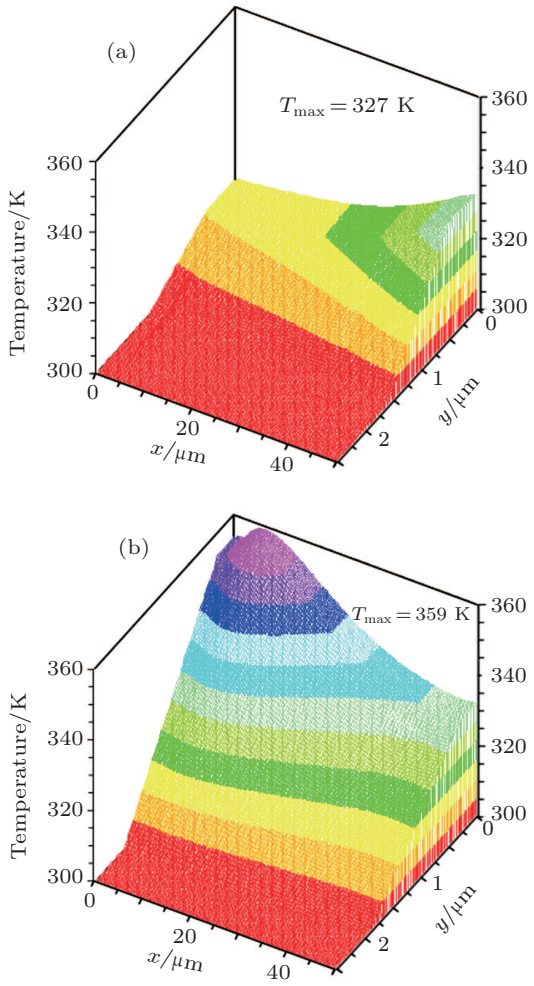


Fig. 5. (color online) 3D temperature distributions at $P = 1$ mW/ μm for (a) AG-BE SOI LDMOS and (b) VLD SOI LDMOS.

Figures 6(a) and 6(b), respectively, show the influences of the L_d and t_{box} on the BV and those of BV and $R_{on,sp}$ on L_d for the AG-BE SOI LDMOS and VLD SOI LDMOS. As illustrated in Fig. 6(a), the BV of the VLD SOI LDMOS is saturated for $L_d > 45$ μm with $t_{box} = 2$ μm and $L_d > 75$ μm with $t_{box} = 3$ μm, because its vertical BV is limited by the thickness values of the drift region and the buried oxide layer. However, the BV of AG-BE SOI LDMOS is determined by the lateral BV and increases approximately linearly with increasing L_d, thereby avoiding the limit of the vertical BV as shown in Figs. 6(a) and 6(b). Therefore, the optimized t_{box} values for the novel device and the VLD SOI LDMOS are 1 μm and 3 μm, respectively. Moreover, owing to the accumulation layer, the $R_{on,sp}$ of the novel device is lower and increases more slowly with the increasing L_d than that of VLD SOI LDMOS as shown in Fig. 6(b). Figure 7 compares the $R_{on,sp}$ versus BV for this work with existing RESURF LDMOSFETs and SJ LDMOSFETs. The AG-BE SOI LDMOS obtains a superior trade-off between the BV and $R_{on,sp}$ to the others.

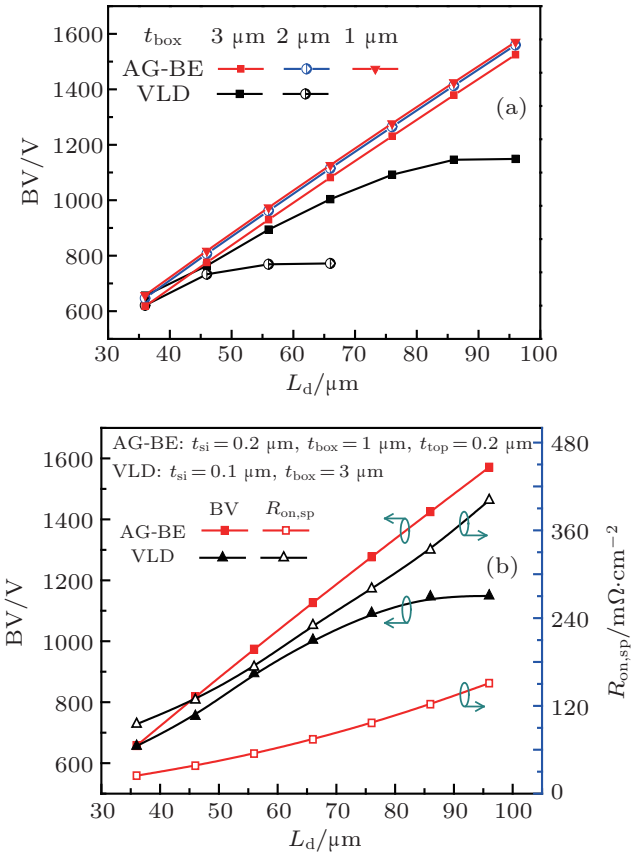


Fig. 6. (color online) (a) Influences of L_d and t_{box} on BV, (b) dependences of the BV and $R_{on,sp}$ on L_d.

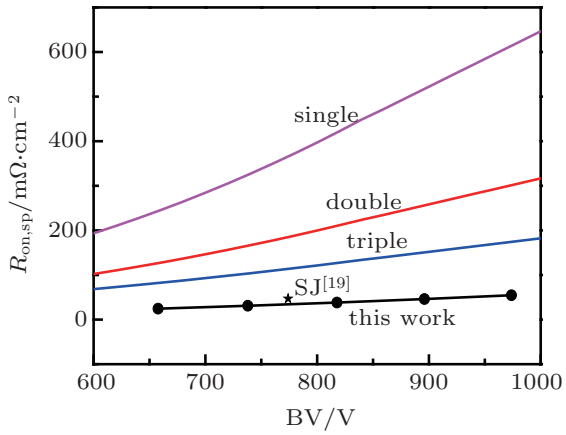


Fig. 7. (color online) Comparison of results between this work and the others.

Figure 8 shows the feasible key fabrication steps of the AG-BE SOI LDMOS. The process to obtain the monocrystalline silicon in the AG is based on the SIMOX technology. Step (a) is for the process of the oxygen ion implantation,[20] followed by the annealing process to form the field oxide layer, leaving monocrystalline silicon on the oxide. Step (b) is for boron implantation to form the P-region in AG. Steps (c) and (d) are to form the active region and P-well by etching and boron implantation. Steps (e)–(g) are for the processes to form the poly-gate, contact regions and electrodes respectively. Finally, front-passivation is accomplished and followed by a substrate back-etching and subsequent back-passivation.[21,22]

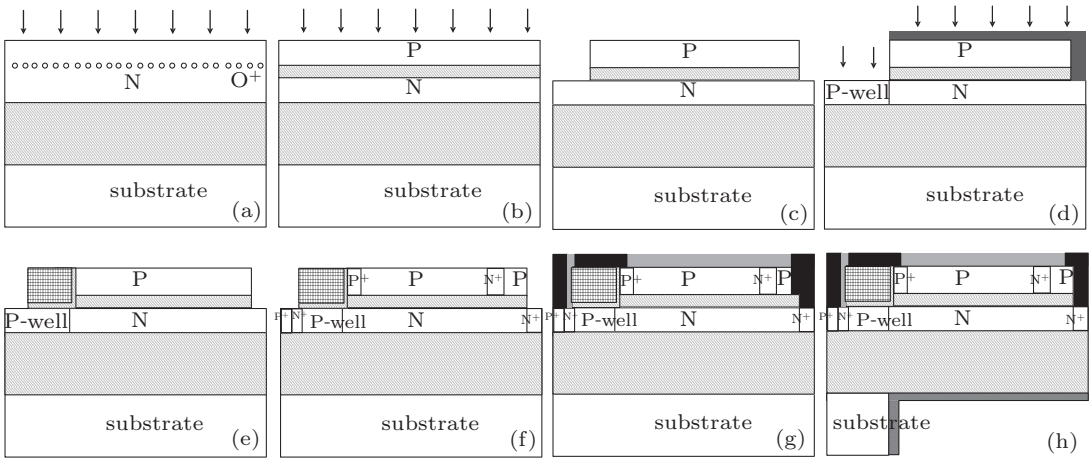


Fig. 8. Feasible key fabrication steps for forming the AG-BE SOI LDMOS: (a) oxygen ion implantation and annealing process to form the gate dielectric layer, (b) boron implantation to form the P-region in AG, (c) etching to form the active region, (d) boron implantation to form the P-well, (e) forming the gate oxide and poly-gate, (f) impurity implantation and annealing to form the contact regions, (g) forming the electrodes and front passivation, and (h) substrate back-etching and back passivation.

4. Conclusions

A novel SOI LDMOS with an accumulation gate and back-side etching is proposed and investigated by simulation. A high density electron accumulation layer generated by the AG provides a low resistant current path, which not only reduces the $R_{on,sp}$, but also flattens the surface temperature. On the other side, the back-side etching not only achieves a near-ideal potential distribution with a uniform doping concentration in the drift region but also avoids vertical premature breakdown. Compared with the VLD SOI LDMOS, the novel device combining the accumulation gate and back-side etching reduces the $R_{on,sp}$ by 70.2% and improves the BV from 776 V to 818 V.

References

[1] Ludikhuize A W 2001 *Proceedings of the 31st European, IEEE Solid-State Device Research Conference*, September 11–13, 2001, p. 35

[2] Iqbal M M, Udrea F and Napoli E 2009 *IEEE Proceedings of the 21st International Symposium on Power Semiconductor Devices and ICs*, June 14–18, 2009, Barcelona, Spain, p. 247

[3] Ming Q, Li Y F, Zhou X, Li Z J and Zhang B 2014 *IEEE Electron Dev. Lett.* **35** 774

[4] Chen X B U S Patent 5216275 [1993-06-01]

[5] Chen Y, Liang Y C, Samudra G S, Xin Y, Buddharaju K D and H H Feng 2008 *IEEE Trans. Electron Dev.* **55** 211

[6] Luo X, Wei J, Shi X, Zhou K, Tian R, Zhang B and Li Z 2014 *IEEE Trans. Electron Dev.* **61** 4304

[7] Merchant S, Arnold E, Baumgart H, Mukherjee S, Pein H and Pinker R 1991 *IEEE Proceedings of the 3rd International Symposium on Power Semiconductor Devices and ICs*, April 22–24, 1991, Maryland, USA, p. 31

[8] Luo X R, Wei J, Shi X L, Zhou K, Tian R C, Zhang B and Li Z J 2014 *IEEE Trans. Electron. Dev.* **61** 4304

[9] Udrea F, Trajkovic T, Lee C, Garner D, Yuan X, Joyce J, Udugampola N, Bonnet G, Coulson D, Jacques R, Izmajlowicz M, van der Duijn Schouten N, Ansari Z, Moyse P and Amaratunga G A J 2005 *IEEE Proceedings of the 17th International Symposium on Power Semiconductor Devices and ICs*, Santa Barbara, USA, p. 267

[10] Leung Y K, Amit K P, Kenneth E G, James D P and Wong S S 1997 *IEEE Electron Dev. Lett.* **18** 414

[11] Zhang S, Sin J K O, Lai T M L and Ko P K 1999 *IEEE Trans. Electron Dev.* **46** 1036

[12] T Trajkovic, F Udrea, C Lee, N Udugampola, V Pathirana, A Mihaila and G A J Amaratunga 2008 *IEEE Proceedings of the 20th International Symposium on Power Semiconductor Devices and ICs*, May 18–22, 2008, Oralando, USA, p. 327

[13] Lyu X J and Chen X B 2013 *IEEE Trans. Electron Dev.* **60** 3821

[14] Chen X B and Sin J K O 2001 *IEEE Trans. Electron Dev.* **48** 344

[15] K P Gan, Yung C Liang, Ganesh S Samudra, S M Xu and Liu Y 2001 *Power Electronics Specialists Conference*, June 17–21, 2001, Vancouver, Canada, p. 2156

[16] Vestling L, Edholm B, Olsson J, Tiensuu S and Soderbarg A 1997 *Proceedings of the International Symposium on Power Semiconductor Devices & IC's*, May 26–29, 1997, Weimar, Germany, p. 45

[17] Wei J, Luo X, Zhang Y, Li P, Zhou K, Li Z and Zhang B 2015 *Proceedings of the International Symposium on Power Semiconductor Devices and IC's*, May 10–14, 2015, Hong Kong, China, p. 185

[18] Luo Y C, Luo X R, Hu G Y, Fan Y H, Li P C, Wei J, Tan Q and Zhang B 2014 *Chin. Phys. B* **23** 077306

[19] Z Lin and X B Chen 2015 *IEEE Electron Dev. Lett.* **36** 588

[20] Matsumura A, Sasaki T and Kitahara K US patent 0170940 [2003].

[21] Udrea F, Trajkovicand T and Amaratunga G A J 2004 *Proceedings of IEEE Int. Electron Devices*, December 13–15, 2004, San Francisco, USA, p. 451

[22] Udrea F and Amaratunga G US patent 6703684 [2004]