Modeling of a triple reduced surface field silicon-on-insulator lateral double-diffused metal–oxide–semiconductor field-effect transistor with low on-state resistance*

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An analytical model for a novel triple reduced surface field (RESURF) silicon-on-insulator (SOI) lateral double-diffused metal–oxide–semiconductor (LDMOS) field effect transistor with n-type top (N-top) layer, which can obtain a low on-state resistance, is proposed in this paper. The analytical model for surface potential and electric field distributions of the novel triple RESURF SOI LDMOS is presented by solving the two-dimensional (2D) Poisson's equation, which can also be applied to single, double and conventional triple RESURF SOI structures. The breakdown voltage (BV) is formulized to quantify the breakdown characteristic. Besides, the optimal integrated charge of N-top layer ($Q_{\rm ntop}$) is derived, which can give guidance for doping the N-top layer. All the analytical results are well verified by numerical simulation results, showing the validity of the presented model. Hence, the proposed model can be a good tool for the device designers to provide accurate first-order design schemes and physical insights into the high voltage triple RESURF SOI device with N-top layer.

Keywords: analytical model, triple reduced surface field (RESURF), silicon-on-insulator (SOI), n-type top (N-top) layer

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1. Introduction

Owing to its ideal dielectric isolation, higher speed, less parasitic effect, and higher integration, silicon-on-insulator (SOI) technology is of great benefit to high voltage lateral double-diffusion metal–oxide–semiconductor (LDMOS) devices and has been widely developed for a variety of power ICs , such as automotive driver IC, display driver IC, high-voltage switching IC, LED driver IC, etc.[1–7] One of the main issues when designing LDMOS is the trade-off between breakdown voltage (BV) and specific on-resistance ($R_{\rm on,sp}$).[8–14] Triple reduced surface field (RESURF) technology[15–21] is an excellent method in mass manufacture to achieve the trade-off between BV and $R_{\rm on,sp}$. With a floating p-type buried (P-buried) layer inserted into n-type drift region, the triple RESURF structure provides dual conduction paths to reducing $R_{\rm on,sp}$. Because of the three-sided vertical depletion, the drift region doping concentration can be three times higher than that in single RESURF, with the BV maintained. Compared with the conventional triple RESURF SOI LDMOS, the novel triple RESURF SOI LDMOS with n-type top (N-top) layer can achieve a lower $R_{\rm on,sp}$, with a high BV maintained, because the incorporation of N-top layer has a weak effect on the breakdown characteristics and provides a lower on-resistance surface conduction path. Hence, the novel triple RESURF SOI LDMOS with N-top layer can achieve a more optimal distribution of impurities for triple RESURF structure to improve the tradeoff between the BV and $R_{\rm on,sp}$. Some similar work of the triple RESURF LDMOS with N-top layer on bulk-silicon is reported in our previous work.[20,21]

In the present paper, an analytical model for the novel triple RESURF SOI LDMOS with low on-state resistance is presented. The model for the surface potential and electrical field distributions, which is based on the two-dimensional (2D) Poisson's equation, is obtained. The analytical expressions of surface potential and electric field can be simply applied to single, double and conventional triple RESURF SOI LDMOS. Further, the analytical results of BV and optimal integrated charge of N-top layer ($Q_{\rm ntop}$) for the novel triple RESURF SOI LDMOS are obtained. The analytical results of the presented model can show great agreement with the numerical simulation results. Hence, the proposed model can give guidance for designer to optimize the novel triple RESURF SOI LDMOS with N-top layer.

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2. Structure and model

Figure 1 shows the cross-section of the triple RESURF SOI LDMOS with N-top layer. The P-buried layer is in the N-well, and the doping concentration is N_{PB}. Compared with the structure of the conventional triple RESURF SOI LDMOS, a high-doped N-top layer with doping concentration N_T is introduced at the surface of N-well. As a result, lower $R_{on,sp}$ is achieved because of extra majority carriers, which provides a lower on-resistance surface conduction path. The doping concentration of the N-well is N_{nwell}. The N-well is divided into five regions along the edges of P-buried layer and N-top layer, and their boundary positions are given by: $x = 0$, L_1, L_2, L_d, and $y = 0$, t_1, t_2, t_d. The t_{ox} is defined as the thickness of the SOI layer.

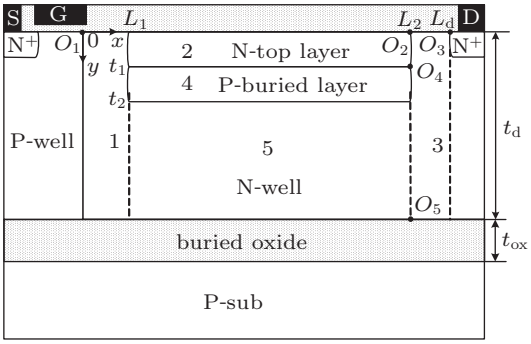


Fig. 1. The cross section of triple RESURF SOI LDMOS with N-top layer.

When the device is biased in the off-state and the N-well is fully depleted, the potential function in the silicon must satisfy 2D Poisson's equation, yielding:

$$\frac{\partial \varphi_i^2(x,y)}{\partial x^2} + \frac{\partial \varphi_i^2(x,y)}{\partial y^2} = -\frac{qN_i}{\varepsilon_s}, \quad i = 1,2,3,4,5, \tag{1}$$

where q is the electric charge, ε_s is the dielectric constant for silicon, $N_1 = N_3 = N_5 = N_{nwell}$, $N_2 = N_T + N_{nwell}$, and $N_4 = N_{PB} - N_{nwell}$. The boundary conditions for the potential function are given by

$$\left.\frac{\partial \varphi_i(x,y)}{\partial y}\right|_{y=0} = 0, \quad i = 1,2,3, \tag{2}$$

$$\left.\frac{\partial \varphi_i(x,y)}{\partial y}\right|_{y=t_d} = -\frac{\varphi_i(x,t_d)}{Kt_{ox}}, \quad i = 1,3,5, \tag{3}$$

$$\varphi_2(x,t_1) = \varphi_4(x,t_1), \left.\frac{\partial \varphi_2(x,y)}{\partial y}\right|_{y=t_1} = \left.\frac{\partial \varphi_4(x,y)}{\partial y}\right|_{y=t_1}, \tag{4}$$

$$\varphi_4(x,t_2) = \varphi_5(x,t_2), \left.\frac{\partial \varphi_4(x,y)}{\partial y}\right|_{y=t_2} = \left.\frac{\partial \varphi_5(x,y)}{\partial y}\right|_{y=t_2}, \tag{5}$$

$$\varphi_1(L_1,0) = \varphi_2(L_1,0) = V_1, \quad \left.\frac{\partial \varphi_1(x,0)}{\partial x}\right|_{x=L_1} = \left.\frac{\partial \varphi_2(x,0)}{\partial x}\right|_{x=L_1}, \tag{6}$$

$$\varphi_2(L_2,0) = \varphi_3(L_2,0) = V_2, \quad \left.\frac{\partial \varphi_2(x,0)}{\partial x}\right|_{x=L_2} = \left.\frac{\partial \varphi_3(x,0)}{\partial x}\right|_{x=L_2}, \tag{7}$$

$$\varphi_1(0,0) = 0, \quad \varphi_3(L_d,0) = V_d, \tag{8}$$

where $K = \varepsilon_s/\varepsilon_{ox}$ and ε_{ox} is the dielectric constant for SiO_2. Equation (2) is the vertical electric field at the semiconductor surface, which can be ignored. Equation (3) is the continuity of electric flux density across charge-free boundary. Equations (4)–(7) are the continuity equations of the potential and electric field along the boundaries of 2–4, 4–5, 1–2, and 2–3 regions, respectively. Equation (8) is the voltage condition applied to the device. The potential function can be Taylor expanded with respect to y coordinate up to the second-order terms as

$$\varphi_i(x,y) = \varphi_i(x,0) + \frac{\partial \varphi_i(x,0)}{\partial y}\cdot y + \frac{\partial^2 \varphi_i(x,0)}{2\cdot \partial y^2}\cdot y^2, \quad i = 1,2,3, \tag{9}$$

$$\varphi_4(x,y) = \varphi_4(x,t_1) + \frac{\partial \varphi_4(x,t_1)}{\partial y}\cdot (y-t_1) + \frac{\partial^2 \varphi_4(x,t_1)}{2\cdot \partial y^2}\cdot (y-t_1)^2, \tag{10}$$

$$\varphi_5(x,y) = \varphi_5(x,t_2) + \frac{\partial \varphi_5(x,t_2)}{\partial y}\cdot (y-t_2) + \frac{\partial^2 \varphi_5(x,t_2)}{2\cdot \partial y^2}\cdot (y-t_2)^2. \tag{11}$$

Substituting Eqs. (1)–(5) into Eqs. (9)–(11) leads to a general differential equation for the surface potential distribution function as

$$\frac{\partial^2 \varphi_i(x,0)}{\partial x^2} - \frac{\varphi_i(x,0)}{t^2} = -\frac{qN_{i,eff}}{\varepsilon_s}, \quad i = 1,2,3, \tag{12}$$

where $N_{1,eff} = N_{3,eff} = N_{nwell}$, and $N_{2,eff} = N_{nwell} - \eta_1 N_{PB} + \eta_2 N_T$. The t, η_1, and η_2 denote the characteristic thickness value of drift region, the vertical doping factors of P-buried layer, and N-top layer, respectively, and are given as follows:

$$t = \sqrt{0.5t_d^2 + Kt_d t_{ox}}, \tag{13}$$

$$\eta_1 = \frac{1}{t^2}\cdot\left[(t_d + Kt_{ox})\cdot(t_2 - t_1) - \frac{1}{2}\left(t_2^2 - t_1^2\right)\right], \tag{14}$$

$$\eta_2 = \frac{1}{t^2}\cdot\left[(t_d + Kt_{ox})\cdot t_1 - \frac{1}{2}t_1^2\right]. \tag{15}$$

Solving Eq. (12) constrained by Eqs. (6)–(8) yields the distributions of surface potential and electric field as follows:

$$\varphi(x.0) = V_{i,eff} + (V_i - V_{i,eff}) \times \frac{\sinh\left((x - L_{i-1})/t\right)}{\sinh\left((L_i - L_{i-1})/t\right)} + (V_{i-1} - V_{i,eff}) \times \frac{\sinh\left((L_i - x)/t\right)}{\sinh\left((L_i - L_{i-1})/t\right)}, \quad L_{i-1} \le x \le L_i, \tag{16}$$

$$E(x,0) = (V_i - V_{i,\text{eff}}) \cdot \frac{\cosh((x-L_{i-1})/t)}{t\sinh((L_i-L_{i-1})/t)} - (V_{i-1}-V_{i,\text{eff}}) \times \frac{\cosh((L_i-x)/t)}{t\sinh((L_i-L_{i-1})/t)}, \quad L_{i-1} \le x \le L_i, \tag{17}$$

where $i = 1, 2, 3$ and $L_{i-1} \le x \le L_i$, $V_{i,\text{eff}} = qN_{i,\text{eff}}t^2/\varepsilon_s$, $V_0 = 0$, $V_3 = V_d$, $L_0 = 0$, $L_3 = L_d$, and $y = 0$. The L_1 and L_2 are the positions of two boundaries between N-well and N-top layer. The V_1 and V_2 are the surface potentials of two boundaries between drift region and N-top layer and can be obtained from the condition (Eqs. (6) and (7)). It is worth nothing that the analytical expressions Eq. (16) and Eq. (17) are also applicable to other devices without being modified, such as single ($N_{PB} = 0$, $N_T = 0$), double ($t_1 = 0$) and conventional triple RESURF ($N_T = 0$) SOI LDMOS.

Solving the potential function partial respect to y and substituting it into Eqs. (1) and (2), the vertical electric field distributions can be described as

$$E_{iy}(x,y) = \frac{\varphi_i(x,0)}{t^2} \cdot y, \quad i = 1,3, \tag{18}$$

$$E_{2y}(x,y) = \xi \cdot y, \quad 0 \le y \le t_1, \tag{19}$$

$$E_{4y}(x,y) = \xi \cdot y - \frac{q(N_T + N_{PB})}{\varepsilon_s} \cdot (y - t_1), \quad t_1 \le y \le t_2, \tag{20}$$

$$E_{5y}(x,y) = \xi \cdot y - \frac{qN_T}{\varepsilon_s} \cdot (y - t_2) - \frac{q(N_T + N_{PB})}{\varepsilon_s} \cdot (t_2 - t_1), \quad t_2 \le y \le t_d, \tag{21}$$

where

$$\xi = \varphi_2(x,0)/t_2 + q(\eta_1 N_{PB} - \eta_2 N_T + N_T)/\varepsilon_s.$$

For the novel triple RESURF SOI LDMOS, the peak field at O_2 in the N-top/N-well junction is larger than that at O_3in the N-well/N^+-drain junction because the P-buried layer is introduced and lengths of N-top layer and P-buried layer are close to the length of drift region. Therefore, there are two surface electric field peaks at O_1 and O_2. The lengths of P-buried layer and N-top layer are both almost equal to the length of drift region. So assuming $L_1 = 0$ and $L_2 = L_d$, the vertical breakdown can only occur at either O_4 or O_5. The electric field at O_4 for the N-top/P-buried junction is larger than that at O_2 due to the influence of vertical electric field at O_4. Hence, the lateral breakdown voltage BV_{lat} can be obtained from $E(0,0) = E_c$ when the breakdown occurs at O_1. The BV_{lat} can be described as:

$$BV_{lat} = \sinh(L_d/t) \cdot t \cdot E_c - [\cosh(L_d/t) - 1] \cdot \frac{qt^2 N_{nwell}}{\varepsilon_s} + \{\cosh[(L_d - L_1)/t] - \cosh[(L_d - L_2)/t]\} \cdot \frac{qt^2(\eta_1 N_{PB} - \eta_2 N_T)}{\varepsilon_s}. \tag{22}$$

Besides, the vertical breakdown voltage BV_{ver1} can be obtained from $E_{2y}(L_1,t_1) = E_c$ when the breakdown occurs at O_4, and BV_{ver2} can be obtained from $E_{5y}(L_2,t_d) = E_c$ when the breakdown occurs at O_5. The BV_{ver1}, BV_{ver2}, and BV are given as follows:

$$BV_{ver1} = \frac{t^2 \cdot E_c}{t_d} - \frac{q(\eta_1 N_{PB} - \eta_2 N_T + N_T) \cdot t^2}{\varepsilon_s} + \frac{t^2[qN_T(t_d - t_1) + qN_{PB}(t_2 - t_1)]}{\varepsilon_s \cdot t_d}, \tag{23}$$

$$BV_{ver2} = \frac{t^2 \cdot E_c}{t_1} - \frac{q(\eta_1 N_{PB} - \eta_2 N_T + N_T) \cdot t^2}{\varepsilon_s}, \tag{24}$$

$$BV = \text{Min}[BV_{lat}, BV_{ver1}, BV_{ver2}]. \tag{25}$$

The analytical Q_{ntop} can be obtained when the N-well is fully depleted and the breakdown occurs at O_4. The Q_{ntop} includes the charges of N-well and N-top layer. The vertical depletion extension d_1 into the N-top layer can be given as follows:

$$d_1 = \frac{\varepsilon_s E_c}{q(N_{nwell} + N_T)}. \tag{26}$$

The optimal Q_{ntop} for the N-top layer is expressed as

$$Q_{ntop} \le (N_{nwell} + N_T) d_1 = \frac{\varepsilon_s E_c}{q}. \tag{27}$$

3. Results and discussion

In this paper, all the numerical results are obtained by 2D device simulator MEDICI and the analytical results are obtained by the analytical model. Figures 2(a) and 2(b) show the numerical and analytical profiles of surface potential and electric field for the novel and conventional triple RESURF SOI LDMOS, respectively. The novel and conventional triple RESURF SOI LDMOS obtain BV values of 450 V and 454 V, respectively. A fair accordance between the analytical and numerical profiles of surface potential and electric field may generally be found for the novel and conventional triple RESURF SOI LDMOS. For the novel triple RESURF SOI LDMOS, the heavily doped N-top layer results in a weak increase of the peak electric field in P-well/N-well junction. Because the P-buried layer is introduced and the lengths of N-top layer and P-buried layer are close to the length of drift region, the surface peak field at the N-top/N-well junction is larger than that at the N-well/N^+-drain junction. Figures 2(c) and 2(d) show the numerical and analytical profiles of surface potential and electric field for the single and double RESURF SOI LDMOS, respectively. The analytical expressions (16) and (17) can be simply used in single ($N_{PB} = 0$, $N_T = 0$) and double ($t_1 = 0$) RESURF SOI LDMOS without being modified. The single and double RESURF SOI LDMOS obtain BV values of 445 V and 447 V, respectively. The analytical results of surface potential and electric field distributions for single and double RESURF SOI LDMOS show good agreement with the numerical simulation results.

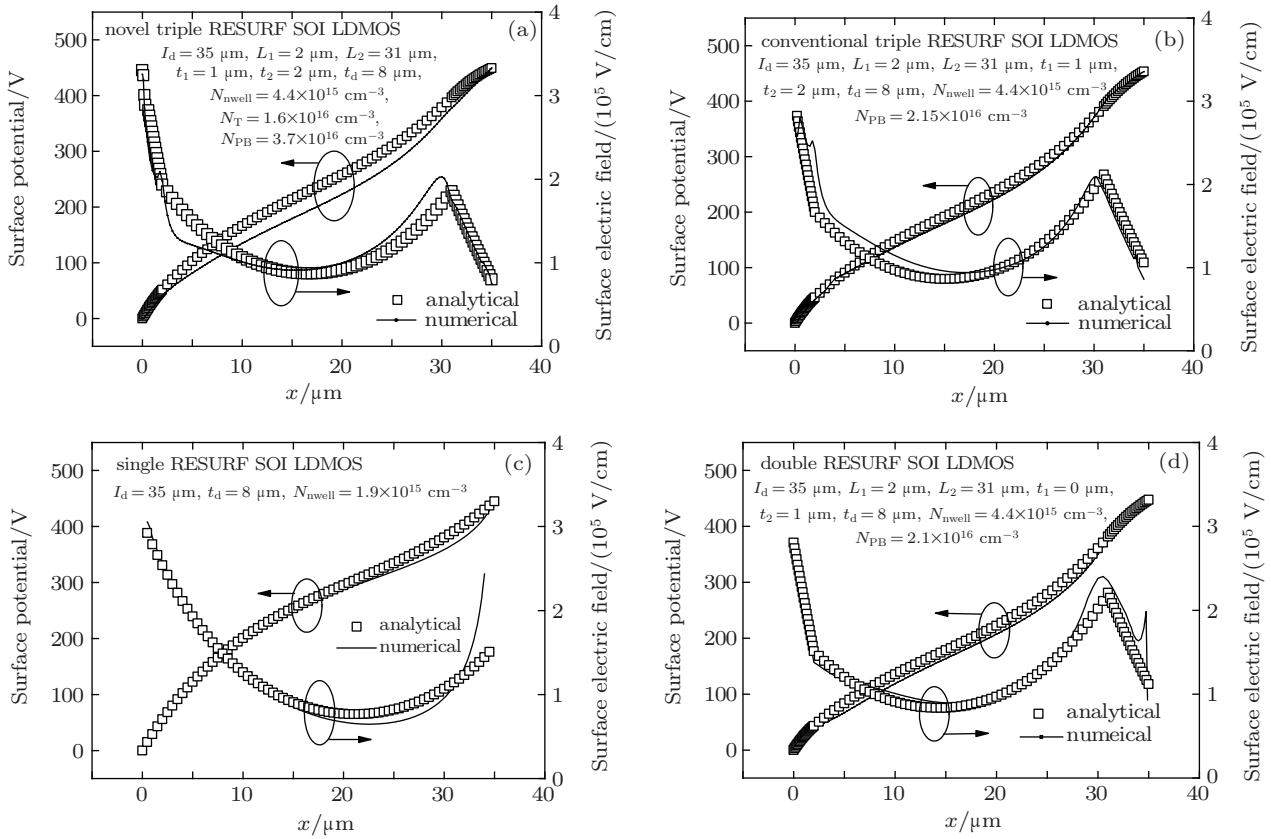


Fig. 2. Numerical and analytical profiles of surface potential and electric field of (a) novel triple RESURF SOI LDMOS, (b) conventional triple RESURF SOI LDMOS, (c) single RESURF SOI LDMOS, and (d) double RESURF SOI LDMOS in drift region.

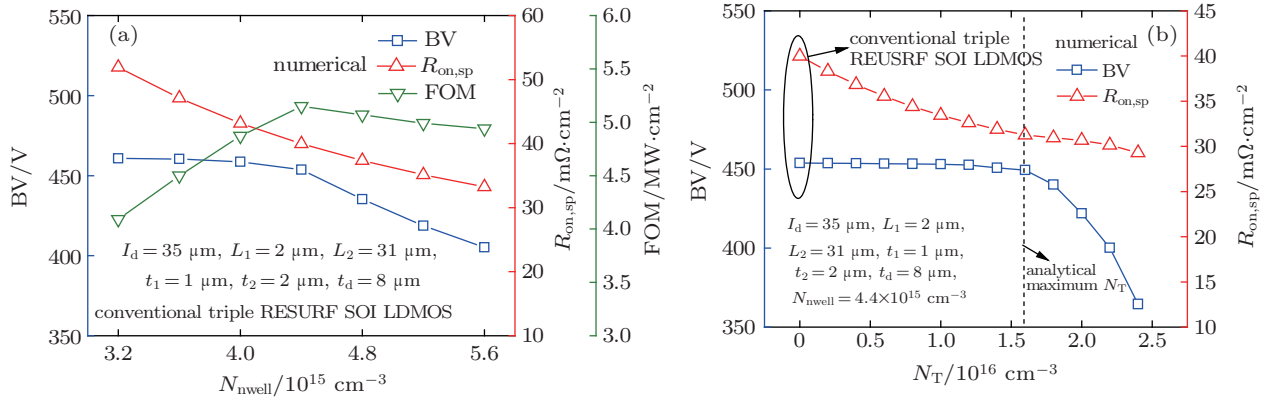


Fig. 3. (color online) (a) Numerical results of BV, $R_{on,sp}$, and FOM versus N_{nwell} for conventional triple RESURF SOI LDMOS, (b) numerical results of BV and $R_{on,sp}$ versus N_T for novel and conventional triple RESURF SOI LDMOS, and analytical maximum N_T.

Figure 3(a) shows the numerical results of BV, $R_{on,sp}$, and power figure of merit (FOM, defined as $BV^2/R_{on,sp}$) versus N_{nwell} for the conventional triple RESURF SOI LDMOS with $L_d = 35$ μm, $L_1 = 2$ μm, $L_2 = 31$ μm, $t_1 = 1$ μm, $t_2 = 2$ μm, and $t_d = 8$ μm. The conventional triple RESURF SOI LDMOS has a correspondingly optimized N_{PB} for any given N_{nwell}. $R_{on,sp}$ decreases with the increase of N_{nwell}. With the increase of N_{nwell} from 3.2×10^{15} cm^{-3} to 4.4×10^{15} cm^{-3}, BV is maintained at a similar value of above 450 V firstly. With the continuous increase of N_{nwell} from 4.4×10^{15} cm^{-3} to 5.6×10^{15} cm^{-3}, BV decreases. With $N_{nwell} = 4.4\times10^{15}$ cm^{-3}, the conventional triple RESURF SOI LDMOS obtains a BV of 454 V and a $R_{on,sp}$ of 40 mΩ·cm^2, yielding a highest FOM of 5.15 MW/cm^2. Figure 3(b) shows the numerical results of BV and $R_{on,sp}$ versus N_T for the novel and conventional triple RESURF SOI LDMOS, and analytical maximum N_T with $L_d = 35$ μm, $L_1 = 2$ μm, $L_2 = 31$ μm, $t_1 = 1$ μm, $t_2 = 2$ μm, $t_d = 8$ μm, and $N_{nwell} = 4.4\times10^{15}$ cm^{-3}. When $N_T = 0\times10^{16}$ cm^{-3}, the device is a conventional triple RESURF SOI LDMOS which achieves a BV of 454 V and a $R_{on,sp}$ of 40 mΩ·cm^2. As N_T increases, the N-top layer is formed. BV can maintain the same value, and $R_{on,sp}$ de-

creases because an additional N-top layer introduces more majority carriers to significantly reduce $R_{on,sp}$, which alleviates the inherent tradeoff between $R_{on,sp}$ and BV. Then, BV decreases whenN_T continues to increase. For any given N_T, the device has a correspondingly optimized N_{PB} when the drift region is fully depleted. When N_T is 1.6×10^{16} cm^{-3}, the novel triple RESURF SOI LDMOS can achieve a low $R_{on,sp}$ of 31.3 m$\Omega\cdot$cm^2 which is 22% lower than that of conventional triple RESURF SOI LDMOS at the same BV level. According to Eq. (27), with $t_1 = 1$ μm, the analytical maximum N_T is 1.56×10^{16} cm^{-3}. When N_T exceeds the value, BV decreases with the increase of N_T.

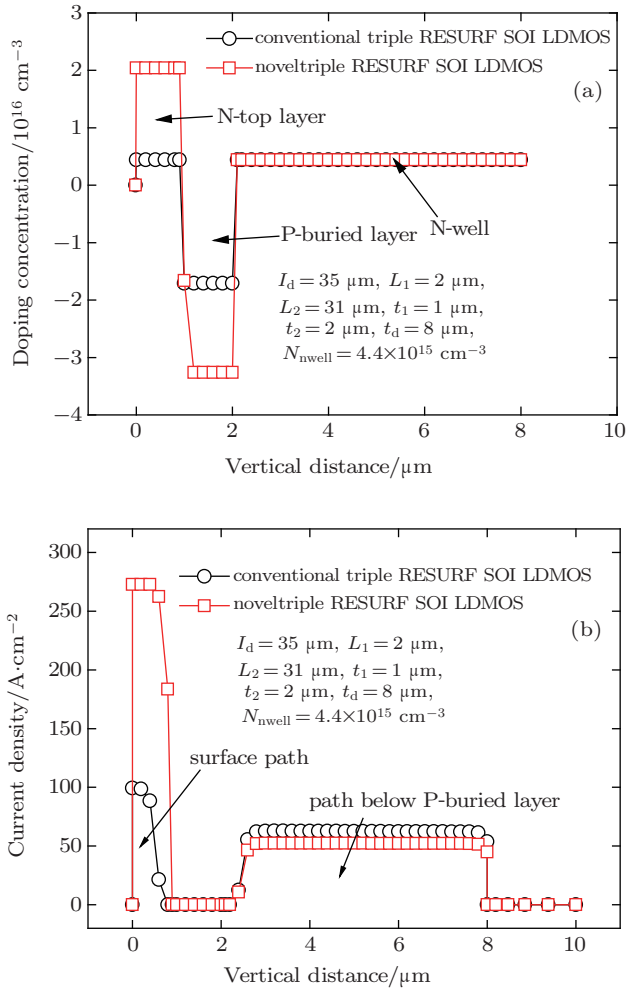


Fig. 4. (color online) (a) Numerical vertical doping concentrations and (b) corresponding current density distributions in the drift region at $x = 25$ μm for the novel and conventional triple RESURF SOI LDMOS.

Figure 4(a) shows the numerical vertical doping profiles in the drift region for the novel and conventional triple RESURF SOI LDMOS with $L_d = 35$ μm, $L_1 = 2$ μm, $L_2 = 31$ μm, $t_1 = 1$ μm, $t_2 = 2$ μm, $t_d = 8$ μm, and $N_{nwell} = 4.4\times10^{15}$ cm^{-3}. With an extra N-top layer, the novel triple RESURF SOI LDMOS has more majority carriers at the surface of N-well than the conventional triple RESURF SOI LDMOS. Meanwhile, in order to keep charge balance for a high BV, the increased N_{PB} is needed. The two structures have similar doping profiles of N-well below P-buried layer due to the same N_{nwell}. Figure 4(b) shows the corresponding current density distributions. Currents passing through the path below P-buried layer maintain for the two structures are approximately the same. However, current passing through the surface path of the novel triple RESURF SOI LDMOS is increased by near 175% in comparison with that of the conventional triple RESURF SOI LDMOS. Hence, the N-top layer provides a low on-resistance surface conduction path for the novel triple RESURF SOI LDMOS, contributing to a lower $R_{on,sp}$. Therefore, compared with the conventional triple RESURF SOI LDMOS, the novel triple RESURF SOI LDMOS with N-top layer can achieve a lower $R_{on,sp}$ while maintaining a high BV.

Figure 5 shows the numerical and analytical results of BV and numerical results of $R_{on,sp}$ versus N_{PB} at different values of N_T for the novel triple RESURF SOI LDMOS when $L_d = 35$ μm, $L_1 = 2$ μm, $L_2 = 31$ μm, $t_1 = 1$ μm, $t_2 = 2$ μm, $t_d = 8$ μm, and $N_{nwell} = 4.4\times10^{15}$ cm^{-3}. For the numerical results, with increase in N_{PB}, BV has a maximum value when the N-well is fully depleted for any given N_T. The $R_{on,sp}$ is almost constant with the increase of N_{PB} due to the nearly equivalent n-type impurity in the n-type drift region. As N_T increases, $R_{on,sp}$ is reduced for the same BV first. Then, BV decreases when N_T continues to increase. The analytical BV values obtained from Eqs. (22)–(25), when the device is fully depleted, accord with the numerical results, showing the validity of the presented model.

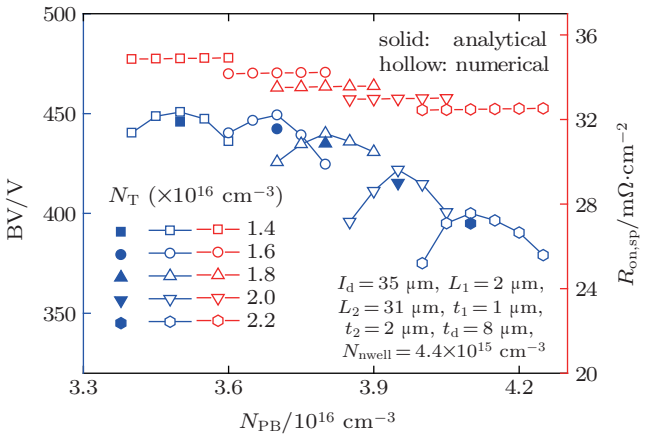


Fig. 5. (color online) Numerical and analytical results of BV and numerical results of $R_{on,sp}$ versus N_{PB} at different N_T values for the novel triple RESURF SOI LDMOS.

Figure 6 shows the numerical results of BV versus Q_{ntop} at different values of t_1 for the novel triple RESURF SOI LDMOS and the analytical maximum Q_{ntop} when $L_d = 35$ μm, $L_1 = 2$ μm, $L_2 = 31$ μm, $t_d = 8$ μm, and $N_{nwell} = 4.4\times10^{15}$ cm^{-3}. The thickness of P-buried layer in the simulations is 1 μm. With the increase of Q_{ntop}, the BV can be first maintained at a similar value and then decreases because of too

high a dose of N-top layer. According to Eq. (27), the analytical maximum $Q_{\rm ntop}$ is $\varepsilon_{\rm s}E_{\rm c}/q$. The analytical maximum $Q_{\rm ntop}$ is an upper theoretical bound for the dose of surface conduction path, which can guide the designer in achieving an optimal distribution of impurities in the drift region to optimize the tradeoff between the BV and $R_{\rm on,sp}$. The critical electric field $E_{\rm c}$ is a weak function of the doping. With the decrease of t_1, the concentration of the N-top layer will increase at the same $Q_{\rm ntop}$, which causes the increase of $E_{\rm c}$. So, the analytical maximum $Q_{\rm ntop}$ will increase with the decrease of t_1. The analytical maximum $Q_{\rm ntop}$ values are obtained at different t_1 values and are also shown in Fig. 6. With $t_1 = 1.0$ μm, the analytical maximum $Q_{\rm ntop}$ is around 2.0×10^{12} cm^{-2}. Hence, compared with the conventional triple RESURF SOI LDMOS, the novel triple RESURF SOI LDMOS can maintain a high BV and a lower $R_{\rm on,sp}$ with $Q_{\rm ntop} \leq 2.0\times10^{12}$ cm^{-2} at $t_1 = 1.0$ μm.

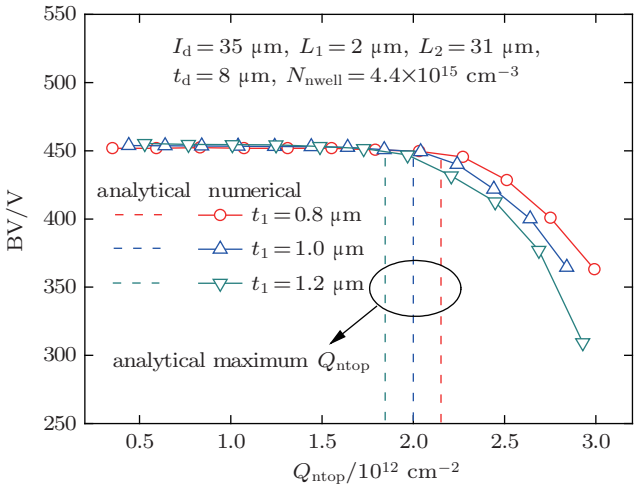


Fig. 6. (color online) Numerical results of BV versus $Q_{\rm ntop}$ at different t_1 values for novel triple RESURF SOI LDMOS and the analytical maximum $Q_{\rm ntop}$.

4. Conclusions

In this work, an analytical model for the surface potential and electric field distributions of the novel triple RESURF SOI LDMOS with N-top layer are presented. The corresponding analytical model for the surface potential and electric field distributions are also applicable to single, double and conventional triple RESURF SOI structures. Besides, the analytical BV and maximum $Q_{\rm ntop}$ are obtained. The analytical maximum $Q_{\rm ntop}$ is an upper theoretical bound which is useful to control the implantation doses and energy for the N-top layer. All the analytical results obtained from the given expressions can show fair agreement with the numerical results, indicating the validity of the presented model. Consequently, the proposed analytical model can be a good tool for the designer to optimize the novel triple RESURF SOI LDMOS with N-top layer. The novel triple RESURF SOI LDMOS can achieve a more optimized distribution of impurities in the drift region to further improve the tradeoff between BV and $R_{\rm on,sp}$ than the conventional triple RESURF SOI LDMOS.

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