Structure-dependent behaviors of diode-triggered silicon controlled rectifier under electrostatic discharge stress*

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The comprehensive understanding of the structure-dependent electrostatic discharge behaviors in a conventional diode-triggered silicon controlled rectifier (DTSCR) is presented in this paper. Combined with the device simulation, a mathematical model is built to get a more in-depth insight into this phenomenon. The theoretical studies are verified by the transmission-line-pulsing (TLP) test results of the modified DTSCR structure, which is realized in a 65-nm complementary metal–oxide–semiconductor (CMOS) process. The detailed analysis of the physical mechanism is used to provide predictions as the DTSCR-based protection scheme is required. In addition, a method is also presented to achieve the tradeoff between the leakage and trigger voltage in DTSCR.

Keywords: electrostatic discharge (ESD), diode-triggered silicon controlled rectifier (DTSCR), transmission-line-pulsing (TLP), mathematical modeling

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1. Introduction

Electrostatic discharge (ESD) remains a reliability issue in semiconductor industry with the critical dimension scaling down.[1,2] In order to meet the tighter requirements in advanced complementary metal–oxide–semiconductor (CMOS) process, the diode-triggered silicon controlled rectifier (DTSCR) device is widely used due to its design simplification and adjustable trigger/holding voltage. Besides, the extremely low parasitic capacitance makes the DTSCR more popular in high frequency applications with less influence on signal integrity.[3–8] The ESD behaviors of the conventional DTSCR structure are extensively investigated with the transmission line pulsing (TLP) test and device simulation.[9–14] Considering the structure-dependent characteristics, the analysis combined with an equivalent mathematic model is still needed.

In this paper, a kind of mathematical analysis model is presented to explore this problem in conjunction with device simulations. The relevant devices are verified in a 65-nm CMOS process and the test results are in good agreement with the theoretical discussions. In Section 2, TLP test results of the conventional DTSCR structure are provided and device simulations are used to explore operating mechanism. According to the physical process analyzed, the structure-sensitive mathematical model is established to investigate ESD behaviors in Section 3. On the basis of the proposed model, the performances of the novel device configuration are predicted and confirmed by the TLP test results shown in Section 4. Finally, the conclusions are reached in Section 5.

2. Operating mechanism under ESD stress

Figure 1 depicts the cross-section of the conventional DTSCR, which contains the intrinsic SCR and four external P^+/N-well diodes, denoted as D2, D3, D4, and D5 respectively. In the normal operation, the DTSCR is not allowed to be switched on and its leakage is strictly limited concerning the integrity of the transmitted signal as used in I/O protection. Compared with the junction leakage in the intrinsic SCR, the leakage of the coupled diodes occupies the biggest fraction before being fully switched on.[15–19] This is attributed to the amplification of multi-stage Darlington beta gain in the vertical parasitic PNP transistor.[20] Increasing the diode numbers can reduce the leakage at the expense of improved trigger voltage. The tradeoff needs to be considered well for effective protection. When an ESD event occurs, the diode chain first turns on due to its lower trigger voltage than that of the intrinsic SCR. This is attributed to the difference between their triggering mechanisms. The trigger voltage of the diode chain is determined by the stacked diode cut-in voltage, while that of the intrinsic SCR is ascribed to the p-n junction breakdown voltage. The diode chain's conducting current will trigger a parasitic SCR consisting of the P^+/N-well in D1, P-substrate and N-well in D5, at a smaller current level than that required in the intrinsic SCR.[21] When the intrinsic SCR is turned on, most of the ESD current flows through this low-resistance path and the core circuits are protected from being affected by the ESD-induced transient voltage.

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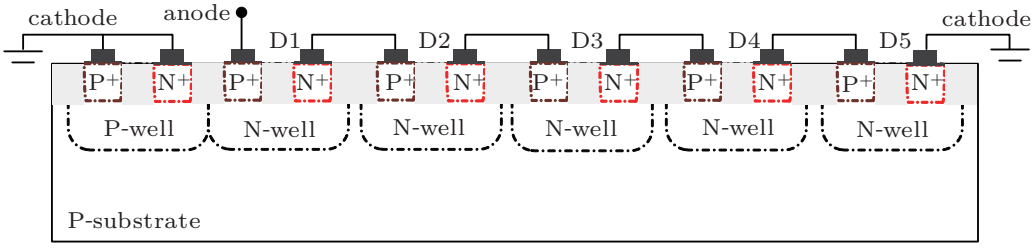


Fig. 1. (color online) Cross-section view of the conventional DTSCR device.

TLP system is used to produce as short as 100-ns pulses to investigate the ESD behaviors of the device under test. The critical characteristics can be observed in the *I*–*V* curve, such as the trigger current, holding current, the secondary breakdown current, etc.

Figure 2 shows a comparison between the TLP test and simulated results of the conventional DTSCR. The "S"-shape behavior is observed in the experimental *I*–*V* curve, which indicates the switching process from the blocked to latched state in the intrinsic SCR. A low-resistance route is formed to discharge the majority of the current and the transient voltage is clamped to a safe value. The two-dimensional (2D) device simulations are performed to reveal the underlying physics through using the TCAD tools. Pulses are used as the input signal to obtain the equivalent voltage averaged between 60 ns and 90 ns at the anode.[22] The simulated *I*–*V* curve correlates well with that of the test results. Considering its snapback behavior, we analyze the state-transition procedure with the pulses of 0.6 mA/μm and 20 mA/μm, respectively. The selected points are marked in Fig. 2.

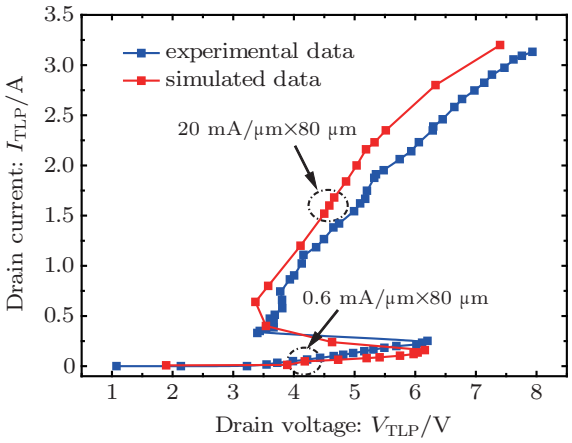


Fig. 2. (color online) Comparison of *I*–*V* behavior between experimental and simulated results of the conventional DTSCR with a width of 80 μm.

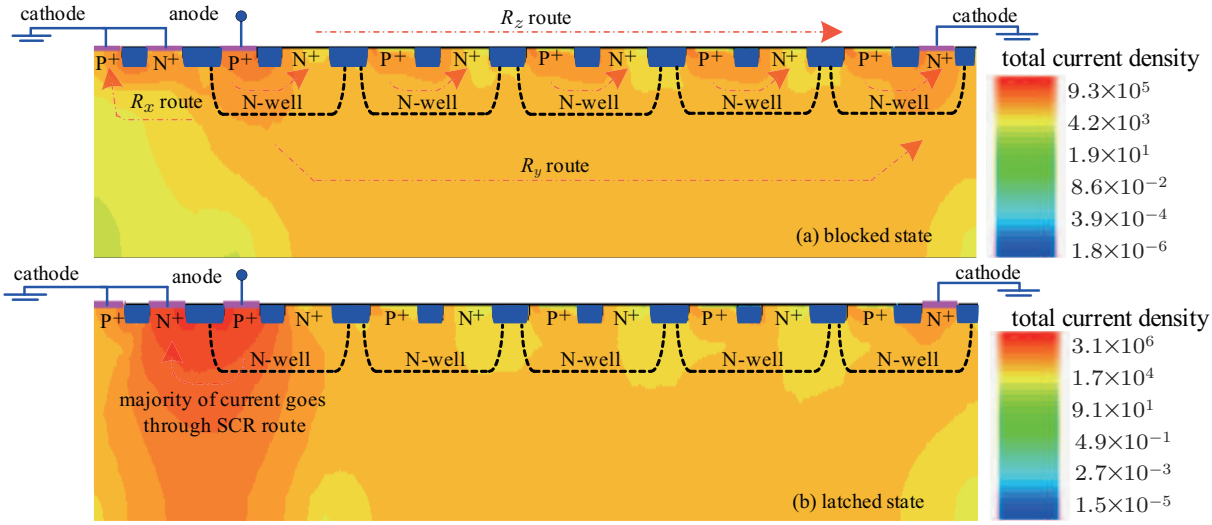


Fig. 3. (color online) Total current densities procured at 100ns as the intrinsic SCR stays at (a) blocked and (b) latched state under the pulse of 0.6 mA/μm and 20 mA/μm, respectively.

Figure 3 shows the total current density at the two marked points. In Fig. 3(a), three current paths can be seen as the intrinsic SCR is at a blocked state. Combined with the operating mechanism under ESD stress, the diode chain first conducts current, and its parasitic resistance is denoted as R_z. Then the current flows through the parasitic SCR and the substrate contact with the parasitic resistances marked as R_y and R_x, respectively. The potential drop is formed across the N+ and P^+ areas of the intrinsic SCR due to the existence of R_x, and the potential increase is corresponding to the improved pulse amplitude. A low-resistance path will take shape when the potential drop is large enough to forward bias the barrier in the N^+/P-well contact area. As a consequence, the intrinsic SCR is transformed from blocked to the latched state, which is illus-

trated in Fig. 3(b). In conclusion, the underlying physics can be confirmed and summarized as follows: as an ESD event occurs, the coupled diodes are turned on to discharge current, and then the substrate collected current will be used to drive the parasitic and intrinsic SCR according to Darlington effect. Based on the above discussion, the turn-on process of the conventional DTSCR seems to result from the current division between the parasitic SCR and the substrate contact. Therefore, a mathematical model is needed to get an insight into this problem, and the details are analyzed in Section 3.

3. Mathematical model analysis and 2D device simulation

The mathematical model of the conventional DTSCR is established to explore the influence of structure-dependent parasitic resistance on current division in the substrate, which was mentioned in Section 2. Compared with the model in previous research, the proposed mathematical model takes the parasitic SCR resistance into consideration. In addition, the influences of the critical parameters on the parasitic SCR resistance are also discussed. The cross-section and its equivalent circuit of the proposed model are depicted in Figs. 4(a) and 4(b), respectively. Three current paths are marked in Fig. 4, which are named I_x, I_y, and I_z respectively according to the parasitic resistance definitions of R_x, R_y, and R_z as shown in Fig. 3.

It is assumed that each diode cut-in voltage is identical, and R_0 is the parasitic resistance between adjacent N-wells on the condition that the conducting current is I_{y0}. If the transport current is changed into αI_{y_0} $(\alpha > 0)$, then the equivalent resistance will be R_0/α based on Ohm's law. Under these assumptions, R_y can be expressed as

$$R_y = R_0 \times \left(1 + \frac{1}{1+\alpha_1} + \frac{1}{1+\alpha_1+\alpha_2} + \frac{1}{1+\alpha_1+\alpha_2+\alpha_3}\right), \tag{1}$$

where I_{y0}, $\alpha_1 I_{y0}$, $\alpha_2 I_{y0}$, and $\alpha_3 I_{y0}$ $(\alpha_1 > 0,\ \alpha_2 > 0,\ \alpha_3 > 0)$ represent the current components in the parasitic SCR route. The conventional DTSCR structure is set as structure (a), and its R_y is named R_y (a), which is expressed in Eq. (1). Insert a large space into the coupled diodes of the structure (a), and R_y expression will be adjusted correspondingly. The modified DTSCR structures are named structures (b), (c), (d), and (e) in the sequence as indicated by the inserted positions from right to left. Therefore, the corresponding R_y's will be R_y (b), R_y (c), R_y (d), and R_y (e), which are determined by the following formulas:

$$R_y\,(\mathrm{b}) = R_0 \times \left(1 + \frac{1}{1+\alpha_1} + \frac{1}{1+\alpha_1+\alpha_2} + \frac{K}{1+\alpha_1+\alpha_2+\alpha_3}\right), \tag{2}$$

$$R_y\,(\mathrm{c}) = R_0 \times \left(1 + \frac{1}{1+\alpha_1} + \frac{K}{1+\alpha_1+\alpha_2} + \frac{1}{1+\alpha_1+\alpha_2+\alpha_3}\right), \tag{3}$$

$$R_y\,(\mathrm{d}) = R_0 \times \left(1 + \frac{K}{1+\alpha_1} + \frac{1}{1+\alpha_1+\alpha_2} + \frac{1}{1+\alpha_1+\alpha_2+\alpha_3}\right), \tag{4}$$

$$R_y\,(\mathrm{e}) = R_0 \times \left(K + \frac{1}{1+\alpha_1} + \frac{1}{1+\alpha_1+\alpha_2} + \frac{1}{1+\alpha_1+\alpha_2+\alpha_3}\right). \tag{5}$$

As mentioned above, R_0 is proportional to the space between the neighboring N-wells, and it will be $K \times R_0$ if the space is changed, where K is a constant, $K > 1$ if the space is extended and $K < 1$ if it is shortened.

From structures (a) to (e), R_x remains the same and R_y is regularly increased on the basis of math model analysis. Considering the extremely low resistivity in metal, the value of R_z keeps constant. That is to say, only the R_y is structure-sensitive in this situation. The Related device simulations are well performed to confirm the principle of dynamic variation of the parasitic resistance before the intrinsic SCR is triggered on. A current pulse of 0.6 mA/μm is used to investigate the current paths in these structures and the simulated current density of each device is depicted in Fig. 5.

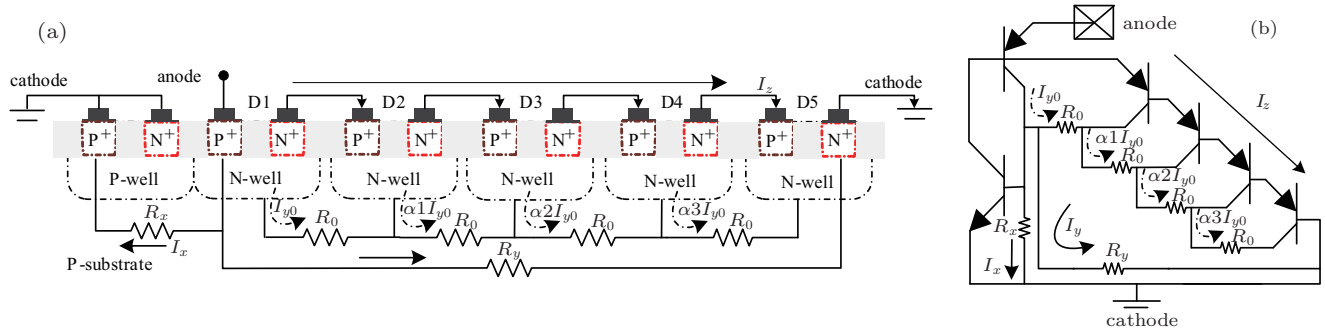


Fig. 4. (color online) Mathematical analysis model in (a) cross-section and (b) equivalent circuit of the conventional DTSCR.

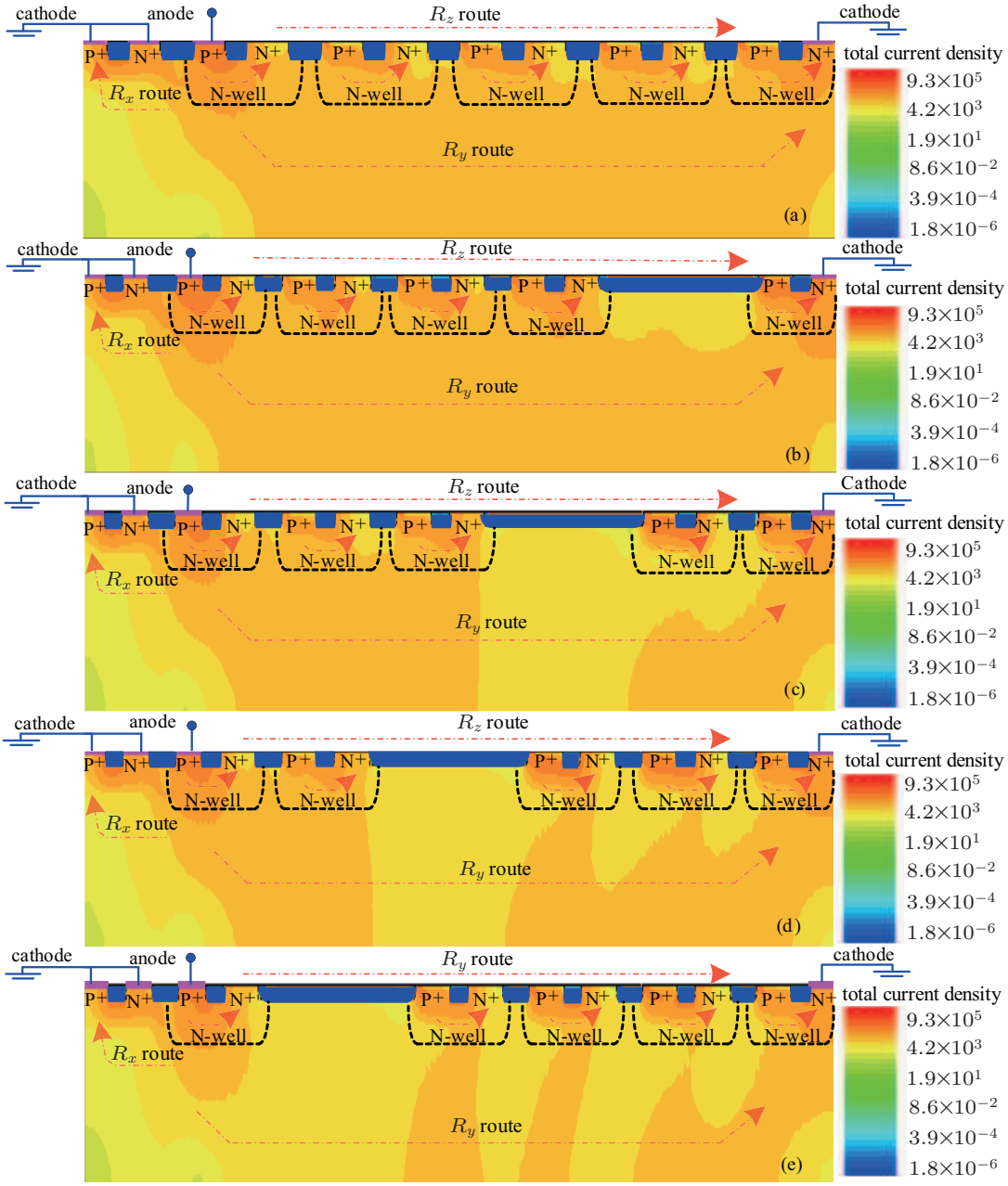


Fig. 5. (color online) Total current densities at 100 ns when the intrinsic SCR is at blocked state under the pulse of 0.6 mA/μm.

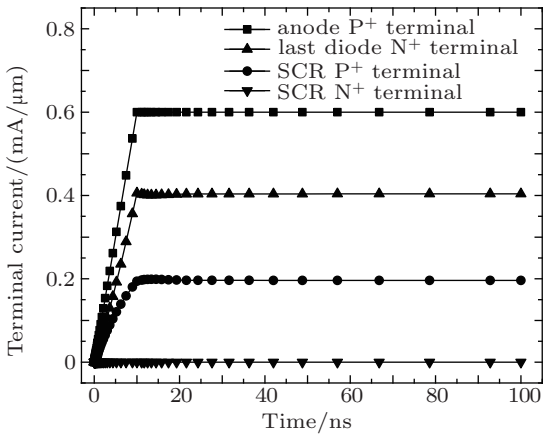


Fig. 6. Curves of simulated terminal current versus time, which are extracted from DTSCR structure (a) under a pulse of 0.6 mA/μm.

The three similar current routes are observed among these structures. Meanwhile, the distinctions cannot be ignored in the contour lines of current density. It can be concluded that changes of the structure have no influence on the ESD-related physical process, but have an effect on the total current division in the mentioned three paths. This qualitatively validates the discussion in the proposed math model. For a more in-depth insight into this phenomenon, a quantitative relation is still needed. Therefore, terminal currents of the conventional DTSCR structure (a) are extracted and depicted in Fig. 6.

Figure 6 shows the current at each terminal of the DTSCR structure (a). I_x is marked as SCR P^+ terminal current and the sum of I_y and I_z is the last diode N^+ terminal current. Considering the blocked state of intrinsic SCR, no current exists in

the SCR N^+ terminal. According to the math model analysis, the sum of I_y and I_z should be regularly reduced as the consequence of the increased R_y from structures (a) to (e). Correspondingly, the I_x increases as analyzed. The current variations in correspondence to the modified structures are consistent with the model discussion, and the curves of current versus time are displayed in Fig. 7.

In Fig. 7, I_x is increased from structures (a) to (e) as analyzed. The higher the value of I_x, the larger the potential drop that is formed across the N^+ and P^+ regions of the intrinsic SCR will be. Two points near the source region are selected to confirm this assertion in Fig. 8, the potential difference between these two points is raised as the value of I_x increases. When it is large enough to forward bias the barrier inside the N^+/P-well contact area, the intrinsic SCR will be switched on and a low-resistance path is formed to discharge most of the current.

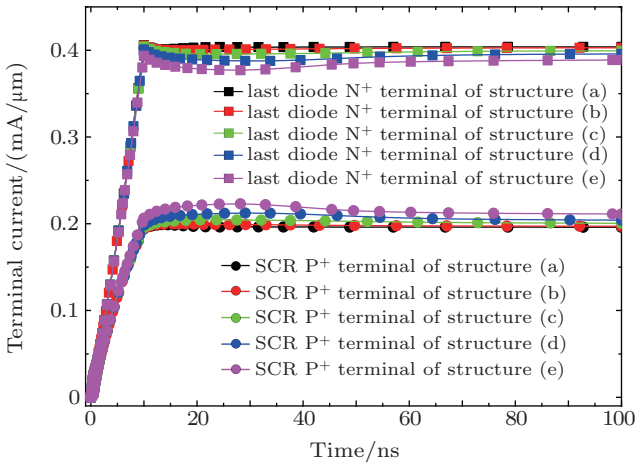


Fig. 7. (color online) Curves of simulated terminal current versus time, which change with the device structure under a pulse of 0.6 mA/μm.

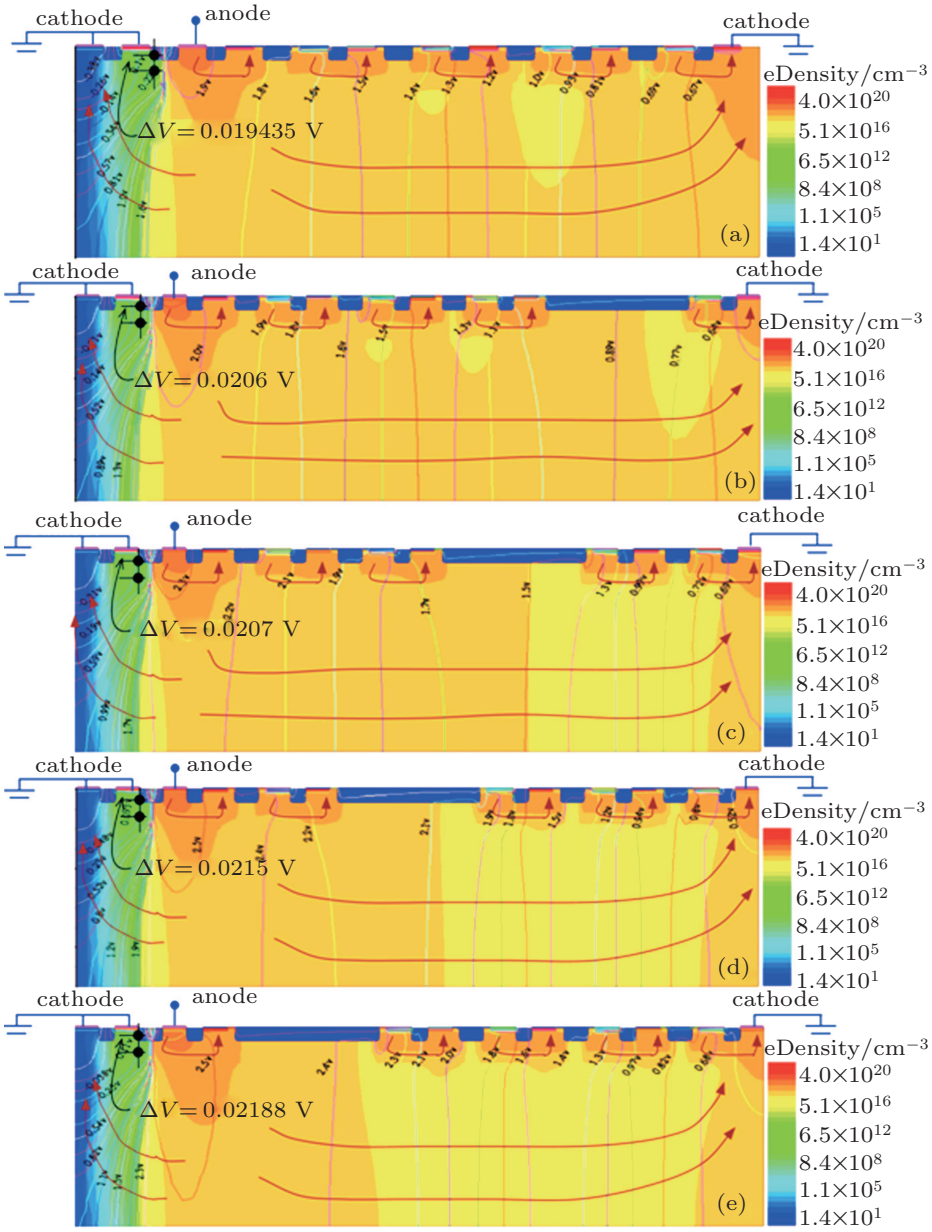


Fig. 8. (color online) Electron density distributions each with potential contour lines, voltage drops between two adjacent black dots are 0.019435 V, 0.0206 V, 0.0207 V, 0.0215 V, and 0.02188 V from structures (a) to (e), respectively.

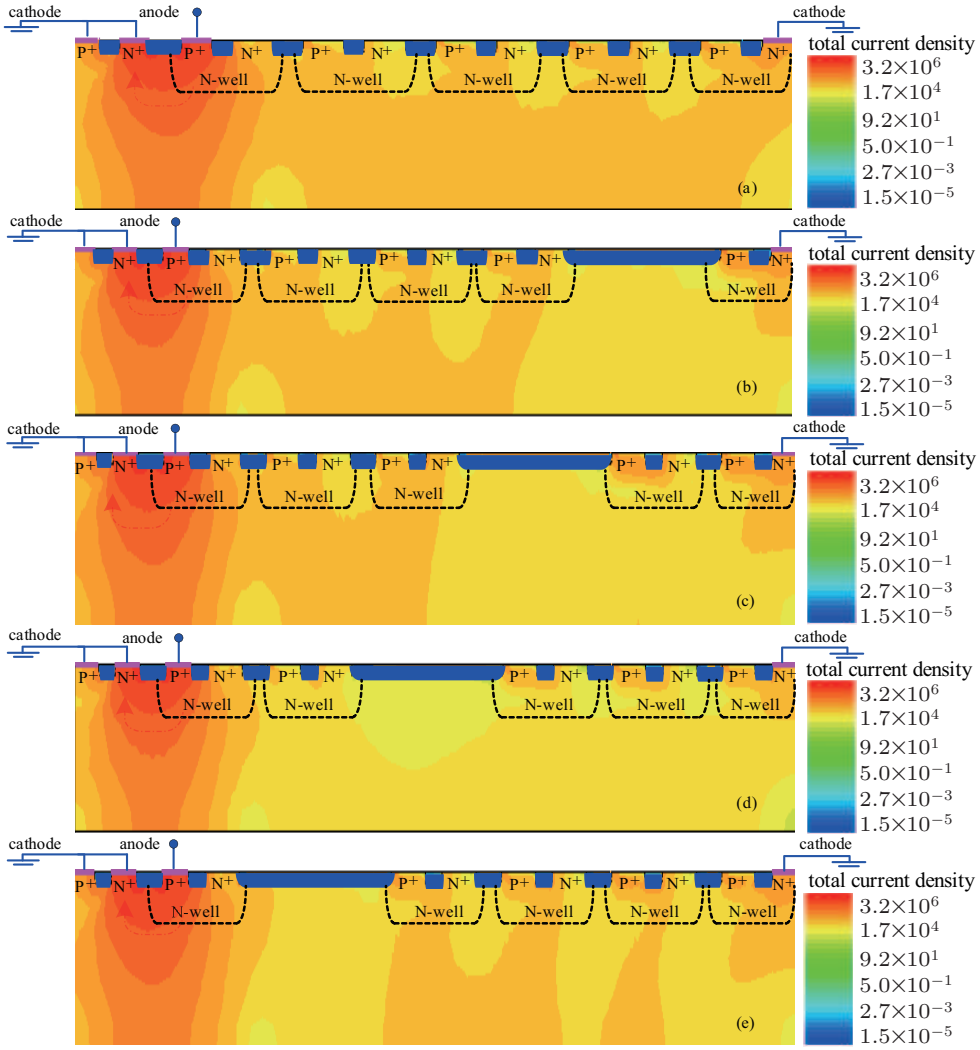


Fig. 9. (color online) Total current density distributions at 100 ns when the intrinsic SCR is at a latched state under a pulse of 20 mA/μm.

Figure 8 depicts the electron density distributions each with potential contour lines, in which the simulated potential drops between the two marked adjacent points are 0.019435 V, 0.0206 V, 0.0207 V, 0.0215 V, and 0.02188 V from structures (a) to (e), respectively. Considering the same potential barrier, the trigger current is regularly reduced with structure variation and this rule is verified by the following TLP test results indicated in Fig. 10. Then the transient voltage is clamped to a safe value due to the turn-on of intrinsic SCR, and this process can be achieved from the distribution of the current density in Fig. 9.

Figure 9 depicts the total current density distributions procured at 100 ns under a pulse of 20 mA/μm. The extremely high current density exists in the intrinsic SCR route, which indicates that a low-resistance path is formed to shunt the majority of the current. Thus a comparatively large voltage switching occurs and the overshoot potential is finally limited to an acceptable level, which can be observed in Fig. 10.

4. TLP measurements and verification

The tested DTSCR structures are fabricated in a 65-nm CMOS process. The widths of all devices are selected to be 80 μm. Compared with the normal space 1.5 μm between adjacent N-wells, the mentioned large space is set to be 6×1.5 μm. Figure 10 shows the TLP test results: the trigger current decreases from structures (a) to (e), and the difference between the maximum and minimum values is 1 mA/μm. Meanwhile, the total parasitic resistance increases based on the model analysis. It is the multi-factors that result in the regular decrease in trigger voltage. The "S"-shape behavior in each of *I*–*V* TLP curves is also observed, which can be summarized as the state-transition of the intrinsic SCR. Considering the same incorporated SCRs, the secondary breakdown currents are identical among these devices. The TLP characteristics of the test structures are consistent with the model analyses and device simulations. Moreover, the balance between the leakage and trigger voltage can be well handled by inserting a large space into the coupled diodes, and the in-

serted position can be flexibly changed to meet different requirements.

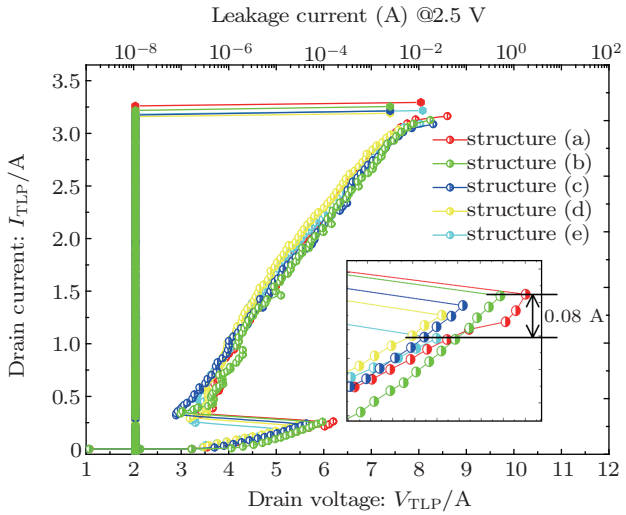


Fig. 10. (color online) TLP characteristics of the DTSCR structures in 80 μm device width.

5. Conclusions

The turn-on processes of the DTSCR structures under ESD stress are investigated in detail. Compared with the device simulation, a mathematical model is proposed to get a more in-depth insight into the structure-dependent TLP characteristics. This proposed mathematical model can be smoothly applied to other technologies. With a large space inserted into the coupled diodes, the novel DTSCRs are constructed and taped out in a 65-nm CMOS process. On the basis of the model analysis, the prediction of the related ESD behaviors is provided and finally verified by the device simulations and TLP test results. The detailed discussion may offer an effective instruction when the DTSCR-based ESD protection is needed. Meanwhile, the method is also presented to solve the problem about the tradeoff between the leakage and trigger voltage in DTSCRs, the space and inserted position can be flexibly adjusted to satisfy different I/O requirements.

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