Nanoscale spatial phase modulation of GaAs growth in V-grooved trenches on Si (001) substrate*

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This letter reports the nanoscale spatial phase modulation of GaAs growth in V-grooved trenches fabricated on a Si (001) substrate by metal–organic vapor-phase epitaxy. Two hexagonal GaAs regions with high density of stacking faults parallel to Si {111} surfaces are observed. A strain-relieved and defect-free cubic phase GaAs was achieved above these highly defective regions. High-resolution transmission electron microscopy and fast Fourier transforms analysis were performed to characterize these regions of GaAs/Si interface. We also discussed the strain relaxation mechanism and phase structure modulation of GaAs selectively grown on this artificially manipulated surface.

Keywords: phase modulation, GaAs, grooves, Si

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1. Introduction

Epitaxial growth of III–V materials on Si has attracted significant attention for many years due to the potential application for monolithic integration of optoelectronic devices with Si integrated circuits and further improvement in the performance of next generation complementary metal–oxide semiconductor (CMOS).[1–6] However, the direct epitaxial growth of III–V materials on a Si substrate faces many challenges due to the lattice mismatch and the formation of antiphase domain boundaries (APBs).[7] The beneficial properties of nucleation on {111} planes were employed in order to improve material quality on (001) substrate.[8,9] Recently, selectively grown III–V materials in high aspect ratio trenches on Si (001) substrate, especially growth in V-shaped trenches is emerging as a promising growth technique for integrated high quality III–V materials on Si.[10–12] But the strain relaxation mechanism of GaAs in this V-shaped trench is still not clear.

Spatial phase separation of GaN selectively grown in nanoscale V-groove trenches on Si {111} surfaces have been reported.[13–15] In this letter, for GaAs growth on nanoscale Si {111} surfaces in V-groove trenches, through crystal structure measurement by high-resolution transmission electron microscopes (HRTEM) near the Si/GaAs interface, we find the same phenomenon of spatial phase modulation between hexagonal and cubic phase structure in V-grooved trenches. The investigation of the crystal structure modulation and the strain relaxation mechanism of GaAs on this artificially manipulated surface were the basic motivation of this work. Based on this method, we have achieved high quality InGaAs/InP multi-quantum wells (MQWs) and high mobility InGaAs channel material on Si substrate, and it will be reported on elsewhere.[16] This result shows great promise for the realization of high mobility devices or optoelectronic integrated circuits on Si substrates.

2. Experiment

The epitaxy was performed by metal–organic chemical vapor deposition (MOCVD) (AIXTRON 200) at a pressure of 50 mbar (1 bar = 10^5 Pa). Triethylgallium (TEGa), trimethylgallium (TMGa), and arsine (AsH3) were used as precursors. The Si (001) substrates were patterned with nanoscale V-shaped trenches along [110] direction. The width of the trench between two SiO_2 sidewalls was about 250 nm, while the depth of the V-groove is 180 nm–200 nm, and the thickness of the SiO_2 sidewall was about 500 nm. The fabrication process details for this V-shaped trench patterned Si substrates were reported elsewhere.[12] Deposition of GaAs on those patterned trenches by a two-steps growth method: a $\sim$ 18-nm thick GaAs low-temperature buffer was grown at 400 °C and a 400-nm-thick GaAs high-temperature epilayer was subsequently deposited at 630 °C. The morphologies of GaAs crystal were investigated by scanning electron microscopy (SEM). The crystal structure was characterized by FEI Tecnai F20 TEM operated at 200 kV. High-resolution TEM (HRTEM) and fast Fourier transforms (FFTs) were performed to analyze the crystal structure modulation and the strain relaxation mechanism near the GaAs/Si interface.

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3. Results and discussion

As shown in Fig. 1, selective growth of GaAs on this patterned substrate results in deposition of GaAs on Si {111} surfaces in V-grooved trenches, leading to two highly defective regions parallel with the {111} interfaces in the initial growth step. The GaAs material in this region shows hexagonal crystal structure with high density of stacking faults. Since GaAs has hexagonal phase on Si {111} with its *c* axis normal to it, the two top (0001) surfaces of GaAs materials formed a V groove at coalescence, with misaligned *c* axes. Above these highly defective regions, the GaAs layers are strain relieved and defect-free, and the crystal structure of GaAs material transforms to cubic the same as the Si substrate. We will discuss the mechanism of this hexagonal structure GaAs crystal growth and phase modulation between hexagonal and cubic structures.

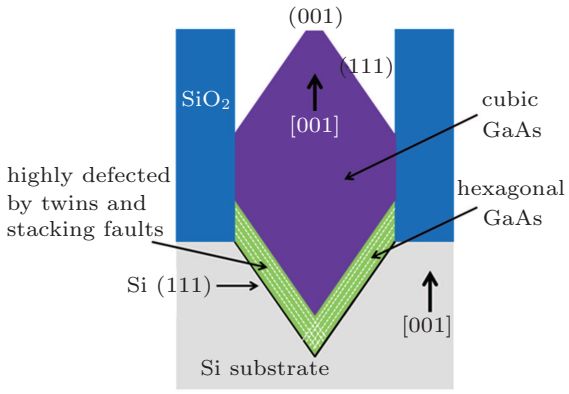


Fig. 1. (color online) Schematic illustration of the material phase map for GaAs selectively grown on {111} nanofaceted Si surfaces in V-groove trenches. Hexagonal highly defective regions and cubic defect-free region are indicated in this figure.

Figure 2(a) shows a cross-sectional TEM image of GaAs selectively grown in Si V-groove trenches. In Fig. 2(a), the V-groove trench is filled with a 400-nm-thick GaAs deposition. The SiO_2, GaAs, Si, and GaAs/Si {111} interface can be seen clearly. A ∼ 15-nm highly defective GaAs region can be observed near the Si/GaAs interface and it forms a boundary with the upper defect-free GaAs region on each side of the trenches which are parallel to the Si {111} surfaces, as illustrated in Fig. 1. The lattice mismatch was accommodated by this high defective region, and leaving a defect-free upper region. The high-quality GaAs material was achieved that showed a ridge crystal morphology consisting of two {111} surfaces. The detailed information about the material quality measurement was reported elsewhere.[12] Figure 2(b) shows a cross SEM image of GaAs material along the V-grooved trenches. It is well known that APBs characterized as pyramid-shaped pits or wedge-shaped surface defects which affected the surface morphology of selectively grown GaAs layers.[17,18] From the SEM image, we can observe that the GaAs layer grew in the V-grooved trenches, and it formed a perfect surface and was nearly flawless along the [110] direction. This result confirmed that no anti-phase boundary (APB) emerged in this material.

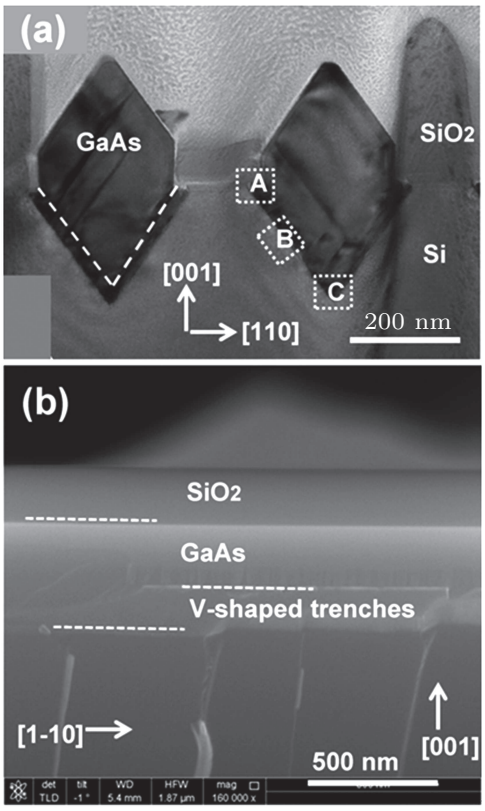


Fig. 2. (a) An XTEM image of GaAs selective growth in V-groove trenches of Si. (b) A cross-sectional SEM image along the [-110] direction. The GaAs crystal is uniform and flawless along the extension direction of the trenches and no anti-phase boundary (APB) was observed.

In order to investigate the strain relaxation mechanism of GaAs selective growth in V-grooved trenches on Si (001) substrate, HRTEM and FFTs measurements were performed to characterize the GaAs crystal structure near the GaAs/Si interface. Figures 3(a)–3(c) show the HRTEM images of GaAs crystal structure in selected areas, labeled A, B, and C in Fig. 2(a), respectively. Figure 3(d) is a higher multiplication HRTEM image of GaAs material in selected areas, labeled 3 in Fig. 3(c). For convenience, the interface of Si/GaAs was set to horizontal. In Figs. 3(a) and 3(b), These HRTEM images clearly reveal a 15-nm high defective region with a series of stacking faults parallel to the GaAs/Si interface. Above these regions, the GaAs crystal is strain relaxed and regains the same crystal structure as the Si substrate. Figure 3(c) shows the bottom of the V-grooved trench, two highly defective GaAs regions parallel with the Si {111} surfaces were observed and formed a V groove with a 70° angle at coalescence. Above this region, an almost defect-free GaAs region with cubic crystal structure can be observed. The HRTEM image shown in Fig. 3(d) indicates the stacking faults sequences in the highly defective region. Since an SF in the cubic phase corresponds to the presence of the hexagonal phase (and vice versa), a region

of SFs can be regarded as a phase fluctuation or an aperiodic variation of the crystal structure between hexagonal and cubic phases.[13,14] The boundary between the highly defective region and defect-free region can be clearly observed in this TEM image.

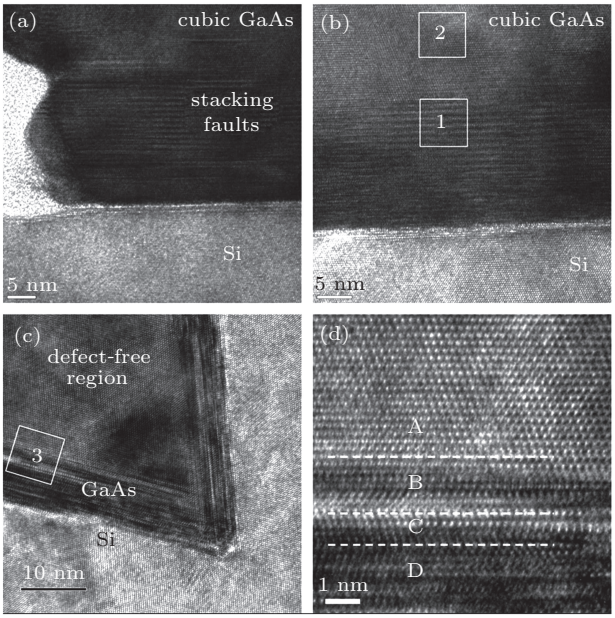


Fig. 3. (a)–(c) High-resolution TEM images of the region labeled A, B, and C in Fig. 2(a). Hexagonal highly defective regions and cubic defect-free region are clearly shown in these images. (d) A higher multiplication HRTEM image of GaAs material in selected areas, labeled 3 in Fig. 3(c). In the image, a series of dashed lines were labeled to show the phase fluctuation in this region.

Figures 4(a) and 4(b) are FFTs patterns corresponding to the white box areas labeled 1 and 2 in Fig. 3(b), which are highly defective regions and upper defect-free region, respectively. They reveal two kinds of diffraction patterns: hexagonal and cubic crystal structure. In Fig. 4(a), the arrows indicate the spots from hexagonal phase GaAs. According to this FFTs pattern, the lattice parameter of hexagonal GaAs along [0001], is approximately 9.79 Å, exactly three times that of the (111) spacing of cubic phase. The interplanar spacing of this GaAs crystal is approximately 3.26 Å for (0002) plane, 3.46 Å for $(01\bar{1}0)$ planes and 2.39 Å for $(01\bar{1}2)$ plane. Then, the average spacing of these GaAs planes, corresponds to a lattice parameter of a typical hexagonal structure, while the associated lattice constant a is 4 Å and c is 6.5 Å, which is close to the theoretical result of 3.912 Å and 6.441 Å.[19] In Fig. 4(b), this FFTs pattern shows that the upper part of the GaAs crystal is a single cubic phase and neither twins nor phase fluctuations influence can be observed. These diffraction spots indicated that the crystal axes of the cubic phase GaAs are parallel with the Si substrate. From this pattern, we calculated the interplanar spacing and lattice constant of GaAs crystal in this defect-free region, and we find that the GaAs layer is almost completely relaxed. It is because of the existence of the interfacial stacking fault network in the hexagonal region. These stacking faults can relieve misfit strain between GaAs and Si by a/6 $\langle 112 \rangle$ type partial dislocation.[20,21]

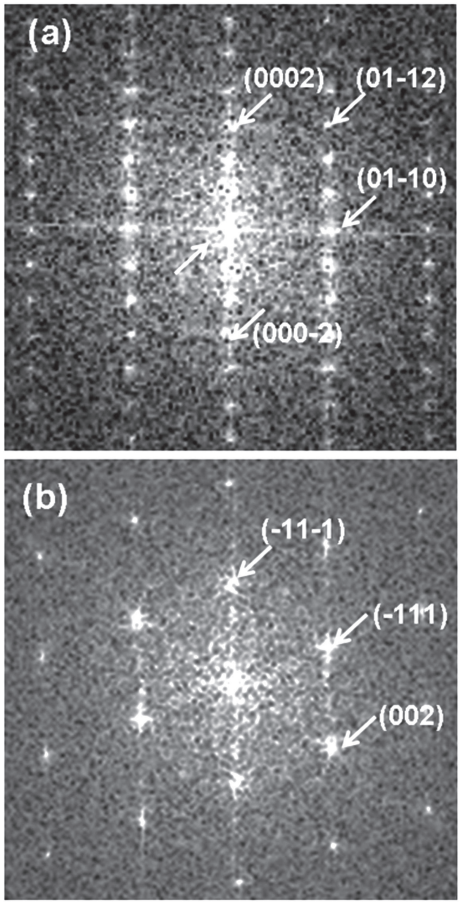


Fig. 4. Panels (a) and (b) are the FFT patterns corresponding to regions inside white box 1 and 2, respectively. They reveal two kinds of diffraction patterns: hexagonal and cubic crystal structures.

Now, we will discuss these results that we obtained from this experiment. Generally, the most stable bulk crystal structure at room temperature for GaAs is zinc-blend (ZB) crystal structure but the total-energy difference of GaAs is only 12.02 meV/atom between WZ and ZB structures. When GaAs growth is on a (111)-oriented ZB substrate, growth of either WZ or ZB is geometrically possible without producing miscoordinated atoms.[19] In this case, growth is preferable to the one which has the best elastic match with the substrate, often in defiance of the relative bulk stabilities.[19] Figure 5 depicts the structural difference between face-centered cubic (fcc) and hexagonal close-packed (hcp) crystal structures. Close-packed planes in fcc and hcp crystal structures are (111) and (0001) planes, respectively. When GaAs was grown on Si $\{111\}$ surface, the lattice mismatch between two materials can be calculated by adjacent atomic distance (λ). We suppose the lattice constant as $a_{\rm fcc}$ and $a_{\rm hcp}$ in these two crystal structures. In close-packed planes, the adjacent atomic spacings are $\sqrt{2}/2a_{\rm fcc}$ and $a_{\rm hcp}$, respectively. For GaAs crystal, the lattice constants of ZB and WZ structure are $a_{\rm GaAs(ZB)} = 5.654$ Å and $a_{\rm GaAs(WZ)} = 3.912$ Å, where the $a_{\rm Si} = 5.431$ Å for cubic

Si structure. The adjacent atomic spacings are $\lambda_{GaAs(ZB)} = 3.998$ Å, $\lambda_{GaAs(WZ)} = 3.912$ Å, and $\lambda_{Si} = 3.840$ Å, respectively. The lattice mismatch between GaAs and Si (111) planes are 4.1% and 1.9% for ZB and WZ crystal structure. So the WZ structure is preferable in the initial step when growing GaAs on Si {111} surface.

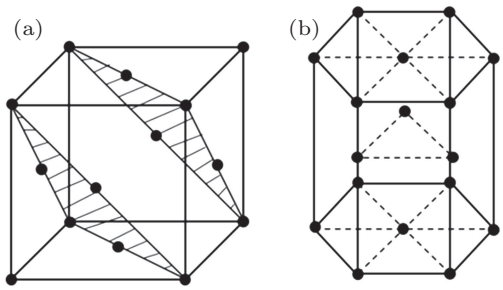


Fig. 5. (a) Face-centered cubic lattice and (111) close-packed plane. (b) Hexagonal close-packed crystal structure.

As discussed before, in V-grooved trenches, the GaAs growth is on Si {111} surfaces with its c axis normal to it. The two high defective regions near Si/GaAs interface, which with misaligned c axes tilted by 70° respect to each other, formed a V groove at coalescence. As the coalescence process goes on, the c axes misaligned hexagonal phase regions will dramatically increase the total lattice energy of GaAs material. The interaction of stacking faults in the coalescence region can also cause an increasing of total lattice energy. This will lead the crystal structure of GaAs to be unstable and eventually relieved by a transition to the cubic phase in the upper region of V-grooved trenches. This implies that the total crystal energy of GaAs on nanofaceted Si surfaces is reduced or minimized by changing phase structures. Experimentally, this phenomenon was demonstrated by Figs. 3(a)–3(c), that when GaAs growth is on Si {111} surfaces in V-grooved trenches, the crystal structure transformation to cubic phase is more favorable than keeping misaligned hexagonal phases. A relatively small energy difference between the WZ and ZB crystal structure of GaAs material is the physical origin of driving phase transition.

4. Conclusion

In conclusion, the nanoscale spatial phase modulation has been observed when there is selective growth of GaAs in V-grooved trenches on an Si (001) substrate. Two hexagonal GaAs regions with high density of stacking faults parallel to Si {111} surfaces are observed, with its c axis normal to it. A strain-relieved and defect-free GaAs cubic region is achieved above these high defective regions. The misfit strain between GaAs and Si was relieved by the hexagonal region with interfacial stacking faults network. We suppose that, when GaAs is selectively grown on this artificially manipulated surface, the phase structure modulation is driven by the total crystal energy minimizing process.

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