Effect of PECVD SiN_x/SiO_yN_x–Si interface property on surface passivation of silicon wafer*

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It is studied in this paper that the electrical characteristics of the interface between SiO_yN_x/SiN_x stack and silicon wafer affect silicon surface passivation. The effects of precursor flow ratio and deposition temperature of the SiO_yN_x layer on interface parameters, such as interface state density D_{it} and fixed charge Q_f, and the surface passivation quality of silicon are observed. Capacitance–voltage measurements reveal that inserting a thin SiO_yN_x layer between the SiN_x and the silicon wafer can suppress Q_f in the film and D_{it} at the interface. The positive Q_f and D_{it} and a high surface recombination velocity in stacks are observed to increase with the introduced oxygen and minimal hydrogen in the SiO_yN_x film increasing. Prepared by deposition at a low temperature and a low ratio of N_2O/SiH_4 flow rate, the SiO_yN_x/SiN_x stacks result in a low effective surface recombination velocity (S_{eff}) of 6 cm/s on a p-type 1 Ω·cm–5 Ω·cm FZ silicon wafer. The positive relationship between S_{eff} and D_{it} suggests that the saturation of the interface defect is the main passivation mechanism although the field-effect passivation provided by the fixed charges also make a contribution to it.

Keywords: solar cell, interface, passivation

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1. Introduction

Silicon oxynitride (SiO_yN_x) deposited through plasma-enhanced chemical vapor deposition (PECVD) has been widely used in microelectronic and optoelectronic devices.[1] The most significant feature of SiO_yN_x thin film is that its composition and properties can be easily controlled by varying precursor gas-flow ratio in deposition and post-annealing process. In recent years, SiO_yN_x, which is usually presented in the form of SiO_xN_y/SiN_x stacks, has shown great potential applications in various designs of the next-generation high-performance solar cells.[2] SiO_yN_x offers an adjustable refractive index between 1.45 and 2.1[3,4] and provides better transmission coefficient than single-layered silicon nitride (SiN_x). The coefficient makes it become a multilayer antireflection coating on the front side of solar cells. Silicon solar cells become thin to reduce wafer cost; thus, there exists a stronger reliance on the surface passivation of solar cells in the efficiency of silicon solar cells. SiO_yN_x has a large fixed positive charge density after being annealed;[5] thus, it is an effective passivation layer for various high-performance solar cells, particularly as a rear passivation layer in passivated emitter and rear cell (PERC) solar cells.[6,7] In our previous work,[8] inserting a PECVD-deposited SiO_yN_x layer between the SiN_x capping layer and the silicon wafer shows an increased resistance to potential-induced degradation (PID) compared with the single SiN_x layer.

Thus far, extensive work has been conducted to investigate the passivation properties of SiO_yN_x thin films. Most of these studies are based on how the deposition parameters and the annealing methods affect the stoichiometry of thin film and influence the minority carrier lifetime. Sommer *et al.*[9] determined oxygen concentration increases as N_2O gas dilution ratio rising, while the nitrogen remains nearly unchanged. Their observations implied that oxygen replaces hydrogen in films. This finding agreed with the report of Dupuis *et al.*,[10] indicating that low oxygen content sample with high hydrogen content exhibits a better surface passivation before being annealed than a sample with high oxygen content. The annealing process affects the hydrogen content in the film[11] and changes the sign of charge in the film, with a negative charge in the film before being annealed and a positive charge after being annealed.[12] However, clarifying how the electrical properties of the interface between the dielectric film and the silicon wafer affect the silicon surface passivation needs in-depth investigation.

The present study aims to examine how N_2O/SiH_4 gas flow ratio (R) and the deposition temperature of SiO_yN_x thin layer affect the SiO_yN_x/SiN_x–stack/silicon interface and the surface passivation of silicon wafer. The interface properties are analyzed via capacitance–conductance–voltage (C–G–V)

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measurement and noncontact corona *C–V* metrology. The passivation influence of the layer is quantified through effective minority carrier lifetime measurement using quasi-static state photo-conductance (QSSPC) method.

2. Experiment

2.1. Sample preparation

High-quality double-side-polished 1 Ω·cm–5 Ω·cm FZ p-type silicon wafers were used as substrates. The wafers experienced a standard RCA cleaning and a 1-min oxide removal process in a 1-wt% HF solution prior to PECVD processing.

The SiO_yN_x films were deposited on silicon wafers in a PECVD system (PlasmaLab System133) from Oxford Instruments. Silane (SiH_4) and nitrous oxide (N_2O) were used as precursor gases. The microwave power and the pressure were maintained at a constant value of 47 mW/cm^2 and 500 mTorr (1 Torr = 1.33322×10^2 Pa), respectively. The deposition temperature varied from 35 °C to 400 °C. The R of SiH_4 and N_2O flow ratio, R, was controlled from 0.44 to 77.

After the deposition of SiO_yN_x film, the capping layer, a 70-nm SiN_x film, was deposited in the same PECVD chamber. Ammonia (NH_3) and SiH_4 were used as precursor gases. The microwave power, the pressure, and the deposition temperature were kept at 58 mW/cm^2, 800 mTorr, and 400 °C, respectively. The refractive index of the SiN_x layer, which was measured via spectroscopic ellipsometry (JobinYvon UVISEL), was 2.04 at wavelength $\lambda = 630$ nm.

After the deposition of the SiO_yN_x/SiN_x stack structure, the rapid thermal annealing (RTA) was performed on each of the samples at approximately 800 °C for 5 s. This process imitates the co-firing screen printing of Ag and Al at the end of the production of the silicon solar cells.

2.2. *C–G–V* measurement

Metal–insulator–semiconductor (MIS) structures were prepared to perform the *C–G–V* characterization. For all kinds of samples, the aluminum contact of 100 nm was thermally evaporated to produce Al/Si/SiO_yN_x/SiN_x/Al device and Al/Si/SiN_x/Al as references. The diameter of the circular gate electrode was 3 mm. Multifrequency (10 kHz to 2 MHz) *C–V* and *G–V* measurements were performed with a Keithley 4200 SCS using the parallel model.[13] All measurements were compensated for by a series resistance. The interface state density (D_{it}) in half the band gap could be extracted by combining the *C–V* and *G–V* tests. A noncontact *C–V* metrology (PV2000, Semilab) was used to investigate the energy distribution of the D_{it} in the band gap for post-RTA sample.[14]

2.3. Effective minority carrier lifetime

The effective minority carrier lifetime (τ_{eff}) of p-type silicon wafer that was double-side coated with the SiO_yN_x/SiN_x stacks was observed. A silicon wafer that was double-side coated with the single 100-nm-thick SiN_x film was used as reference. QSSPC measurements (Sinton Instruments lifetime tester) were performed with the optical constant as "1- reflection index" at an injection level of $\Delta n = 7\times10^{14}$ cm^{-3}. The effective surface recombination velocity (S_{eff}) can be calculated from[15]

$$\frac{1}{\tau_{eff}} \approx \frac{1}{\tau_b} + \frac{2S_{eff}}{W}, \tag{1}$$

where W is the thickness of the wafer. A minority carrier lifetime of 3 ms for p-type wafer with a resistance of 1.37 Ω·cm was obtained through high-quality intrinsic a-Si passivation. For wafers that have similar resistances, this is the lower limit to the bulk lifetime, which approximately could be taken as the bulk minority carrier lifetime $\tau_b = 3$ ms.

3. Result and discussion

3.1. *C–V* characteristic of SiO_xN_y/SiN_x stacks

The multifrequency *C–G–V* characteristics of one of the post-RTA SiO_xN_y/SiN_x stack samples are shown in Fig. 1. The regions of accumulation, depletion, and inversion are clearly shown, thereby verifying a typical metal–oxide–semiconductor (MOS) behavior. No dependence on the frequency of *C–V* curve is observed in the accumulation because the the device structure is automatically compensated for by a series resistance during the measurement. However, the *C–V* curve is stretched out at the low frequency in depletion possibly because of the capacitive response of the interface states of dielectrics/Si to the measurement frequency.[16] The distinctive peaks of the G/ω–V curves are shown in this region, thereby indicating the presence of interface-trapped charges.[17] These distinctive peaks are correspondingly helpful to analyze the electrical responses of interface defect states to different frequencies. Moreover, at 40 kHz the G/ω–V curve reaches a highest G/ω–V peak, which is used for *C–G–V* measurement to obtain D_{it} information.

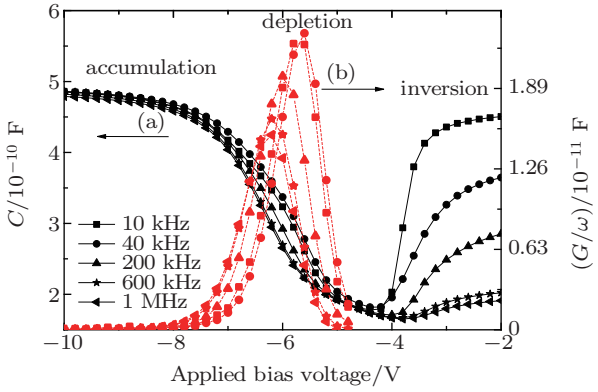


Fig. 1. (color online) Multifrequency (10 kHz to 1 MHz) *C–G–V* characteristics of an MIS capacitor utilizing post-RTA SiO_yN_x/SiN_x stacks. (a) The *C–V* curves were measured in inversion–accumulation direction. (b) The peaks of G/ω–V curves lie in the range of depletion.

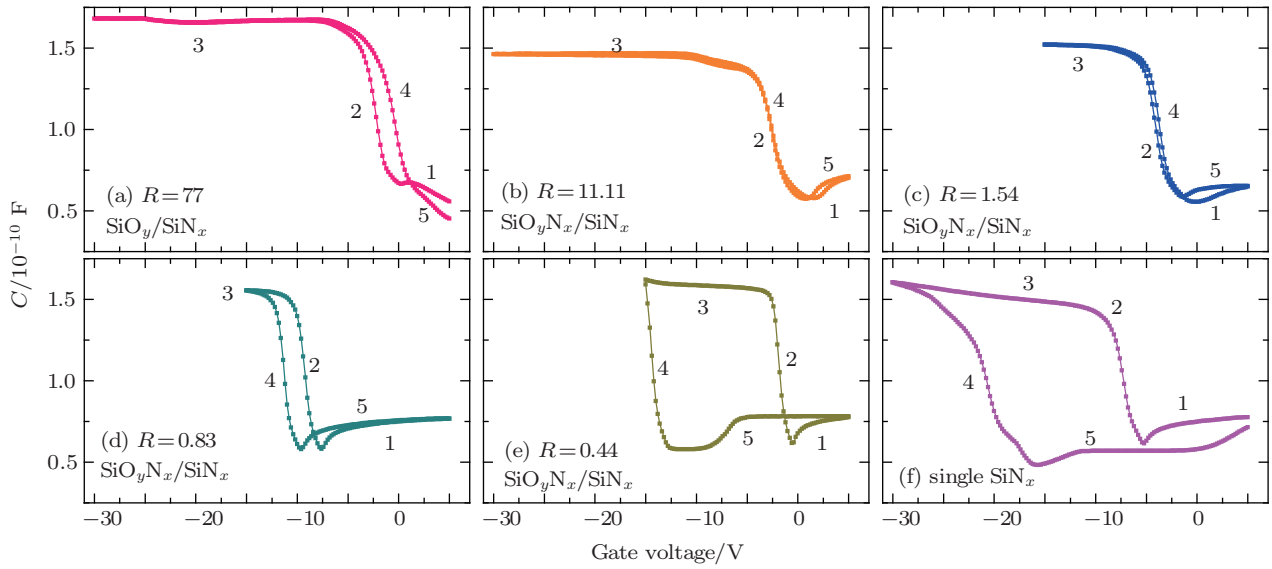


Fig. 2. (color online) Compositions of the SiO_yN_x layer of the SiO_yN_x (30 nm) / SiN_x (70 nm) stacks influence the hysteresis in C–V curves. The complete measurement circle is inversion–accumulation–inversion. In the SiO_y/SiN_x stacks, (a) $R = 77$. In the SiO_yN_x/SiN_xstacks, (b) $R = 11.11$, (c) $R = 1.54$, (d) $R = 0.83$, and (e) $R = 0.54$. The reference is (f) the single SiN_x (100 nm) layer.

The varying N_2O/SiH_4 gas flow ratio (R) changes the Si, O, and N concentrations in the SiO_yN_x layer. The hysteresis formation of the SiO_yN_x (30 nm)/SiN_x (70 nm) stacks is measured using inversion–accumulation–inversion complete circles as shown in Fig. 2. From Figs. 2(a) to 2(e), the R varies from 77 to 0.44; $R = 77$ means that the film is basically the SiO_y layer measured via the Fourier transform infrared (FTIR) spectroscopy (not shown in this paper). The result of the single SiN_x (100 nm) layer (f) is also shown for reference.

The largest hysteresis is observed in the sample with only a single SiN_x layer at $\Delta V_{FB} = 13$ V. For PECVD-prepared SiN_x film, the hysteresis of the Si-rich film with numerous Si dangling bonds is larger than that of the N-rich film.[18] The SiO_yN_x films deposited with low R values of 0.44 and 0.83 each show a counter-clockwise hysteresis formation, which can be interpreted by the following hole-trapping mechanism:[19] High-density hole trapping sites possibly exist at the interface. These trapping sites can be filled with majority carrier holes at the accumulation state when voltage sweeping is applied from inversion to accumulation. Therefore, the excess positive charge trapped at the interface can make the flat voltage (V_{FB}) shift to a negative applied bias voltage when voltage sweeping is applied from accumulation back to inversion. The V_{FB} is affected by the applied bias sweep range and by its history, and the injected charges generate hysteresis during the C–V measurements, thereby leading to the shift of the V_{FB}. For instance, the hysteresis effect of the single SiN_x layer is reduced by inserting a SiO_yN_x layer at $R = 0.83$, thereby making the ΔV_{FB} decrease to 2.5 V. This observation indicates the reduction of the trap state density existing in the stacks.

The hysteresis effect changes the feature from counter-clockwise to clockwise direction when R is increased up to a value of 1.54 ($\Delta V_{FB} = 1$ V). The hysteresis effect leads to a counter-clockwise feature in SiN_x[20] and a clockwise feature in SiO_2.[21] The former indicates the hole trapping at the negative bias, whereas the latter shows the electron trapping. This observation implies that the increase of R results in the change of the charge-trapping center in stacks from the nitrogen-related (similar to SiN_x films) to the oxygen-related silicon dangling bonds (similar SiO_2 films).

The R also affects the energy distribution of the D_{it} in the band gap. The variations of measured D_{it} with energy level in the band gap of post-RTA SiO_yN_x (10 nm)/SiN_x (70 nm) stacks for different N_2O:SiH_4 ratios are shown in Fig. 3. The D_{it} distribution curves each have a nearly symmetrical U shape, and the minimum value is reached near the mid-gap. For stacks, the minimum value of D_{it} in the mid-gap rises as the R increases from 6.5×10^{11} $eV^{-1}{\cdot}cm^{-2}$ at $R = 0.44$ to 7.9×10^{11} $eV^{-1}{\cdot}cm^{-2}$ at $R = 77$. The D_{it} of the single SiN_x layer in the mid-gap is 2.4×10^{12} $eV^{-1}{\cdot}cm^{-2}$, which is one order of magnitude higher than that of SiN_x layer in the stacks. The N–H bonds in the SiO_yN_x films are considerably less than those in the SiN_x films. However, the increase of R (i.e., more oxygen content is introduced into the SiO_yN_x film) results in the increase of the N–H bonds with the decrease of Si–H bonds.[20] Previous results show that the N–H bonds in films are inferior to Si–H bonds for silicon surface passivation.[22] Consequently, the more oxygen content incorporated in the SiO_yN_x layer significantly affects the passivation quality of the interface. If a small oxygen content is introduced into the dielectric layer, low N–H bond density results in decreases of D_{it} and Q_f compared with the case of less oxygen content incorporated into the single SiN_x layer.[22] However, an increased oxygen content is incorporated into the dielectric layer; thus,

the decrease of the Si–H bond density and the increase of the N-H bond density result in forming numerous oxygen-related silicon dangling bonds, such as N≡Si·, N_2O≡Si·, NO_2 ≡Si·, and O≡Si··.[23]

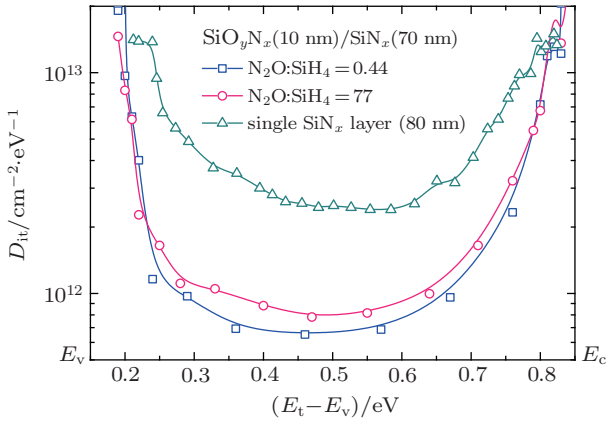


Fig. 3. (color online) Energy distribution of D_{it} in the band gap for the post-RTA SiO_yN_x (10 nm)/SiN_x (70 nm) stacks with the single SiN_x (100 nm) layer as reference. The SiO_yN_x layers are deposited at different R values with the deposition temperature of 130 °C.

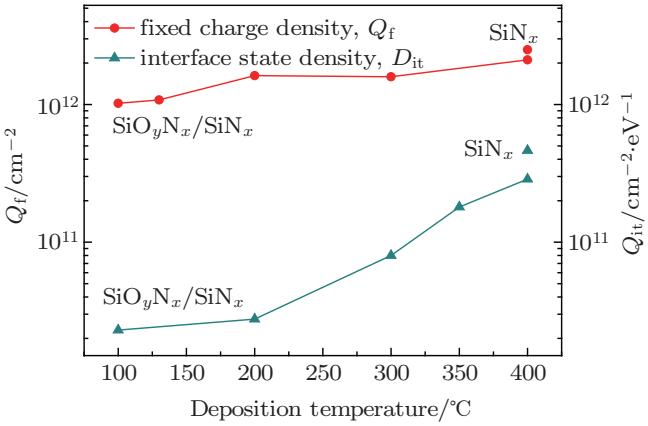


Fig. 4. (color online) Summary of the electrical parameters of the SiO_yN_x (30 nm)/SiN_x (70 nm) stacks, including Q_f and D_{it}, with the single SiN_x (100 nm) film as reference. The SiO_yN_x layers are deposited at different deposition temperatures of 100 °C–400 °C, with $R = 1.54$.

The effect of the deposition temperature on the electrical properties of the interface between the SiO_yN_x/SiN_x stacks and the Si substrate is studied. The D_{it} and Q_f of the stacks and the single SiN_x layer-coated silicon wafers are summarized in Fig. 4. The D_{it} of the SiO_yN_x/SiN_x stacks increases with the increase of deposition temperature: it increases from 2.3×10^{10} $eV^{-1}\cdot cm^{-2}$ at 100 °C to 2.9×10^{11} $eV^{-1}\cdot cm^{-2}$ at 400 °C. The D_{it} of the single SiN_x layer is 4.7×10^{11} $eV^{-1}\cdot cm^{-2}$ in a typical range from 1×10^{11} $eV^{-1}\cdot cm^{-2}$ to 5×10^{12} $eV^{-1}\cdot cm^{-2}$, which was reported by Aberle.[24] The Q_f of the SiO_yN_x/SiN_x stacks rises with deposition temperature increasing from 1×10^{12} cm^{-2} at 100 °C to 2.1×10^{12} cm^{-2} at 400 °C. The Q_f of the single SiN_x layer is 2.5×10^{12} cm^{-2}, which is larger than that in the SiO_yN_x/SiN_x stacks. In their stable form N_3 ≡Si^+ (K^+ centers), the K centers contribute primarily to the fixed positive charges in the SiN_x films.[25] These fixed positive charges are situated in a 20-nm interface layer between the dielectric and the Si substrate.[23] The stacks present lower Q_f and D_{it} than the reference sample (100-nm SiN_x-coated silicon). This observation illustrates that the reduction of the structure defect at the SiO_yN_x/Si interface or in film results from the effect of O atom incorporation during deposition and annealing.

3.2. Surface passivation properties on silicon wafers

The S_{eff} of the SiO_yN_x (30 nm)/SiN_x (70 nm) stacks is obtained through the QSSPC measurement at an injection level of $\Delta n = 7 \times 10^{14}$ cm^{-3}. The effect of the N_2O/SiH_4 gas flow ratio (R) is presented in Fig. 5 using the single SiN_x (80 nm) layer as reference. The S_{eff} of the single SiN_x layer is 71 cm/s. For SiO_yN_x/SiN_x stacks, the S_{eff} increases from 6 cm/s to 700 cm/s as R increases from 0.44 to 77. In addition, the S_{eff} is approximately 1000 cm/s on the entire surface of an "O-rich" sample, for instance, when R is above 10. The highest $S_{eff} = 2360$ cm/s is obtained at $R = 15.56$. In this condition, the film is basically the SiO_x layer measured by FTIR spectroscopy (not shown in this paper). In a range of $R = 0.44$–1.54 (refractive index: 2.1–1.6), the S_{eff} increases from 6 cm/s at $R = 0.44$ to 35 cm/s at $R = 1.54$. All values are lower than those in the cases of single SiN_x coating. Therefore, good passivation properties are clearly obtained when the SiO_yN_x layer, not the SiO_x, is introduced as the passivation layer.

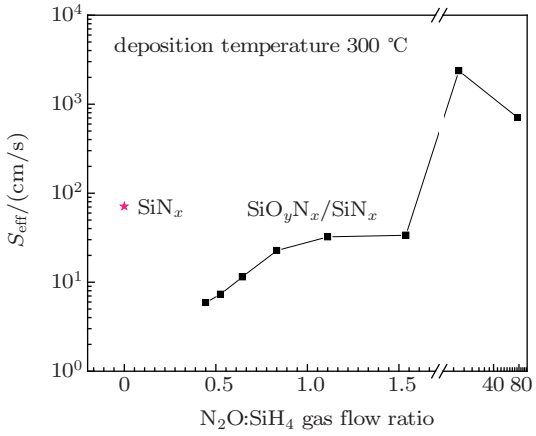


Fig. 5. (color online) S_{eff} of the post-RTA SiO_yN_x (30 nm)/SiN_x (70 nm) stacks at an injection level of $\Delta n = 7 \times 10^{14}$ cm^{-3} through QSSPC with the single SiN_x (80 nm) layer as reference. The SiO_yN_x layer is deposited at different R values with the deposition temperature of 300 °C.

The effect of the deposition temperature is presented in Fig. 6. The S_{eff} increases from 6 cm/s to 70 cm/s as deposition temperature increases from 100 °C to 400 °C for sample deposited with $R = 1.54$. Good passivation properties are clearly obtained when the SiO_yN_x deposition is conducted at a low temperature. Numerous Si–O bonds are introduced into the films as the deposition temperature increases,[26] thereby creating many oxygen-related defects at the interface. The total H content decreases when the deposition temperature increases, thereby resulting in many non-passivated defects in the film and at the interface, and leading to the increases of Q_f and

D_{it} (as shown in Fig. 4). Figure 4 shows that the D_{it} significantly increases as deposition temperature increases; however, Q_f exhibits a slight change: it increases from 1×10^{12} cm^{-2} when the deposition temperature is 100 °C to 2.1×10^{12} cm^{-2} when the deposition temperature is 400 °C. The combination of the relationship among S_{eff}, D_{it}, and Q_f with the deposition temperature shows that the surface passivation is influenced mainly by the interface state (chemical passivation). High Q_f provides a certain degree of field-effect passivation; however, high D_{it} induces the increase of S_{eff} with deposition temperature rising because of poor chemical passivation. According to the preceding result, the optimized deposition parameter for the SiO_yN_x film is obtained at a low deposition temperature and a low ratio of N_2O/SiH_4 flow rate.

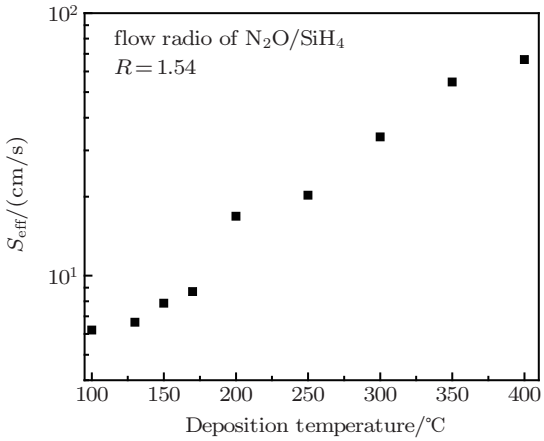


Fig. 6. S_{eff} of the post-RTA SiO_yN_x (30 nm)/SiN_x (70 nm) stacks at a corona charge injection level of $\Delta n = 7 \times 10^{14}$ cm^{-3} through QSSPC. The SiO_yN_x layer is deposited at different deposition temperatures, with $R = 1.54$.

4. Conclusions

Low interface state density (D_{it}) and fixed charge density (Q_f) are obtained after a thin SiO_yN_x layer has been inserted between the capping SiN_x layer and the silicon wafer. The small hysteresis for stack in *C*–*V* curve indicates that there exists a lower charge-trapping state density in the stack than that in the single SiN_x film. Other oxygen-related defects are induced in the films by increasing the O content and minimizing H content in the SiO_yN_x films as R increases. The minimum value of D_{it} in the energy distribution of the sample with a stack rises with the increase of R by one order of magnitude lower than the one with a single SiN_x layer. The S_{eff} varies from 6 cm/s to 35 cm/s as R increases from 0.44 to 1.54. This S_{eff} is lower than the S_{eff} (71 cm/s) of the single SiN_x layer. The minimum value of D_{it} of the stack in the band gap rises with the deposition temperature increasing in a range from 100 °C to 400 °C. Good passivation properties, such as $S_{eff} = 6$ cm/s, are obtained at low deposition temperature. The correlation between D_{it} and S_{eff} indicates that although the field-effect passivation may contribute to the passivation of the silicon surface, the chemical passivation from the stack dominates the entire passivation process.

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