A technique for simultaneously improving the product of cutoff frequency–breakdown voltage and thermal stability of SOI SiGe HBT*

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The product of the cutoff frequency and breakdown voltage ($f_T \times BV_{CEO}$) is an important figure of merit (FOM) to characterize overall performance of heterojunction bipolar transistor (HBT). In this paper, an approach to introducing a thin N^+-buried layer into N collector region in silicon-on-insulator (SOI) SiGe HBT to simultaneously improve the FOM of $f_T \times BV_{CEO}$ and thermal stability is presented by using two-dimensional (2D) numerical simulation through SILVACO device simulator. Firstly, in order to show some disadvantages of the introduction of SOI structure, the effects of SOI insulation layer thickness (T_{BOX}) on f_T, BV_{CEO}, and the FOM of $f_T \times BV_{CEO}$ are presented. The introduction of SOI structure remarkably reduces the electron concentration in collector region near SOI substrate insulation layer, obviously reduces f_T, slightly increases BV_{CEO} to some extent, but ultimately degrades the FOM of $f_T \times BV_{CEO}$. Although the f_T, BV_{CEO}, and the FOM of $f_T \times BV_{CEO}$ can be improved by increasing SOI insulator SiO_2 layer thickness T_{BOX} in SOI structure, the device temperature and collector current are increased due to lower thermal conductivity of SiO_2 layer, as a result, the self-heating effect of the device is enhanced, and the thermal stability of the device is degraded. Secondly, in order to alleviate the foregoing problem of low electron concentration in collector region near SOI insulation layer and the thermal stability resulting from thick T_{BOX}, a thin N^+-buried layer is introduced into collector region to not only improve the FOM of $f_T \times BV_{CEO}$, but also weaken the self-heating effect of the device, thus improving the thermal stability of the device. Furthermore, the effect of the location of the thin N^+-buried layer in collector region is investigated in detail. The result show that the FOM of $f_T \times BV_{CEO}$ is improved and the device temperature decreases as the N^+-buried layer shifts toward SOI substrate insulation layer. The approach to introducing a thin N^+-buried layer into collector region provides an effective method to improve SOI SiGe HBT overall performance.

Keywords: SOI SiGe HBT, collector optimization, $f_T \times BV_{CEO}$, self-heating effect

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1. Introduction

In recent years, the processing integration of high-performance SiGe heterojunction bipolar transistor (HBT) with low-power CMOS on thin-film silicon on insulator (SOI), which forms SiGe BiCMOS technology,[1–3] has been considered as one of the most efficient and flexible techniques to meet the requirements for the microwave and radio frequency domain.[4–7] The substrate insulation layer SiO_2 in SOI structure eliminates the collector-substrate PN junction, which causes the collector potential to be unable to go deep into the substrate, resulting in the fact that the charges accumulted in collector region near SOI insulation layer are much smaller than those in bulk HBTs. As a result, it suppress the charge collection in collector region near SOI insulation layer,[8] remarkably reducing the electron concentration in collector region near SOI substrate insulation layer, obviously increasing collector resistance, eventually substantially reducing the unity gain cutoff frequency (f_T) in SOI SiGe HBT.[9] Meanwhile, the decrease of electron concentration in collector region near SOI substrate insulation layer is beneficial to the increase of breakdown voltage (BV_{CEO}) to some extent, but it causes ultimately the product of cutoff frequency-breakdown voltage ($f_T \times BV_{CEO}$) to decrease,[10] which is an important figure of merit (FOM) to characterize overall performance of HBT. On the other hand, the lower thermal conductivity of the insulation layer SiO_2 in SOI structure can cause the device temperature to rise (self-heating effect), which results in the increase of the collector current rapidly, and even generates thermal runaway, and therefore degrades the thermal stability of the device.[11,12] In this paper, a technique to improve the FOM of $f_T \times BV_{CEO}$ is presented. A thin N^+-buried layer is introduced into N collector region of SOI SiGe HBT for not only improving the FOM of $f_T \times BV_{CEO}$, but also weakening the self-heating effect of the device.

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2. SOI SiGe HBT structure

Compared with SiGe HBT on bulk silicon, SOI SiGe HBT owns the same emitter and base structure, but owns a different collector structure which is formed by introducing SOI substrate insulation layer into collector region.[13,14] Figure 1 shows the two-dimensional (2D) cross-section of traditional SOI SiGe HBT used in SILVACO/ATHENA, and the schematic diagram of structure parameters for SOI SiGe HBT is shown in Fig. 2. The SOI structure is comprised of 0.8-μm N^- silicon layer with an average doping concentration of 2×10^{16} cm^{-3} and a 50-nm buried oxide layer (BOX) on the top of 0.55-μm P substrate with an average doping concentration of 1×10^{15} cm^{-3}. A 50-nm P SiGe with an average doping concentration of 1×10^{18} cm^{-3} and Ge fraction of 0.16 is deposited on SOI structure. A 0.2-μm P^+ extrinsic base with a doping concentration of 3×10^{18} cm^{-3} is grown on the top of P SiGe base. After the growth of P^+ extrinsic base layer, a 0.2-μm N^+ POLY emitter with a doping concentration of 1×10^{20} cm^{-3} is deposited for reducing the emitter resistance, which simultaneously forms a 0.2-μm N Si emitter on the top of P SiGe base.

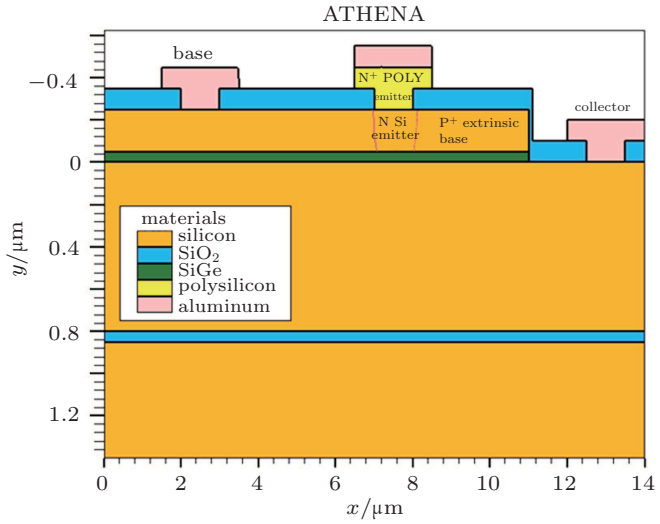


Fig. 1. (color online) 2D cross-section of traditional SOI SiGe HBT used in SILVACO/ATHENA.

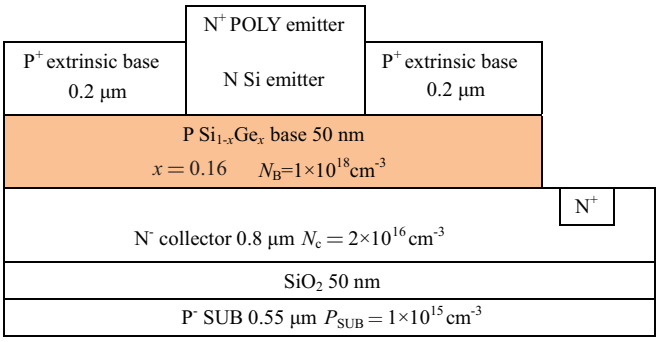


Fig. 2. (color online) Schematic diagram of structure parameters for traditional SOI SiGe HBT.

Figure 3 shows a novel SOI SiGe HBT with a thin N^+-buried layer in N collector region, all the structure parameters are the same as those of traditional SOI SiGe HBT except thin N^+-buried layer with a thickness of 50 nm. z is the distance from the N^+-buried layer to SOI substrate insulation layer.

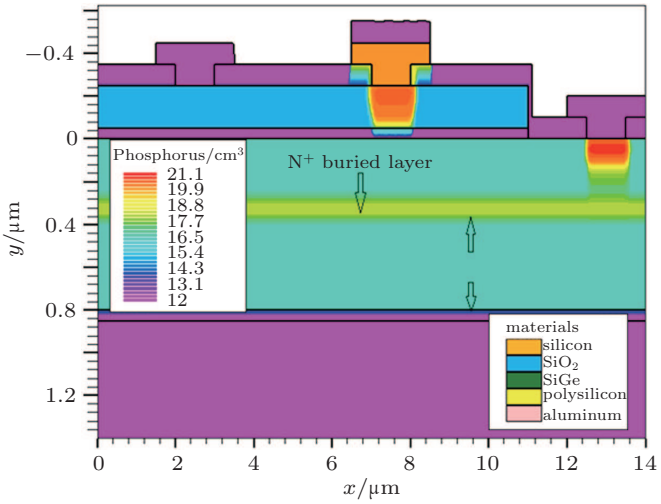


Fig. 3. (color online) Novel SOI SiGe HBT with thin N^+-buried layer in N collector region (T_{BOX} = 50 nm).

3. Results of traditional SOI SiGe HBT

Figure 4 shows the comparison of plot f_T–J_C between traditional SOI SiGe HBT and standard SiGe HBT on bulk silicon. The peak unity gain cutoff frequency f_T in traditional SOI SiGe HBT is 10.9 GHz, which is reduced by 44.1% compared with that of the standard SiGe HBT on bulk silicon (19.5 GHz).

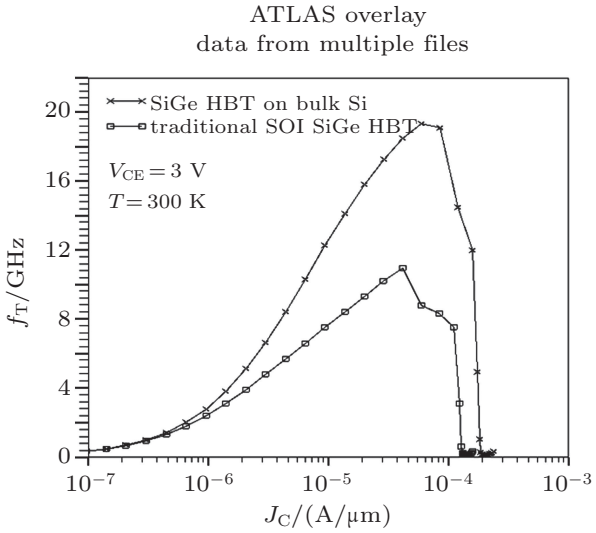


Fig. 4. Comparison of plot f_T–J_C between traditional SOI SiGe HBT and standard SiGe HBT on bulk silicon.

The result can be explained as follows.

The unity gain cutoff frequency (f_T) in SiGe HBT is given in generally as[15]

$$f_T = \frac{1}{2\pi\tau_{ec,SiGe}}, \tag{1}$$

where $\tau_{ec,SiGe}$ is the total emitter-to-collector delay time in SiGe HBT, $\tau_{ec,SiGe}$ is given by[16]

$$\tau_{ec,SiGe} = \frac{kT}{qI_C}(C_{eb}+C_{cb}) + \tau_{e,SiGe} + \tau_{b,SiGe} + \tau_{bc,SiGe}, \quad (2)$$

where $\tau_{e,SiGe}$, $\tau_{b,SiGe}$, and $\tau_{bc,SiGe}$ are the emitter, base, and collector transit times in SiGe HBT, $\tau_{bc,SiGe}$ and $\tau_{e,SiGe}$ are expressed as[17,18]

$$\tau_{bc,SiGe} = \left[\frac{kT}{qI_C} + (r_e + r_c)\right] C_{cb}, \quad (3)$$

$$\tau_{e,SiGe} = \left(\frac{kT}{qI_c}\right) C_{eb}. \quad (4)$$

As C_{BOX} formed by the introducing of SOI substrate insulation layer is in series with C_{cb}, the collector transit time in SOI SiGe HBT ($\tau_{bc,SOISiGe}$) is written as

$$\tau_{bc,SOISiGe} = \left[\frac{kT}{qI_c} + (r_e + r_c)\right] \frac{C_{cb}C_{BOX}}{C_{cb}+C_{BOX}}. \quad (5)$$

Substituting Eqs. (4) and (5) into Eq. (2), the total emitter-to-collector delay time in SOI SiGe HBT ($\tau_{ec,SOISiGe}$) is obtained as

$$\begin{aligned}\tau_{ec,SOISiGe} &= \frac{kT}{qI_c}(C_{eb}+C_{cb}) + \tau_{b,SiGe} \\ &+ \left[\frac{kT}{qI_c} + (r_e + r_c)\right] \frac{C_{cb}C_{BOX}}{C_{cb}+C_{BOX}} + \left(\frac{kT}{qI_c}\right) C_{eb}, \quad (6)\end{aligned}$$

where C_{BOX} is the SOI insulation layer capacitance and C_{cb} is the base–collector junction capacitance, and other symbols have their usual meanings.

The introduction of SOI insulation layer SiO_2 reduces base–collector equivalent capacitance because C_{BOX} and C_{cb} are connected in series, which is beneficial to improving f_T in traditional SOI SiGe HBT. But it also remarkably reduces the electron concentration in collector region near SOI insulation layer as shown in Fig. 5, thus leading to the obvious increase in the collector resistance, consequently the increase of $\tau_{bc,SiGe}$, which is dominant, and eventually the decrease of f_T.

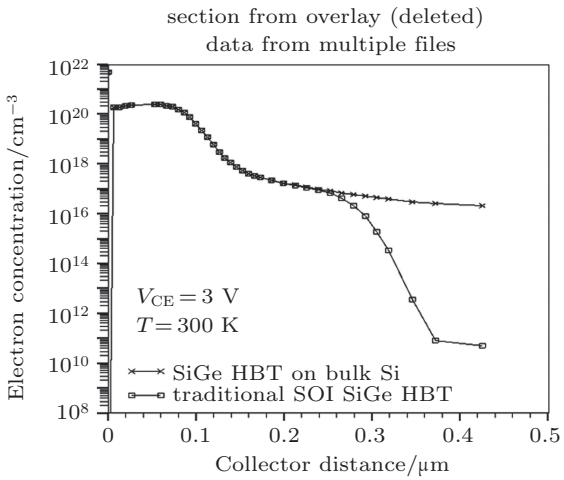


Fig. 5. Electron concentration profiles in collector region for traditional SOI SiGe HBT and standard SiGe HBT on bulk silicon, respectively.

In addition, the decrease of electron concentration in collector region near SOI substrate insulation layer caused by the introduction of SOI insulation layer SiO_2 results in the increase of BV_{CEO}, as shown in Fig. 6. BV_{CEO} improves from 8.9 V to 11.3 V, an increase of 27%. However, the product of $f_T \times BV_{CEO}$ decreases from 173.55 GHz·V to 123.17 GHz·V, a decrease of 29%. Table 1 compares traditional SOI SiGe HBT with standard SiGe HBT on bulk silicon.

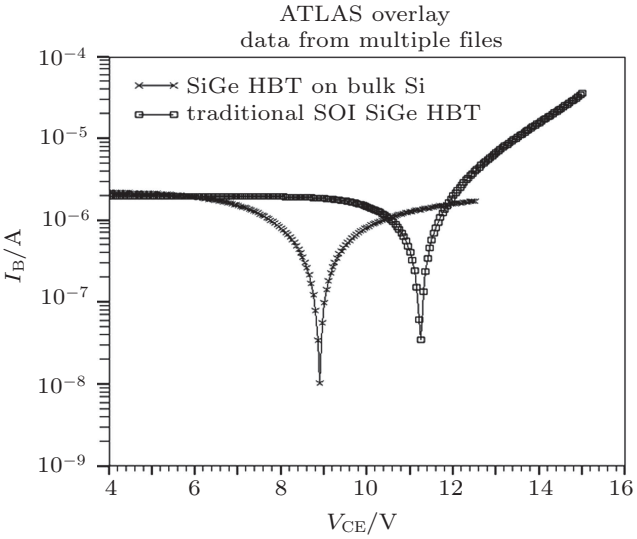


Fig. 6. Absolute values of the base current versus V_{CE} for traditional SOI SiGe HBT and standard SiGe HBT on bulk silicon, respectively.

Table 1. Parameters for traditional SOI SiGe HBT and standard SiGe HBT on bulk silicon.

Type of SiGe HBT	f_T/GHz	BV_{CEO}/V	$f_T \times BV_{CEO}$/GHz·V
Traditional SOI SiGe HBT	10.9	11.3	123.17
Standard SiGe HBT on bulk silicon	19.5	8.9	173.55

For the traditional SOI SiGe HBT, the f_T can be improved by reducing C_{BOX} in order to reduce $\tau_{ec,SOISiGe}$ by adjusting the SOI insulation layer thickness (T_{BOX}). Figure 7 shows the comparison of the plot f_T–J_C for traditional SOI SiGe HBT among the cases of different T_{BOX} values. With the increase of T_{BOX} from 50 nm to 150 nm, the peak f_T increases from 10.9 GHz to 12.9 GHz, an increase of 18.3%.

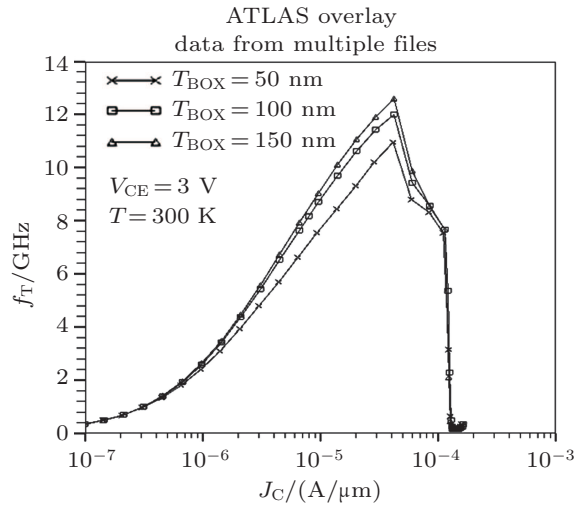


Fig. 7. Comparison of plot f_T–J_C for traditional SOI SiGe HBT among the cases of different T_{BOX} values.

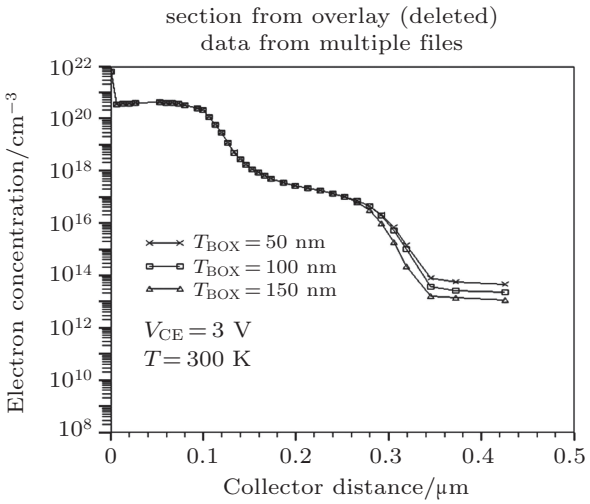


Fig. 8. Electron concentration profiles in collector region for traditional SOI SiGe HBT with different T_{BOX} values.

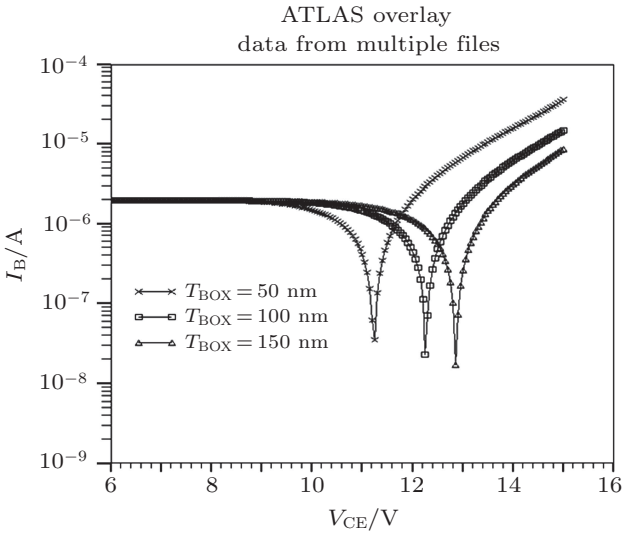


Fig. 9. Plots of absolute values of the base current versus V_{CE} for traditional SOI SiGe HBT with different T_{BOX} values.

However, the increase of T_{BOX} also reduce the electron concentration in collector region near SOI insulation layer as shown in Fig. 8, which leads to the increase of the collector resistance, hence tend to the increase of $\tau_{ec,SOISiGe}$. However, the decrease of $\tau_{ec,SOISiGe}$ by reducing C_{BOX} due to the increase of T_{BOX} is dominant. As a result, the peak f_T increases with the increase of T_{BOX}.

The decrease of electron concentration in collector region near SOI insulation layer by increasing the T_{BOX} also increases BV_{CEO} as shown in Fig. 9. With the increase of T_{BOX} from 50 nm to 150 nm, BV_{CEO} improves from 11.3 V to 12.9 V, an increase of 14.2%, and the product of $f_T \times BV_{CEO}$ increases from 123.17 GHz·V to 166.41 GHz·V, an increase of 35.1%. Table 2 shows the comparison among SOI SiGe HBTs with different T_{BOX} values.

Table 2. Parameters for traditional SOI SiGe HBTs with different T_{BOX} values.

T_{BOX}/nm	f_T/GHz	BV_{CEO}/V	$f_T \times BV_{CEO}$/GHz·V
50	10.9	11.3	123.17
100	11.8	12.3	145.14
150	12.9	12.9	166.41

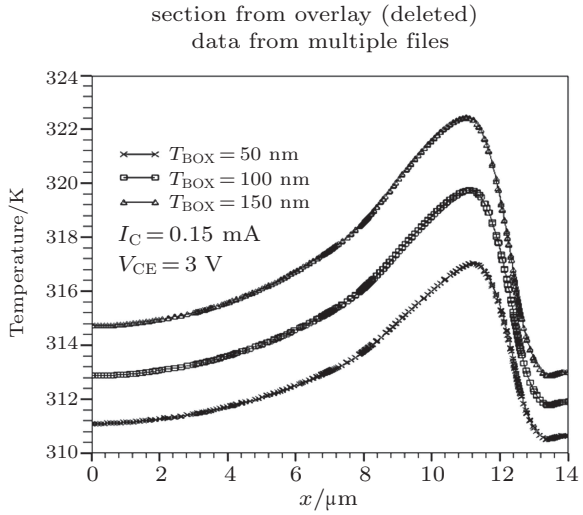


Fig. 10. Device surface temperature profiles of traditional SOI SiGe HBT with different T_{BOX} values.

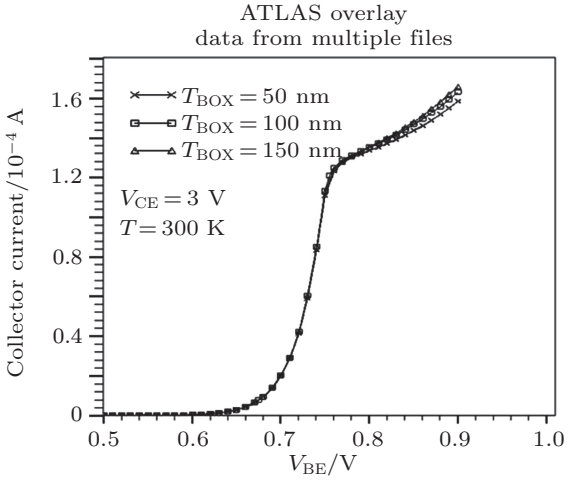


Fig. 11. Comparisons among the plots of collector current versus V_{BE} for traditional SOI SiGe HBT with different T_{BOX} values.

Although the increase of T_{BOX} above improves f_T, BV_{CEO}, and $f_T \times BV_{CEO}$, at the same time, it also causes the device surface temperature to rise as shown in Fig. 10. With the increase of T_{BOX} from 50 nm to 150 nm, the peak device surface temperature (T_{PEAK}) rises from 317 K to 323 K. The rising of the device surface temperature further enhances the self-heating effect of the device, so that the collector current is higher under the same high V_{BE} bias condition as shown in Fig. 11, so the thermal stability of the device is degraded.[19,20]

4. Results of novel SOI SiGe HBT with a thin N^+-buried layer

In order to alleviate the negative effect, i.e., the decrease of electron concentration in collector region and the degradation of thermal stability caused by the increase of T_{BOX} due to lower thermal conductivity of the SiO_2 in SOI structure, a thin N^+-buried layer is introduced into the collector region as shown in Fig. 3.

Figure 12 shows the comparisons among plots of f_T versus J_C for novel SOI SiGe HBTs with different z values. With the decrease of z from 400 nm to 200 nm, the peak f_T improves from 27.2 GHz to 34.6 GHz. The maximum improvement amplitude of f_T is as high as 217.4% compared with that of traditional SOI SiGe HBT without N^+-buried layer in collector region. This is attributed to the N^+-buried layer in collector region which leads to remarkable increase of electron concentration in collector region near SOI insulation layer as shown in Fig. 13, significantly reducing the collector resistance, consequently reducing the $\tau_{bc,SiGe}$, and obviously improving f_T.

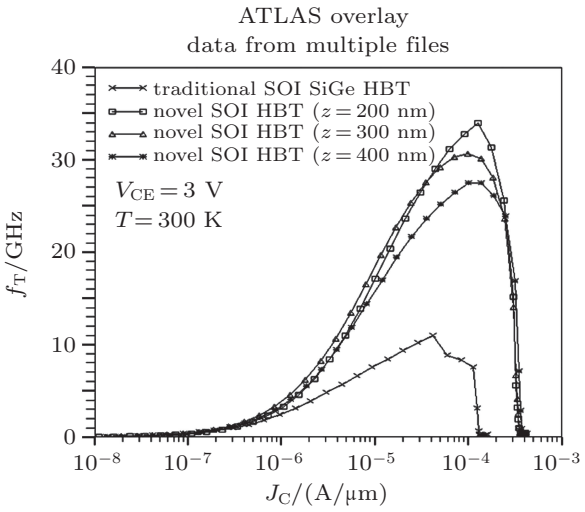


Fig. 12. Comparisonsof plot of f_T versus J_C between traditional SOI SiGe HBT and novel SOI SiGe HBT with different z values.

Figure 14 shows plots of absolute values of the base current versus V_{CE} for novel SOI SiGe HBT with different z values. BV_{CEO} decreases slightly from 11.1 V to 10.5 V, but the product of $f_T \times BV_{CEO}$ increases from 301.9 GHz·V to 363.3 GHz·V. The maximum decrease amplitude of BV_{CEO} is as slightly low as 7.1%, but the maximum increase amplitude of the product of $f_T \times BV_{CEO}$ is as obviously high as 195% compared with those in the case of traditional SOI SiGe HBT without N^+-buried layer in collector region. Table 3 compares parameters for novel SOI SiGe HBTs with different locations of N^+-buried layer in collector region.

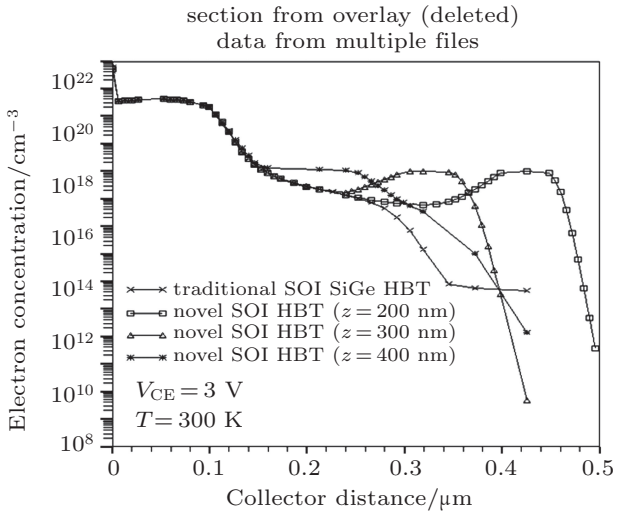


Fig. 13. Electron concentration profiles in collector region for traditional SOI SiGe HBT and novel SOI SiGe HBT with different z values.

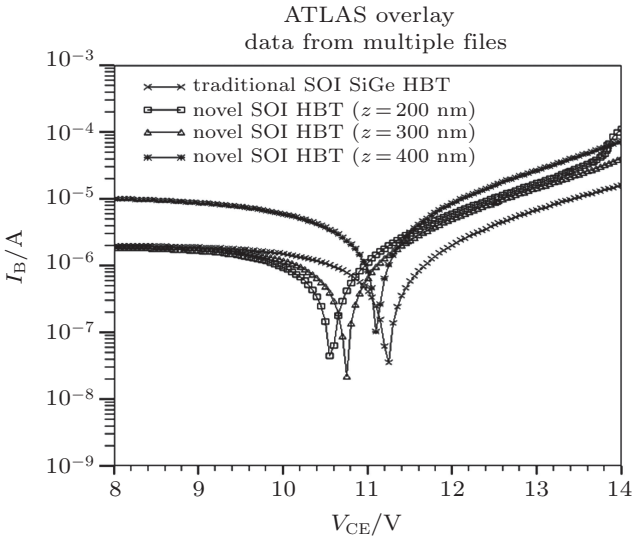


Fig. 14. Plots of absolute value of the base current versus V_{CE} for traditional SOI SiGe HBT and novel SOI SiGe HBT with different z values.

Table 3. Parameters for traditional SOI SiGe HBT and novel SOI SiGe HBT with different z values.

Type of SOI SiGe HBT	f_T/GHz	BV_{CEO}/V	$f_T \times BV_{CEO}$/GHz·V
Traditional SOI SiGe HBT	10.9	11.3	123.17
Novel SOI SiGe HBT ($z = 200$ nm)	34.6	10.5	363.3
Novel SOI SiGe HBT ($z = 300$ nm)	31	10.7	331.7
Novel SOI SiGe HBT ($z = 400$ nm)	27.2	11.1	301.9

As the position of N^+-buried layer in collector region shifts toward SOI insulation layer, the device surface temperature is also reduced as shown in Fig. 15. Peak temperature

T_{PEAK} drops from 315.7 K down to 310.4 K. The peak temperature of T_{PEAK} is reduced by 6.6 K compared with the case in traditional SOI SiGe HBT without N^+-buried layer in collector region. Furthermore, the self-heating effect of the device is weakened, which means that the collector current is smaller under the same high V_{BE} bias condition as shown in Fig. 16.

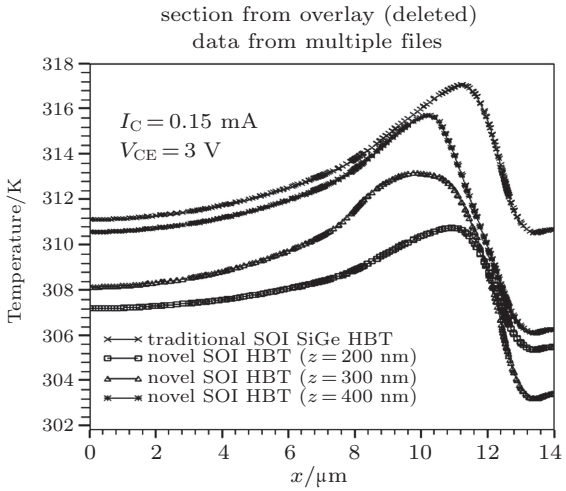


Fig. 15. Surface temperature profiles for traditional SOI SiGe HBT and novel SOI SiGe HBT with different z values.

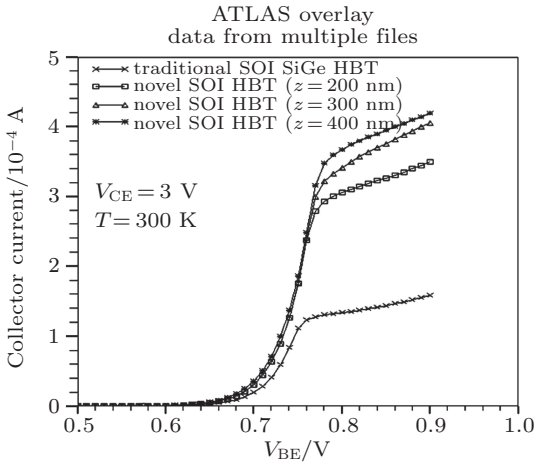


Fig. 16. Comparisons of plot of collector current versus V_{BE} between traditional SOI SiGe HBT and novel SOI SiGe HBT with different z values.

5. Conclusions

The existence of insulation layer SiO_2 in traditional SOI SiGe HBT reduces the FOM of $f_T \times BV_{CEO}$ compared with the case in standard SiGe HBT on bulk silicon. By increasing insulation layer thickness T_{BOX}, although the FOM of $f_T \times BV_{CEO}$ of traditional SOI SiGe HBT can be improved, the self-heating effect is enhanced and the thermal stability of the device is worsened. The introduction of a thin N^+-buried layer into N collector region can alleviate these negative influences. The results show that the FOM of $f_T \times BV_{CEO}$ is greatly improved, at the same time, the device temperature is reduced, and the self-heating effect is weakened as the position of N^+-buried layer in the collector region is shifted toward the substrate insulation layer. The effectiveness of the approach of introducing thin N^+-buried layer into collector region in improving FOM of $f_T \times BV_{CEO}$ and the thermal stability are validated.

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