Technology demonstration of a novel poly-Si nanowire thin film transistor*

Libin Liu(刘立滨), Renrong Liang(梁仁荣)†, Bolin Shan(单柏霖), Jun Xu(许军), and Jing Wang(王敬)

Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics, Tsinghua University, Beijing 100084, *China*

(Received 15 May 2016; revised manuscript received 4 July 2016; published online 30 September 2016)

A simple process flow method for the fabrication of poly-Si nanowire thin film transistors (NW-TFTs) without advanced lithographic tools is introduced in this paper. The cross section of the nanowire channel was manipulated to have a parallelogram shape by combining a two-step etching process and a spacer formation technique. The electrical and temperature characteristics of the developed NW-TFTs are measured in detail and compared with those of conventional planar TFTs (used as a control). The as-demonstrated NW-TFT exhibits a small subthreshold swing (191 mV/dec), a high ON/OFF ratio (8.5×10^7), a low threshold voltage (1.12 V), a decreased OFF-state current, and a low drain-induced-barrier lowering value (70.11 mV/V). The effective trap densities both at the interface and grain boundaries are also significantly reduced in the NW-TFT. The results show that all improvements of the NW-TFT originate from the enhanced gate controllability of the multi-gate over the channel.

Keywords: thin film transistor, poly-Si, nanowire, spacer technique

PACS: 85.30.Tv, 85.35.–p, 85.30.–z **DOI:** 10.1088/1674-1056/25/11/118504

1. Introduction

With superior drive capability and performance stability, polycrystalline-silicon thin film transistors (poly-Si TFTs) have been utilized widely in high definition and fully integrated active matrix flat panel display (AM-FPD) applications.[1] For future high-level applications, such as monolithic three-dimensional integration[2] and system-on-panel circuits,[3,4] better performance is highly desirable for the poly-Si TFTs, e.g., higher drive capability, lower subthreshold swing (SS), and lower OFF-state current ($I_{\rm off}$). However, there are numerous traps at the poly-Si/gate oxide interface and grain boundaries, resulting in degraded subthreshold swing (SS), high OFF-state current, low ON-state current ($I_{\rm on}$), and high threshold voltage ($V_{\rm TH}$).[5–7] The high anomalous leakage current generated by thermionic emission and tunneling via the grain boundaries deteriorates the power of the circuit and the display quality of the AM-FPD.[8,9] In addition, the existence of a pseudo-subthreshold regime in the above threshold regime further worsens the switching properties.[10]

Fin field-effect transistors (FinFETs), with a multi-gate structure, have been extensively examined due to their superior gate controllability and electrical performance.[11–13] Recently, multi-gate TFTs with a nanowire channel have also been proposed to improve their electrical performance. Based on the stated goals of low cost and the capacity for mass production on large panels, earlier studies demonstrated that the nanowire channel can be formed by using a spacer formation technique.[14–16] However, these nanowire channels usually have cone-shaped cross-sections, with a large thickness at the bottom, where less control is obtained from the gate and the majority of the current leakage path is located. The performance of these TFTs is also dependent on the material of the substrate.[17,18] In this work, we introduce a novel multi-gate poly-Si TFT with a parallelogram-shaped nanowire channel without the use of advanced lithographic tools. A gate-all-around structure was accessed and the influence of the substrate could be eliminated in our method. The result was a high-performance nanowire TFT (NW-TFT) with an improved drive capability, reduced SS, decreased OFF-state current, and lower threshold voltage. The proposed NW-TFT is shown to be a promising candidate for many advanced applications.

2. Device fabrication

The detailed fabrication process of the proposed NW-TFT is described as follows, with the key steps shown schematically in Fig. 1. The fabrication begins with depositing a 100-nm-thick SiN layer using a Low Pressure Chemical Vapor Deposition (LPCVD) system on 4-inch single-crystal silicon wafers. Next, a 200-nm-thick sacrificial layer of SiO_x was deposited using a plasma enhanced chemical vapor deposition (PECVD) system at 300 °C. The sacrificial SiO_x was then etched to form several dummy strips using a two-step etching process in an inductively coupled plasma (ICP) reactor with fluorine chemistry. The two-step etching process consisted

*Project supported by the National Key Research and Development Program of China (Grant Nos. 2016YFA0302300 and 2016YFA0200404), the National Natural Science Foundation of China (Grant No. 61306105), the National Science and Technology Major Project of China (Grant No. 2011ZX02708-002), the Tsinghua University Initiative Scientific Research Program, China and the Tsinghua National Laboratory for Information Science and Technology (TNList) Cross-discipline Foundation, China.

†Corresponding author. E-mail: liangrr@mail.tsinghua.edu.cn

© 2016 Chinese Physical Society and IOP Publishing Ltd

of two sequential etching steps. First, a highly anisotropic etching was used to remove the first 100-nm-thick SiO_x, generating a steep step profile. Second, the remaining SiO_x was isotropically etched to form a gradual step profile. Figure 1(a) shows the dummy strips with a two-step profile formed by the two-step etching process, which are the key steps for manipulating the cross-sectional shape of the nanowire. Then a 120-nm-thick poly-Si thin film was conformally deposited through a Reduced Pressure Chemical Vapor Deposition (RPCVD) system at 600 °C as shown in Fig. 1(b). After patterning the source/drain (S/D) regions, the poly-Si thin film was etched using the ICP reactor with a highly anisotropic recipe, forming a pair of poly-Si sidewall spacers *in situ* residing against the side walls of the SiO_x dummy strips, as shown in Fig. 1(c). These poly-Si spacers acted as the nanowire channel and were naturally connected to the S/D regions. As shown in Fig. 1(d), after removing the 200-nm-thick PECVD SiO_x strips using a diluted hydrofluoric solution, a 7.5-nm-thick SiO_2 thermal oxide was grown as the gate oxide. Afterwards, as shown in Fig. 1(e), 200-nm-thick platinum (Pt) with an adhesion titanium (Ti) layer was sputtered and patterned as the gate electrode using lift-off. After the formation of the gate electrode, a self-aligned phosphorous ion implantation was performed at 30 keV with a dose of 4×10^{15} cm^{-2} to dope the S/D regions. The dopants were then activated at 600 °C for 12 h in N_2 ambient. After the definition of S/D contact holes, a 200-nm-thick Al-1%Si alloy was sputtered and patterned as the S/D contact pads. Finally, the devices were sintered in forming gas at 430 °C for 30 min to complete the device fabrication. In addition to the developed NW-TFTs, conventional planar TFTs were also fabricated as control devices on the same wafers using the same lithographic masks.

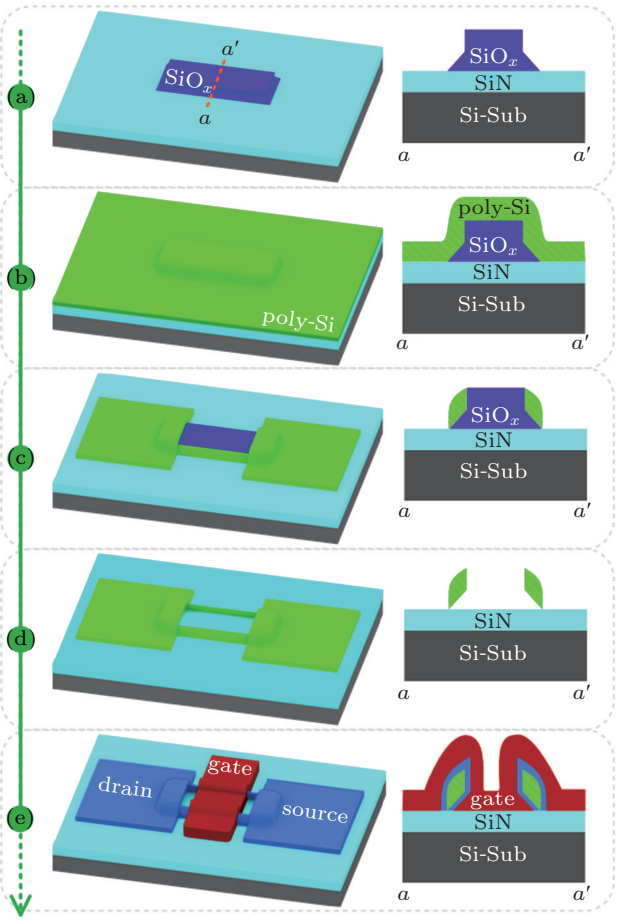


Fig. 1. (color online) Three-dimensional (3D) and cross-sectional illustrations of the key fabrication steps of the proposed NW-TFTs; the cut-planes of all cross-sectional graphs are located at the middle of the channel and perpendicular to the gate length direction, as shown in panel (a) and indicated by the orange line (a–a'). (a) A two-stage step profile was obtained after etching the sacrificial SiO_x using a two-step etching process; (b) a 120-nm-thick poly-Si was conformally deposited by RPCVD; (c) two nanowire channels and S/D regions were simultaneously obtained by precisely etching the poly-Si thin film; (d) the SiO_x was removed by a diluted hydrofluoric solution; and (e) the gate stack is formed.

The NW-TFTs and the planar TFTs were examined using a Keysight B1500A Semiconductor Device Analyzer. The transmission electron microscopy (TEM) and scanning electron microscopy (SEM) measurements were carried out using a high-resolution transmission electron microscope (FEI Tecnai G2 F20) and a field-emission scanning electron microscope (FEI Quanta 450 FEG), respectively.

3. Results and discussion

A typical SEM image of the fabricated NW-TFT is shown in Fig. 2(a). The gate length (L) of the NW-TFT is around 4 μm. Two nanowire channels were connected to the S/D regions and there is a gap between the S/D regions and the gate electrode. The existence of the S/D regions increases the yield of the nanowire channel, and it is also helpful for reducing the S/D series resistance. The cross-sectional TEM image of the stacked nanowire channel is shown in Fig. 2(b). The cutting plane of the focus ion beam precision TEM is located at the center of the nanowire channel, as indicated in Fig. 2(a) by line a–a'. A nanowire channel with a parallelogram-shaped cross section is clearly visible, and the SiO_2 and gate metal wrap around it. The height of the nanowire is about 200 nm, which is equal to the thickness of the sacrificial SiO_x. It can be seen that little connection exists between the channel and the SiN substrate, so the substrate has little effect on the device performance. Thus, the nanowire channel and the multi-gate structure are successfully demonstrated. Although the channel is not fully surrounded by the gate metal, due to the non-conformal growth of the Pt/Ti layer by sputtering, the validity of the proposed process flow will not be affected. A fully conformal gate stack can be obtained by using LPCVD[14] or atomic layer deposition techniques. To conduct a fair comparison with the control planar TFT, the effective gate width (W) of the NW-TFT is defined by the perimeter of the channel covered by the gate, which is $\sim 0.4 \times 2 = 0.8$ μm; the gate width (W) of the planar TFT is 20 μm.

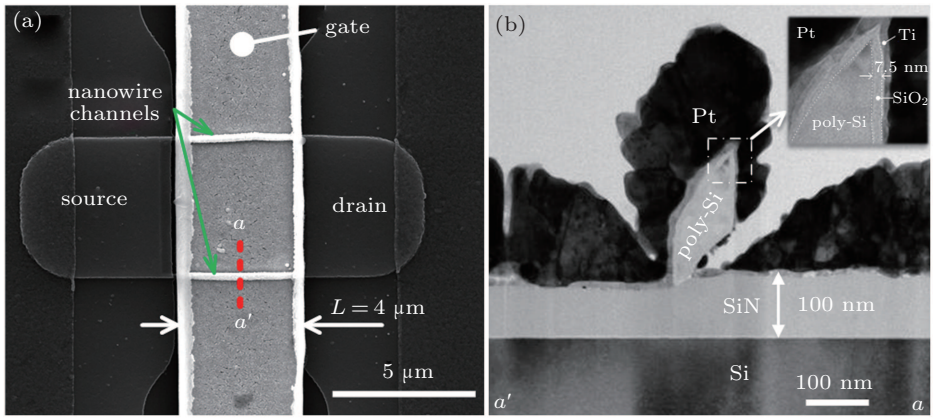


Fig. 2. (color online) (a) SEM graph of the fabricated NW-TFT with two nanowire channels, where the gate length is 4 μm; and (b) cross-sectional TEM graph of the nanowire channel along the red line (a–a') shown in panel (a). The inset in panel (b) shows the gate stack of the device, which is Pt/Ti/SiO_2/Poly-Si. The effective gate width of the NW-TFT is around 0.8 μm, and the gate oxide thickness is 7.5 nm.

Figure 3 shows the transfer characteristics ($I_{DS} - V_{GS}$) of both the NW-TFT and planar TFT at V_{DS} values of 0.1 V and 1.0 V. The illustrated drain current (I_{DS}) values of both devices were normalized by the effective gate width for fair comparison. V_{TH} is defined as the gate voltage (V_{GS}) at which the drain current reaches 10 nA$\times W/L$ under $V_{DS} = 0.1$ V. The minimum subthreshold swing in the subthreshold regime is chosen as the SS in this work. Flat band voltage (V_{FB}) is defined as the gate voltage corresponding to the minimum drain current. Although both TFTs show good switching characteristics, the electrical properties of the NW-TFT are superior to those of the planar TFT. The planar TFT revealed a large V_{TH} of 1.43 V, a low I_{on}/I_{off} ratio of 5.87×10^5 at $V_{DS} = 0.1$ V, and an SS of 240 mV/dec, while the NW-TFT revealed a smaller V_{TH} of 1.12 V, a higher I_{on}/I_{off} ratio of 8.51×10^7 at $V_{DS} = 0.1$ V, and a smaller SS of 191 mV/dec. In addition, the nanowire structure is also beneficial for suppressing the drain induced barrier lowering (DIBL) effect. The DIBL value was reduced from 159.40 mV/V (planar TFT) to 70.11 mV/V (NW-TFT), which indicates a superior scaling down capability.

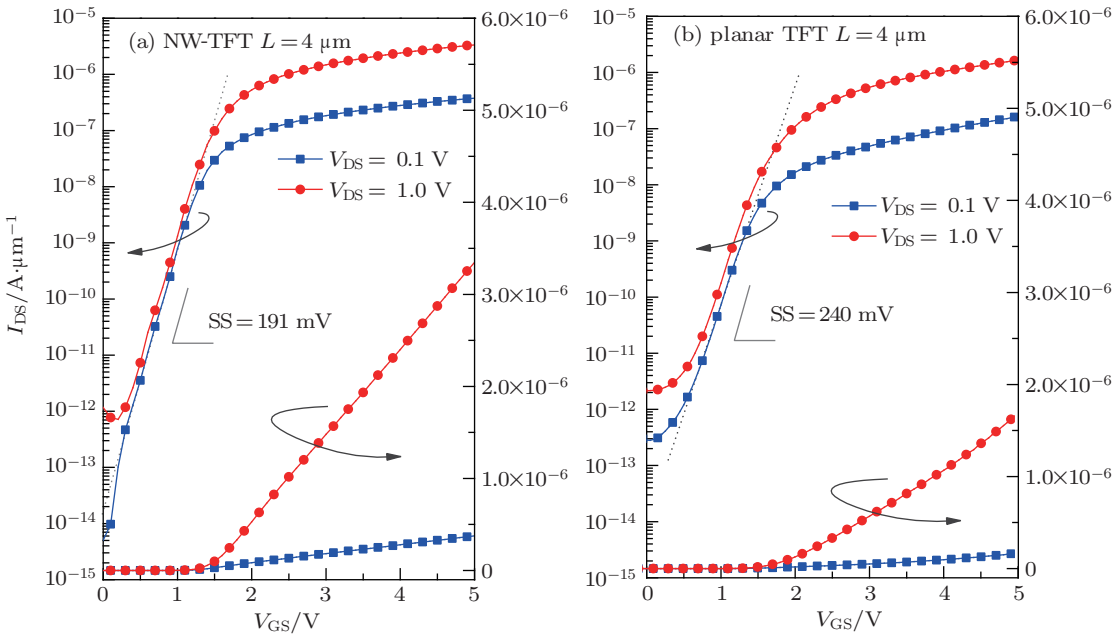


Fig. 3. (color online) I_{DS}–V_{GS} curves of (a) the fabricated NW-TFT; and (b) the fabricated planar TFT (in both logarithmic and linear scales).

A smaller SS indicates a faster switching characteristic and is of vital importance for low-power and low-voltage applications. The SS of the NW-TFT was 191 mV/dec and remained almost unchanged in about 5 orders of magnitude from 10^{-8} to 10^{-13} A/μm, while that of the planar TFT was 240 mV/dec and only lasted in 2 orders of magnitude from 10^{-9} to 10^{-11} A/μm. In the poly-Si TFT, the subthreshold behavior is mainly dominated by the effective trap state density (N_T) near the poly-Si/SiO_2 interface. By neglecting the depletion capacitance in the channel, the N_T can be estimated from

the SS using the following relationship:[19]

$$N_{\mathrm{T}} = \left(\frac{\mathrm{SS}}{\ln 10}\frac{q}{kT} - 1\right)\frac{C_{\mathrm{ox}}}{q},$$

where C_{ox}, q, k, and T are the gate oxide capacitance per unit area, the electron charge, the Boltzmann constant, and the temperature, respectively. The NW-TFT exhibits an N_{T} of 6.44×10^{12} cm^{-2}, whereas the planar TFT has an N_{T} of 8.70×10^{12} cm^{-2}. Although both the NW-TFT and planar TFT were fabricated using the same interface passivation method, the NW-TFT obtains a lower N_{T}. The gate controllability over the channel is boosted by the multi-gate structure. Due to the sharing of the depletion charge in the channel, a lower V_{GS} is needed for the same surface potential in the channel.[20] Thus, the nanowire structure with a multi-gate configuration can significantly reduce the effective trap state density and improve the SS.

The I_{off} is also suppressed by the nanowire structure. As seen from Fig. 3, the OFF-state current of the NW-TFT is much smaller than that of the planar TFT, especially at low V_{DS} values. The I_{off} in the poly-Si TFT originates from the carrier emission via grain boundary traps and band-to-band tunneling in the channel near the drain.[21] At low V_{DS}, the dominant leakage mechanism is carrier emission via the grain boundaries; the greater the gate controllability, the lower the Fermi level, and the higher the thermionic emission barrier for the carriers. Furthermore, the enhanced gate controllability can also reduce the lateral electric field near the drain, which is also helpful for reducing the tunneling leakage current at the drain side.

The I_{on} is relevant for drive capability. It is obvious that in the above threshold regime, the normalized I_{on} of the NW-TFT is 2 times higher than that of the planar TFT, especially at low V_{GS}. Due to the increased I_{on} and suppressed I_{off}, the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of the NW-TFT increases about 2 orders of magnitude. The improvement of the driven capability can be revealed by the carrier mobility. The field effect mobility μ_{EF} was calculated by applying the following equation:[22]

$$\mu_{\mathrm{EF}} = \frac{W}{L}\frac{g_{\mathrm{m}}}{C_{\mathrm{ox}}V_{\mathrm{DS}}}, \quad g_{\mathrm{m}} = \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GS}}},$$

where g_{m} is the transconductance of the device. The μ_{EF} was calculated as a function of V_{GS} and is shown in Fig. 4. It can be seen that the μ_{EF} of the NW-TFT is several times higher than that of the planar TFT, especially at low V_{GS}. The low field mobility (at $V_{\mathrm{GS}} \approx V_{\mathrm{TH}}$) of the NW-TFT is about 10.09 cm^2/V·s, while that of the planar TFT is only 2.59 cm^2/V·s. An energy band diagram of the poly-Si channel in the ON-state is shown in Fig. 4(b). The grain boundaries induce grain boundary barriers in the channel, and mobility is severely reduced by these grain boundary barriers. Therefore, in the poly-Si TFT, the μ_{EF} is governed by the scattering both at the grain boundaries and inside the grains, which can be written as[23]

$$\frac{1}{\mu_{\mathrm{EF}}} = \frac{1}{\mu_{\mathrm{gb}}} + \frac{1}{\mu_{\mathrm{grain}}},$$

where μ_{gb} and μ_{grain} are the mobilities at the grain boundaries and inside the grains, respectively. μ_{gb} is governed by the thermionic emission over the grain boundary barrier, which has an experiential relationship with grain boundary barrier height (ψ_{GB}) as follows: $\mu_{\mathrm{gb}} = \mu_{\mathrm{gb0}}\exp(-\alpha\psi_{\mathrm{GB}})$, where μ_{gb0} and α are constants. The μ_{grain} is almost the same as the mobility of single-crystal silicon and is higher than μ_{gb}. Therefore, the μ_{EF} of the poly-TFT is dominated by μ_{gb}, and is therefore determined by ψ_{GB}. With the multi-gate and nanowire structure, gate controllability over the channel charges increases. Therefore, at the same V_{GS}, the ψ_{GB} in the NW-TFT is lower than that of the planar TFT. Thus, the NW-TFT has a much higher I_{on} and μ_{EF}.

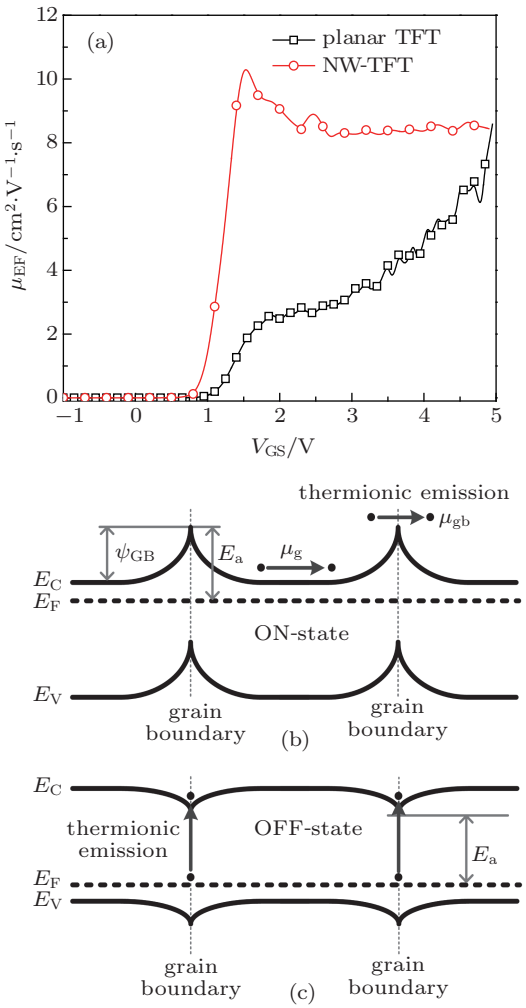


Fig. 4. (color online) (a) Low field mobility μ_{EF} of NW-TFT and planar TFT at $V_{\mathrm{DS}} = 0.1$ V; (b) energy band diagram of the poly-Si in the ON-state; and (c) energy band diagram of the poly-Si in the OFF-state regime. E_{C}, E_{V}, and E_{F} stand for the conduction band, valence band, and Fermi level, respectively, and E_{a} is the activation energy.

In order to compare the ψ_{GB} values, the current activation

energy (E_a) was estimated. According to the Arrhenius theory, the drain current activation energy E_a can be extracted via the temperature test based on the following equation:[21]

$$I_{DS}(T) = I_0 \exp\left(-\frac{E_a}{kT}\right),$$

where I_0 is a constant independent of temperature. The value of E_a measures the difference between the conduction band edge and the energy of the grain boundary states within kT of the Fermi level. As shown in Figs. 4(b) and 4(c), in the ON-state, the value of E_a represents the carrier transport barrier resulting from the trap states in the channel, while in the OFF-state (low V_{GS}), E_a is the energy required for carriers to leak via trap states. The extracted E_a is shown as a function of the gate voltage in Fig. 5; it is calculated from the I_{DS}–V_{GS} curves obtained at 30 °C, 60 °C, 90 °C, 120 °C, and 150 °C. Compared with the planar TFT, the NW-TFT exhibits a much lower E_a in the ON-state regime ($V_{GS} \gtrsim 2$ V). Thus, a lower barrier height and hence a higher I_{on} is expected. In the OFF-state regime ($V_{GS} \lesssim 1$ V), the NW-TFT shows a higher E_a, which suppresses the trap-assisted leakage current and contributes to a lower I_{off}. Furthermore, a steeper E_a–V_{GS} profile can also be found in the subthreshold regime for the NW-TFT, indicating a lower effective interface trap density (N_T). The difference in the E_a is also caused by the nanowire structure, which applies enhanced gate control to not only the free carriers but also the trap states in the channel. In addition, the extracted I_{on}/I_{off} ratio and SS are shown as a function of temperature in the inset of Fig. 5. It is clear that the performance improvement of the NW-TFT can be maintained in a wide range of temperatures. The I_{on}/I_{off} ratio of the NW-TFT is over one order of magnitude higher than that of the planar TFT, and the SS value is always smaller for the former than for the latter.

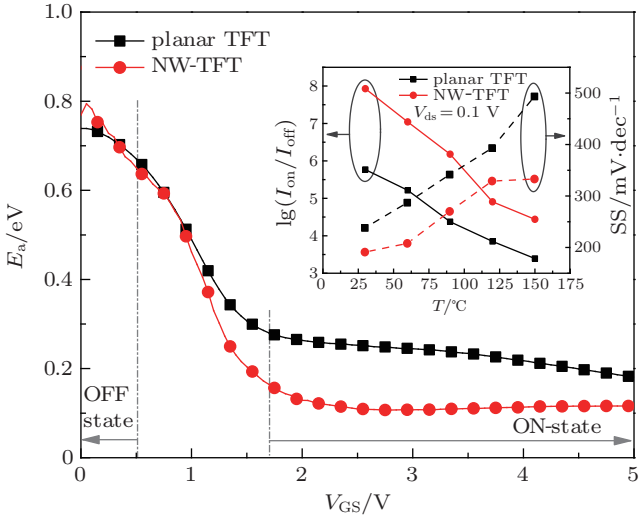


Fig. 5. (color online) Activation energy (E_a) of the NW-TFT and planar TFT as a function of gate voltage V_{GS}. The inset shows the extracted I_{on}/I_{off} ratio and SS at different temperatures.

The traps in the grain boundary and inside the grains not only trap carriers, they also reduce carrier mobility. Therefore, these traps are expected to be reduced or even eliminated. The grain-boundary trap-state density (Q_T) of the NW-TFT and planar TFT can be estimated using the method proposed by Levinson *et al.*[23] and Proano *et al.*[24] Figure 6 shows the $\ln[I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at a low drain voltage ($V_{DS} = 0.1$ V). The Q_T of the NW-TFT is 6.58×10^{12} cm^{-2}, whereas the planar TFT has a Q_T of 8.2×10^{12} cm^{-2}. Due to the multi-gate structure, the traps in the grain boundaries are shared by the adjacent gate, and thus, the gate controllability over the grain boundary traps is also enhanced. Therefore, the NW-TFT shows a lower Q_T and a lower ψ_{GB}.

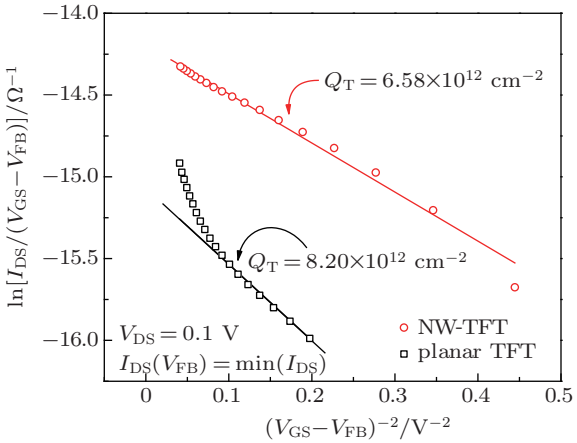


Fig. 6. (color online) $\ln[I_{DS}/(V_{GS}-V_{FB})]$ versus $1/(V_{GS}-V_{FB})^2$ curves at a low drain voltage ($V_{DS} = 0.1$ V); the markers and lines represent the measured data and the linearly fitted curves, respectively.

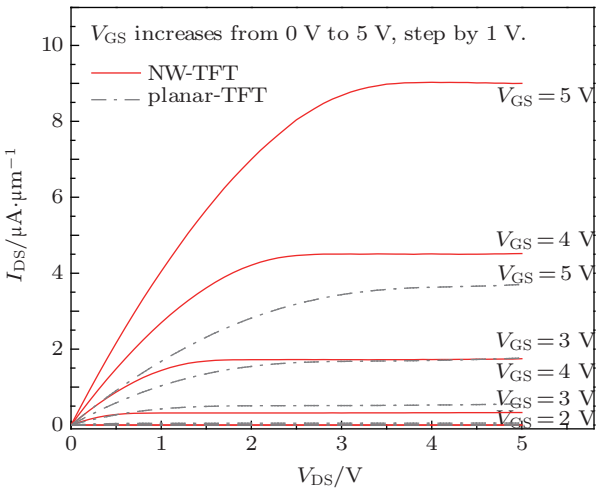


Fig. 7. (color online) Output characteristics ($I_{DS}-V_{DS}$) of the NW-TFT and the planar TFT.

The output characteristics ($I_{DS}-V_{DS}$) of the NW-TFT and the planar TFT are shown in Fig. 7. Clear saturation without the kink effect can be observed for the NW-TFT, even at high V_{DS} values. The comparison of the NW-TFT and planar TFT

is shown in Table 1. Because poly-Si was directly grown by using the RPCVD system, there were fine grains and rough surfaces in the poly-Si channel. Although the mobility is not high enough (even for the NW-TFT), the mobility of the NW-TFT could be further boosted if advanced crystallization methods were used such as solid phase recrystallization,[25] metal induced crystallization,[26] and laser annealing.[27]

Table 1. Comparison of the NW-TFT and the planar TFT.

Variable	NW-TFT	Planar TFT
W/μm	0.8	20
L/μm	4	4
μ_{EF}/cm^2·V^{-1}·s^{-1}	10.09	2.59
V_{TH}/V	1.12	1.43
I_{on}/I_{off}	8.51×10^7	5.87×10^5
SS/mV·dec^{-1}	191	240
DIBL/mV·V^{-1}	70.11	159.40
N_T/cm^{-2}	6.44×10^{12}	8.70×10^{12}
Q_T/cm^{-2}	6.58×10^{12}	8.20×10^{12}

4. Conclusions

A simple method for fabricating poly-Si TFTs with a nanowire channel to improve performance has been developed. The cross section of the nanowire channel was molded into a parallelogram shape using a two-step etching process. This method avoids using advanced lithographic tools, so it is suitable for mass production of high performance TFTs in large or low-cost electronics. Compared with the conventional planar TFT, the NW-TFT exhibits improved drive capability, reduced I_{off}, lower V_{TH}, lower SS, and lower DIBL. These improvements all originate from the improved gate controllability over the carriers and trap states in the poly-Si channel. Similarly, the effective interface trap density and grain boundary trap density can be effectively reduced with the multi-gate structure. Thus, the nanowire structure poly-Si TFT is a promising candidate as a high-performance TFT.

References

[1] Stewart M, Howell R S, Pires L and Hatalis M K 2001 *IEEE Trans. Electron Dev.* **48** 845

[2] Shen C H, Shieh J M, Wu T T, Huang W H, Yang C C, Wan C J, Lin C D, Wang H H, Chen B Y, Huang G W, Lien Y C, Wong S, Wang C, Lai Y C, Chen C F, Chang M F, Hu C and Yang F L 2013 *Electron Devices Meeting (IEDM),* 2013 *IEEE International*, December 9–11, 2013, Washington, United States, p. 9.3.1

[3] Meng Z, Wang M and Wong M 2000 *IEEE Trans. Electron Dev.* **47** 404

[4] Lee T Y, Chiu C C, Liu Y C, Liu C C, King Y C and Lin C J 2008 *IEEE Electron Dev. Lett.* **29** 906

[5] Chou T K A and Kanicki J 1999 *Jpn. J. Appl. Phys.* **38** 2251

[6] Sun J H, Shen W Z and Meng F Y 2003 *J. Appl. Phys.* **93** 9615

[7] Genshiro K, Shinzo T, Takashi O, Masahiro M and Masakiyo M 2006 *J. Appl. Phys.* **100** 114507

[8] Kim C H, Sohn K S and Jang J 1997 *J. Appl. Phys.* **81** 8084

[9] Wang L Y, Sun L, Han D D, Wang Y, Chan M S and Zhang S D 2015 *Sci. China-Info Sci.* **58** 42401

[10] Li T S and Lin P S 1993 *IEEE Electron Dev. Lett.* **14** 240

[11] Yang F L, Chen H Y, Huang C C, Ge C H, Su K W, Huang C C, Chang C Y, Lin D W, Wu C C, Ho J K, Lee W C,Yeo Y C, Carlos H D, Liang M S, Jack Y C S and Hu C 2003 *VLSI Technology,* 2003 *Symposium on*, June 10–12, 2003, Kyoto, Japan, p. 138

[12] Yu J T, Chen S M, Chen J J and Huang P C 2015 *Chin. Phys. B* **24** 119401

[13] Ma L H, Han W H, Wang H, Lyu Q F, Zhang W, Yang X and Yang H F 2016 *Chin. Phys. B* **25** 068103

[14] Chang C W, Deng C K, Chang H R, Chang C L and Lei T F 2007 *IEEE Electron Dev. Lett.* **28** 993

[15] Wu C Y, Liu Y T, Liao T C, Yu M H and Cheng H C 2011 *IEEE Electron Dev. Lett.* **32** 1095

[16] Kang T K, Yang Y Y and Chien F T 2014 *IEEE Trans. Electron Dev.* **61** 2113

[17] Li J, Wu C Y, Liu J P, Zhao S Y, Meng Z G, Xiong S Z and Zhang L Z 2006 *Chin. Phys. B* **15** 1330

[18] Gao X, Lin L, Liu Y and Huang X 2015 *J. Disp. Technol.* **11** 666

[19] Dimitriadis C A, Coxon P A, Dozsa L, Papadimitriou L and Economou L 1992 *IEEE Trans. Electron Dev.* **39** 598

[20] Liu L B, Liang R R, Zhao L F, Wang J and Xu J 2014 *Jpn. J. Appl. Phys.* **53** 064304

[21] Olasupo K R and Hatalis M K 1996 *IEEE Trans. Electron Dev.* **43** 1218

[22] Hung B F, Chiang K C, Huang C C, Chin A and McAlister S P 2005 *IEEE Electron Dev. Lett.* **26** 384

[23] Levinson J, Shepherd F R, Scanlon P J, Westwood W D, Este G and Rider M 1982 *J. Appl. Phys.* **53** 1193

[24] Proano R E, Misage R S and Ast D G 1989 *IEEE Electron Dev. Lett.* **36** 1915

[25] Pichon L, Mercha A, Carin R, Bonnaud O, Mohammed-Brahim T, Helen Y and Rogel R 2000 *Appl. Phys. Lett.* **77** 576

[26] Man W, Hoi S K, Meng Z G, Li Y, Wu C Y, Zhao S Y, Li J, Man W, Hoi S K and Xiong S Z 2008 *Chin. Phys. B* **17** 1415

[27] Yamano M, Kuroki S I, Sato T and Kotani k 2014 *Jpn. J. Appl. Phys.* **53** 03CC02