Ultra-low temperature radio-frequency performance of partially depleted silicon-on-insulator n-type metal–oxide–semiconductor field-effect transistors with tunnel diode body contact structures

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Radio-frequency (RF) characteristics under ultra-low temperature of multi-finger partially depleted silicon-on-insulator (PD SOI) n-type metal–oxide–semiconductor field-effect transistors (nMOSFETs) with tunnel diode body-contact (TDBC) structure and T-gate body-contact (TB) structure are investigated in this paper. When operating at 77 K, TDBC device suppresses floating-body effect (FBE) as well as the TB device. For TB device and TDBC device, cut-off frequency (f_T) improves as the temperature decreases to liquid-helium temperature (77 K) while that of the maximum oscillation frequency (f_{MAX}) is opposite due to the decrease of the unilateral power gain. While operating under 77 K, f_T and f_{MAX} of TDBC device reach to 125 GHz and 77 GHz, representing 8% and 15% improvements compared with those of TB device, respectively, which is mainly due to the lower parasitic resistances and capacitances. The results indicate that TDBC SOI MOSFETs could be considered as promising candidates for analog and RF applications over a wide range of temperatures and there is immense potential for the development of RF CMOS integrated circuits for cryogenic applications.

Keywords: partially depleted silicon-on-insulator, radio-frequency, body contact, ultra-low temperature

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1. Introduction

Silicon-on-insulator (SOI) technology has become more popular as a potential technology for low-power microwave circuits due to the advantages of the improved frequency performance through reduced capacitance, high mobility, and a reduction in the interconnect length, compared with bulk-Si technology.[1] Because of lower parasitic gate capacitance, the floating body (FB) structure has better frequency performance compared with body contact structures.[2] However, the main concern for FB structure is the floating body effect (FBE) caused by the impact-ionization under high drain voltage. FBE limited the application of partially depleted (PD) SOI metal–oxide–semiconductor field-effect transistors (MOSFETs) in analog circuits and RF circuits due to Kink effect.[3] In addition, the body potential instability and an abnormal subthreshold swing, caused by FBE, are also disadvantageous factors.[4] To suppress FBE in PD SOI MOSFETs, body contact methods with different structures have been proposed, such as T-gate body contact (TB) structure, H-gate body contact (HB) structure, and so on. The tunnel diode body contact (TDBC) structure was proposed to suppress FBE and improve RF performance by using a tunnel diode under the source region.[5] In contrast from the conventional body contact structure, TDBC structure efficiently suppresses FBE and body-instability problems with smaller areas compared with TB structure and achieves better f_T and f_{MAX} with respect to smaller parasitic gate-source capacitance.[6] The TDBC structure also shows excellent immunity of back gate bias effect[7] compared with FB and TB devices. Most importantly, the fabrication process of TDBC structure is fully compatible with the usual SOI CMOS technology.

Small signal ac performances of multi-finger PD SOI nMOSFET with TDBC structure and conventional TB structure manufactured by employing a 0.13-μm SOI CMOS technology are investigated at 77 K and 300 K. Moreover, the stability factors of devices based on the small-signal model parameters are derived and the effects of temperature are also investigated for RF applications.

2. Proposed device structure

The multi-finger PD SOI nMOSFETs with TDBC structure and TB structure are fabricated in 0.13-μm SOI CMOS technology to investigate the RF performance. The devices designed with multi-fingers investigated in this paper have the same dimensions: the gate length is 0.13 μm and the total width is 20 μm. The unit finger width is 5 μm and the finger number is 4. The thicknesses for silicon film (T_{si}) and buried oxides (T_{box}) for the devices are 100 nm and 145 nm, respectively. For the TB device, p^+ implantation is performed to form the p^+ body contact area. Figure 1 shows the top

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view of TB device and TDBC device while the TB structure takes more area. Instead of an n^+ source as in a conventional TB SOI MOSFET, an Esaki tunnel diode[8] which can effectively release the accumulated body carriers is embedded in the source region, adjacent to the buried oxide interface requiring an extra mask of p^+-type diffusion region. The fabrication procedure of the TDBC SOI nMOSFET can be found in Ref. [5]. Figure 2(b) shows the band diagram for the n^+ source/p^+/p-body/n^+ drain structure. With reference to Fig. 2, the holes caused by FBE flow to the p^+ region and are then released by Esaki tunneling to suppress the floating body effect.

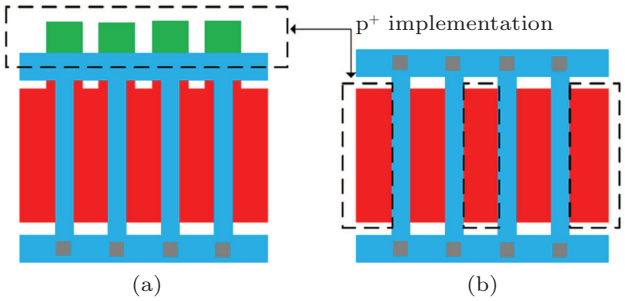


Fig. 1. (color online) (a) Top view of TB nMOSFET and (b) TDBC nMOSFET.

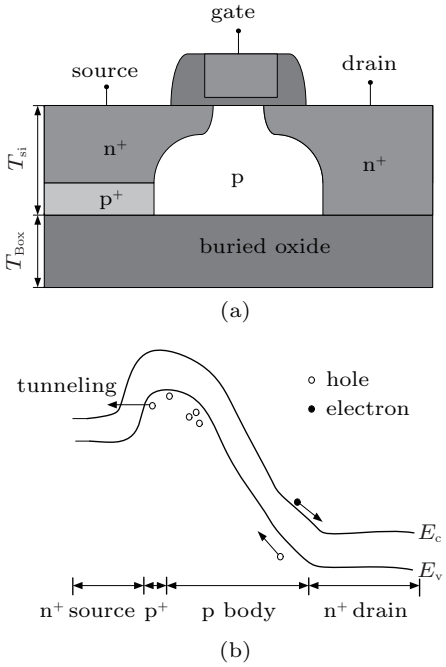


Fig. 2. (a) Cross-sectional schematic of the proposed TDBC SOI MOSFET structure. (b) Band diagram for the n^+ source/p^+/p-body/n^+ drain structure.

3. Results and discussion

The devices were used to perform a *S*-parameter measurement under liquid-helium temperature (77 K) and room temperature (300 K) from 1 GHz to 15 GHz. To extract the practical performance of the devices, the measured *S*-parameters are de-embedded using open and short de-embedding structures. Threshold voltage (V_{th}) of TDBC, and TB device extracted when the drain current equals $0.1W/L$ μA (W is the total gate width, L is the gate length) at a constant drain voltage ($V_d = 1.2$ V) is 0.38 V, and 0.306 V at 77 K and 0.241 V, and 0.176 V at 300 K, respectively. The reason for the higher threshold of TDBC is the boron diffused into the channel region at the anneal stage. The output characteristic and drain conductance (G_{ds}) of the devices under different temperatures when V_g is 0.8 V is shown in Fig. 3. As shown in Fig. 3, there is no kink phenomena appearing in these devices under both temperatures.

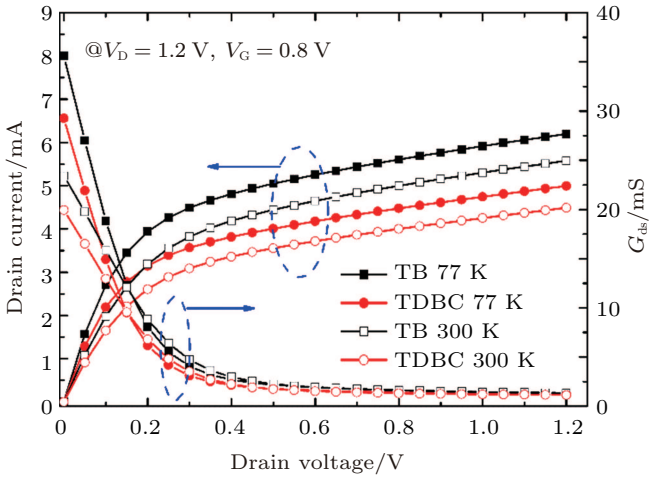


Fig. 3. (color online) G_{ds} of TB and TDBC vary with drain voltage at $V_g = 0.8$ V.

To compare the small signal characteristics of TB and TDBC devices, a simple small signal equivalent circuit is illustrated in Fig. 4, where G_{ds} is the drain conductance and G_m is the trans-conductance, C_{ds}, C_{gs}, and C_{gd} are drain-to-source capacitance, gate-to-source capacitance, and gate-to-drain capacitance, respectively. R_g, R_s, and R_d are gate resistance, source resistance, and drain resistance, respectively. The parasitic resistance and capacitance could be extracted by the following equations:

$$R_g = \mathrm{Re}(Z_{11} - Z_{12}), \tag{1}$$

$$G_{ds} = \mathrm{Re}(Y_{22}), \tag{2}$$

$$G_m = \mathrm{Re}(Y_{21}), \tag{3}$$

$$C_{gs} = \mathrm{Im}(Y_{11} + Y_{12})/(2\pi f), \tag{4}$$

$$C_{gd} = -\mathrm{Im}(Y_{12})/(2\pi f). \tag{5}$$

Figure 5 shows G_{ds} of two types of devices extracted by the *S*-parameters varying with frequency at 300 K and 77 K. Possibly due to the existence of body resistance, the TB device shows higher G_{ds} compared with TDBC device. Moreover, compared with G_{ds} shown in Figs. 3 and 5, the existence of body resistance may cause G_{ds} degradation in TB device at high frequency.[9] Figure 6 shows the comparison of the trans-conductance (G_m) extracted by Re (Y_{21}) under the given bias condition at different temperatures. The G_{ds} and G_m increase with the decrease in temperature, mainly attributed to the increase in the effective mobility at low temperature.

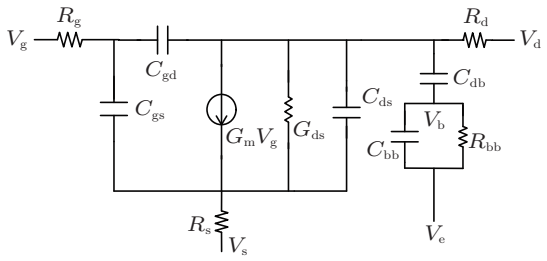


Fig. 4. The small signal equivalent circuit of the SOI MOSFET.

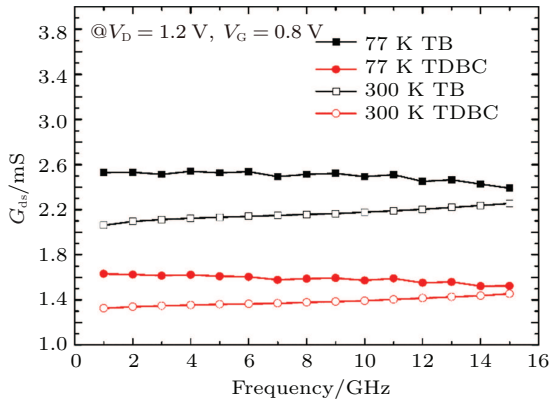


Fig. 5. (color online) The G_{ds} as a function of frequency at 300 K and 77 K for TB and TDBC devices, respectively.

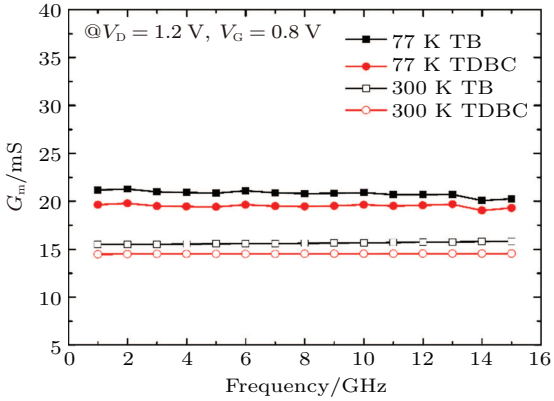


Fig. 6. (color online) The G_m as a function of frequency at 300 K and 77 K for TB and TDBC devices, respectively.

Due to the design rules limiting that the gate contact was forbidden upon active region, the gate of TDBC device is contacted from both sides and TB device is contacted from only one side, as shown in Fig. 1. The gate resistance extracted from the measured S-parameters at $V_G = 0.8$ V, $V_D = 1.2$ V are shown in Fig. 7. The parasitic gate resistance of the device with TDBC structure represents $\sim 60\%$ and $\sim 30\%$ lower than that of TB devices at 77 K and 300 K, respectively. The decrease in the gate resistance at 77 K is due to lower poly/silicide resistances. Because the existence of body resistance in TB structure raises an effective gate length, C_{gs} of TB shows more than 20% compared with PD SOI nMOSFETs with TDBC structure under both the two temperatures as shown in Fig. 8. The result may indicate that the n^+/p^+ junction in TDBC structure does not increase the capacitance.

The cut-off frequency (f_T) and the maximum oscillation frequency (f_{MAX}) are important figures of merit to quantify the RF performance of a transistor.[10] The f_T is the frequency when the drain current gain equals to one, and f_{MAX} is the frequency when the power gain is unity. The physics background of f_T and f_{MAX} can be expressed as follows:[11]

$$f_T = \frac{f_c}{\left(1+\frac{C_{gd}}{C_{ds}}\right)+(R_s+R_d)\left[\frac{C_{gd}}{C_{ds}}(g_m+g_{ds})+g_{ds}\right]}, \tag{6}$$

$$f_{MAX} = \frac{f_c}{2\left(1+\frac{C_{gd}}{C_{ds}}\right)\sqrt{g_d(R_g+R_s)+\frac{1}{2}\frac{C_{gd}}{C_{gs}}\left(R_s g_m+\frac{C_{gd}}{C_{ds}}\right)}}. \tag{7}$$

Here, f_T and f_{MAX} can be extracted by $|H_{21}|f$ and $\sqrt{\text{MUG}}f$, where f is the operating frequency, $|H_{21}|$ is the current gain, and MUG is the Manson's unilateral power gain,[12] MUG could be extracted by the following equation:

$$\text{MUG} = \frac{|H_{21}+H_{12}|^2}{4[\text{Re}(H_{11})\text{Re}(H_{22})+\text{Im}(H_{21})\text{Im}(H_{12})]}. \tag{8}$$

Due to lower parasitic resistances and capacitances, the device with TDBC structure represents 15% improvement in

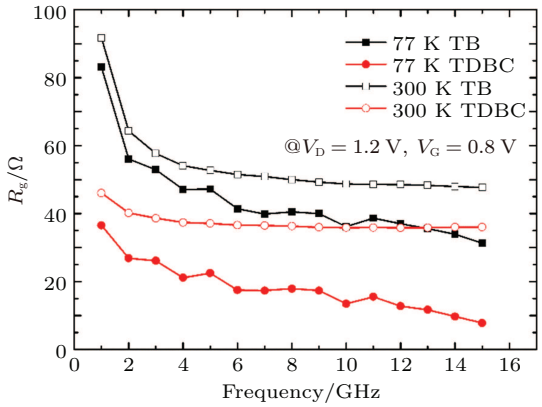


Fig. 7. (color online) Gate resistance R_g as a function of frequency at 300 K and 77 K for TB and TDBC devices, respectively.

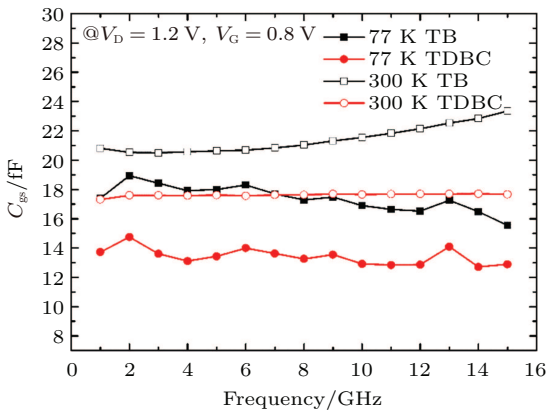


Fig. 8. (color online) Gate-to-source capacitance (C_{gs}) as a function of frequency at 300 K and 77 K, respectively.

f_{MAX} and 8% improvement in f_T compared with TB devices at 77 K respectively, as shown in Figs. 9 and 10. Due to the increase in G_m and the mobility at low temperature, the extracted f_T shows a rising trend with the decrease of temperature and TDBC device presents more improvement at low temperature compared with a TB device. The results mentioned above clearly show that the TDBC SOI nMOSFET is more attractive than the TB SOI nMOSFET for high-frequency applications over a wide range of temperatures. However, unlike the behavior of f_T at low temperature, f_{MAX} of TB and TDBC shows significant degradation when the devices operate at 77 K.

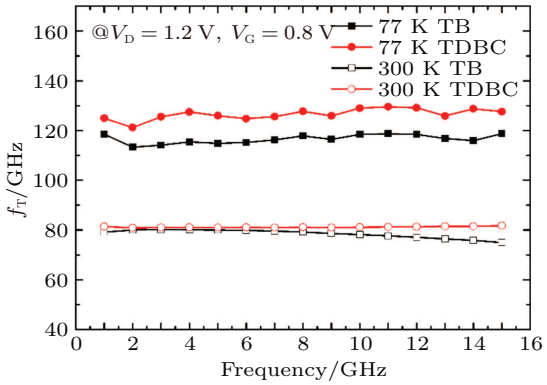


Fig. 9. (color online) The f_T as a function of frequency at 300 K and 77 K, respectively.

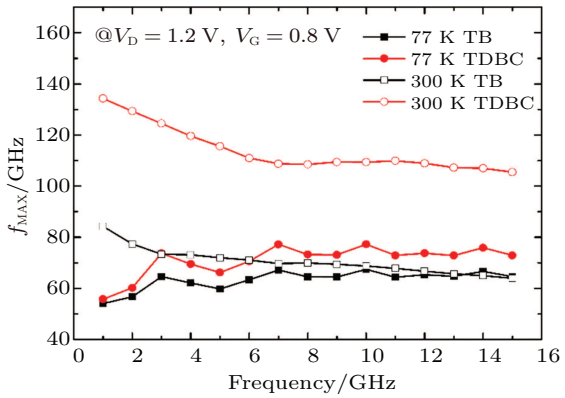


Fig. 10. (color online) The f_{MAX} as a function of frequency at 300 K and 77 K, respectively.

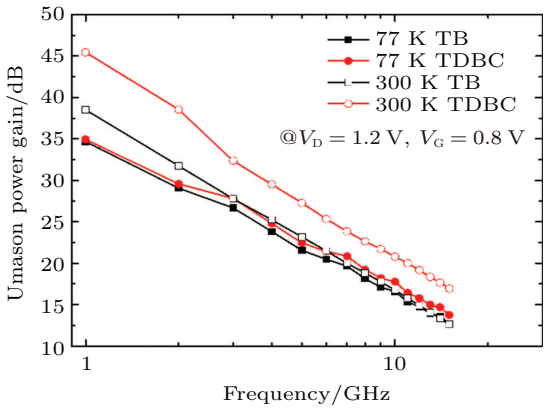


Fig. 11. (color online) Manson's unilateral power gain as a function of frequency at 300 K and 77 K for TB and TDBC devices at $V_D = 1.2$ V, $V_G = 0.8$ V, respectively.

As Eq. (7) shows, the most possible reasons for this degradation are G_{ds} and C_{gd}. For the TB device, MUG almost keeps the same value when the device operates at different temperatures. However, the MUG of TDBC decreases $\sim$ 15% compared with that at 300 K when the device operates at 77 K as shown in Fig. 11.

4. Conclusion

The RF performances of multi-finger PD SOI nMOSFETs with TDBC structure and conventional TB structure at 77 K and 300 K are compared in this paper. By using a simple small signal equivalent circuit model, the extracted small signal parameters of two types of devices are discussed to evaluate the influence on RF performance. The cut-off frequencies (f_T) of TB and TDBC devices show $\sim$50% and $\sim$60% improvement compared with those at 300 K. The improvement in f_T happens because of the improvement in trans-conductance and the decrease of gate capacitance. By contrast with the behavior of f_T, maximum oscillation frequency (f_{MAX}) decreases as the temperature decreases. For TB and TDBC devices, the most possible reason for this degradation is resulting from the increase of G_{ds} and C_{gd}, while the TDBC shows more significant degradation does than TB. However, the degradation in f_{MAX}, TDBC still shows $\sim$15% improvement than TB. The significant high-frequency characteristics of TDBC device under both the two temperatures indicate that the TDBC SOI MOSFETs are a good candidate for the analog and RF application over a wide range of temperatures. Moreover, based on the measured data, the significant high-frequency performance at 77 K indicates that there is immense potential for the development for cryogenic applications.

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