Equivalent distributed capacitance model of oxide traps on frequency dispersion of C–V curve for MOS capacitors*

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An equivalent distributed capacitance model is established by considering only the gate oxide-trap capacitance to explain the frequency dispersion in the C–V curve of MOS capacitors measured for a frequency range from 1 kHz to 1 MHz. The proposed model is based on the Fermi–Dirac statistics and the charging/discharging effects of the oxide traps induced by a small ac signal. The validity of the proposed model is confirmed by the good agreement between the simulated results and experimental data. Simulations indicate that the capacitance dispersion of an MOS capacitor under accumulation and near flatband is mainly caused by traps adjacent to the oxide/semiconductor interface, with negligible effects from the traps far from the interface, and the relevant distance from the interface at which the traps can still contribute to the gate capacitance is also discussed. In addition, by excluding the negligible effect of oxide-trap conductance, the model avoids the use of imaginary numbers and complex calculations, and thus is simple and intuitive.

Keywords: MOS capacitor, C–V curve, frequency dispersion, oxide–trap capacitance

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1. Introduction

Recently, III–V compound semiconductors, especially InGaAs, have been recognized as one of the leading candidates to replace silicon for digital CMOS applications, because of their higher carrier mobility.[1–3] However, as the MOSFET dimensions are continually scaled down, high-k materials, e.g., Al_2O_3,[4] HfO_2,[5] La_2O_3,[6] and ZrO_2,[7] are employed to replace SiO_2 as a gate dielectric because their larger k values allow for the use of a thicker gate dielectric for suppressing the gate leakage current. However, the high-k gate dielectrics often have more traps, which result in serious frequency dispersion of the capacitance–voltage (C–V) curve, especially in the accumulation region.[8–12] The conventional interface-state theory cannot explain this phenomenon because the time constant of the interface states is too small for typical measurement frequencies (1 kHz to 1 MHz) to make the interface states respond to the applied voltage.[13,14] Therefore, many relevant models have focused on the traps in the gate oxide, which have large time constant, and thus can interact with the electrons in the conduction band of the semiconductor via a tunneling mechanism.[15–19] These frequency-dispersion models based on oxide traps include the lumped RC circuit model,[16,17] the distributive-transconductance model,[18] and the distributed circuit model,[19] which involves both the capacitance and conductance effects of the oxide traps. It is believed that the traps in the gate dielectric can capture and emit charges to produce capacitance and conductance. Although it has been pointed out that errors probably exist in the distributive-transconductance model,[20] it could still prove that the oxide traps can result in frequency dispersion in the C–V and G–V curves. In addition, some researchers regarded the traps in the oxide as near-interface traps,[21,22] and the relevant models were established based on the traditional interface-state theory and by considering only the capacitance effect of the near-interface states and interface states. These models could well be used to simulate the dispersion effect in the depletion region of the C–V curve for 1 kHz to 1 MHz, and extract the interface-state and near-interface-state densities by measuring the gate capacitance at different temperatures, but the dispersion effect in the accumulation region cannot be successfully accounted for. Therefore, in this work, an equivalent distributed capacitance model considering only the capacitance effect of the oxide traps in the MOS devices, e.g., Al_2O_3/InGaAs MOS devices, is developed to explain the frequency dispersion of C–V curve, especially in the accumulation region, for the frequency range from 1 kHz to 1 MHz. The proposed model is made simple and intuitive by excluding the conductance effect of the oxide traps. This approximation is confirmed to be reasonable by the good agreement between simulated results and experimental data, demonstrating

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that the oxide traps are the major origin to cause the frequency dispersion in the *C*–*V* curve.

2. Model

Under equilibrium, the probability that an oxide trap in an MOS device is occupied by an electron obeys the Fermi–Dirac statistics[20]

$$f^0(E_t) = \frac{1}{1+\exp[(E_t - E_f)/kT]}, \tag{1}$$

where E_t is the trap level, E_f is the Fermi level, k is the Boltzmann's constant, and T is the absolute temperature. When the gate voltage is changed, the location of E_t will move relative to that of E_f. As a result, the probability that a trap is occupied is changed, and thus the total trapped charge in the oxide is changed. For the traps at x (distance from the interface), the total charge trapped in the oxide traps can be calculated as

$$Q_{bt} = q\int N_{bt} f(E_t)\,\mathrm{d}E_t, \tag{2}$$

where N_{bt} is the density of the oxide traps in units of $\mathrm{cm}^{-3}\cdot\mathrm{eV}^{-1}$ and is assumed to be independent of the distance and energy.

When a small ac signal of $\delta V_g = V\mathrm{e}^{\mathrm{i}\omega t}$ is applied to the gate electrode, the trap-level occupation probability becomes[21]

$$f = f^0 + \delta f, \tag{3}$$

where δf is the deviation from equilibrium

$$\delta f = \frac{q}{kT}\frac{f^0(1-f^0)}{1+\mathrm{i}\omega\tau}\delta\varphi. \tag{4}$$

Here, ω is the angular frequency of the ac small signal, τ is time constant of a trap, and $\delta\varphi$ is the energy variation of E_t due to δV_g. In the oxide, τ is associated with the charge exchange between the oxide traps and semiconductor by the tunneling mechanism, and is also a function of x[15,16]

$$\tau(x) = \tau_0\mathrm{e}^{2\kappa x}, \tag{5}$$

where τ_0 is the time constant of the interface states and κ is the attenuation coefficient for the decay of electron wave-function with energy E under an energy barrier of $E_C^{OX} > E$

$$\kappa = \sqrt{2m^*(E_C^{OX} - E)}/\hbar, \tag{6}$$

where m^* is the effective electron mass in the oxide, E_C^{OX} is the conduction-band bottom of the oxide, and $\hbar$ is the reduced Planck's constant.

Thus, the Q_{bt} variation induced by δV_g can be expressed as

$$\delta Q_{bt}(\omega) = -q\int_{-\infty}^{+\infty} N_{bt}\delta f(E_t,\omega)\,\mathrm{d}E_t, \tag{7}$$

which induces an oxide-trap capacitance

$$\tilde{C}_{bt}(\omega) = \frac{-\delta Q_{bt}(\omega)}{\delta\varphi_s}, \tag{8}$$

where $\tilde{C}_{bt}$ is a complex number and its real part can be written as

$$C_{bt} = \frac{q^2}{kT}\int_{-\infty}^{+\infty} N_{bt}\frac{f^0(1-f^0)}{1+\omega^2\tau^2}\,\mathrm{d}E_t. \tag{9}$$

Since the term $f^0(1-f^0)$ is sharply peaked at $E = E_f$, κ is set to be a constant when $E = E_f$ in the integration.[23] So integrating Eq. (9) gives

$$C_{bt} = \frac{q^2 N_{bt}}{1+\omega^2\tau_0^2\mathrm{e}^{4\kappa x}}. \tag{10}$$

For a given gate dc bias, the oxide traps with distance x and energy E_t can change occupancy in response to a small ac signal modulation,[24] with the highest occupation probability when $E_t = E_f$ by exchanging charge with the conduction band of the semiconductor via tunneling.[24] So it is reasonably suggested that the small-signal capacitance is produced mainly by those traps at $E_t = E_f$ (κ is a constant in the integration).

The proposed model is an equivalent distributed capacitance model, as shown in Fig. 1, in which $C(x)$ is the total equivalent capacitance from the oxide/semiconductor interface to x. The oxide is divided into many small equal parts and only the capacitance of the oxide traps is taken into consideration. The small oxide-trap capacitance for the small part at x can be expressed as

$$\Delta C_{bt}(x) = \frac{q^2 N_{bt}\Delta x}{1+\omega^2\tau_0^2\mathrm{e}^{4\kappa x}}. \tag{11}$$

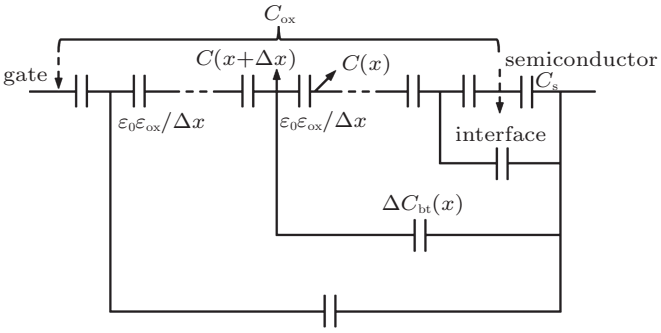


Fig. 1. Equivalent circuit for the traps in the oxide. $C(x)$ is the total capacitance at x, C_s is the semiconductor capacitance, $\varepsilon_0\varepsilon_{ox}/\Delta x$ is the oxide capacitance in Δx, and C_{ox} is the oxide capacitance of the MOS capacitor.

As shown in Fig. 1, the total equivalent capacitance $C(x+\Delta x)$ at $x+\Delta x$ includes three parts: $\Delta C_{bt}(x)$, $C(x)$, and $\varepsilon_0\varepsilon_{ox}/\Delta x$. Therefore, $C(x+\Delta x)$ can be expressed as

$$C(x+\Delta x) = \frac{1}{\Delta x/\varepsilon_0\varepsilon_{ox} + 1/C(x)} + \frac{q^2 N_{bt}\Delta x}{1+\omega^2\tau_0^2\mathrm{e}^{4\kappa x}}. \tag{12}$$

Subtracting $C(x)$ and dividing by Δx on both sides of Eq. (12) results in a differential equation for $C(x)$

$$\frac{\mathrm{d}C(x)}{\mathrm{d}x} = -\frac{C^2(x)}{\varepsilon_0\varepsilon_{ox}} + \frac{q^2 N_{bt}}{1+\omega^2\tau_0^2\mathrm{e}^{4\kappa x}}, \tag{13}$$

with the boundary condition $C(x=0)=C_s$ which is the semiconductor capacitance. By using an iterative method, the differential equation can be numerically solved to obtain the total capacitance $C(x=t_{ox})$ of the MOS structure with an oxide thickness of t_{ox}. If N_{bt} is assumed to be a constant, then the differential equation can be transformed into a hyper-geometric differential equation and can be solved analytically by using the Gaussian hyper-geometric function.[24,25]

3. Results and discussion

3.1. Comparison between simulated results and experimental data

In the following simulations, InGaAs MOS devices are considered and simulated results are shown in Figs. 2–4. The experimental data in Fig. 2 come from Refs. [23] and [24], where a Pt/5-nm Al_2O_3/n-InGaAs MOS device was fabricated with a channel concentration of 2×10^{16} cm^{-3} and $C_{ox}=1.06$ μF/cm^2, and the distributed circuit model was used to explain the capacitance and conductance dispersions of the device. The experimental data are obtained with the gate biased at 2.9 V and 0.3 V, and are represented by open circles and squares, respectively, in Fig. 2. When the MOS device is biased at 2.9 V under accumulation, κ is calculated to be 5.0 nm^{-1} for $E_C^{OX}-E=1.91$ eV and $m^*=0.5m_0$ (m_0 is free-electron mass) in Ref. [24], and a single-level trap density $N_{bt}=4.5\times10^{19}$ cm^{-3}·eV^{-1}, $C_s=2.8$ μF/cm^2, and $\tau_0=2.8\times10^{-10}$ s are chosen by fitting to the experimental data, as listed in Table 1. The simulated results are compared with the experimental data and good agreement between them is demonstrated, as shown in Fig. 2. When the MOS device is biased at 0.3 V near the flatband region, the relevant parameters are $N_{bt}=2.2\times10^{19}$ cm^{-3}·eV^{-1}, $C_s=0.635$ μF/cm^2, $\kappa=5.47$ nm^{-1}, and $\tau_0=5\times10^{-8}$ s, as also shown in Table 1. It should be noted that in the simulation of Fig. 2, the same parameter values of N_{bt}, C_s, and κ as those in Refs. [23] and [24] are used.

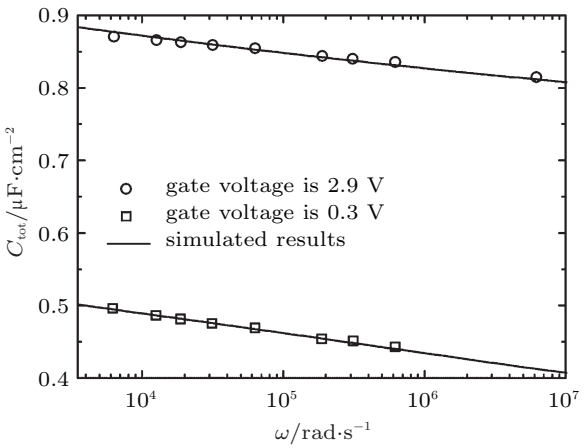


Fig. 2. Comparison between simulated results (solid line) and experimental data (symbols) for a Pt/5-nm Al_2O_3/n-InGaAs MOS device with the gate biased at 2.9 V (open circles) and 0.3 V (open squares).

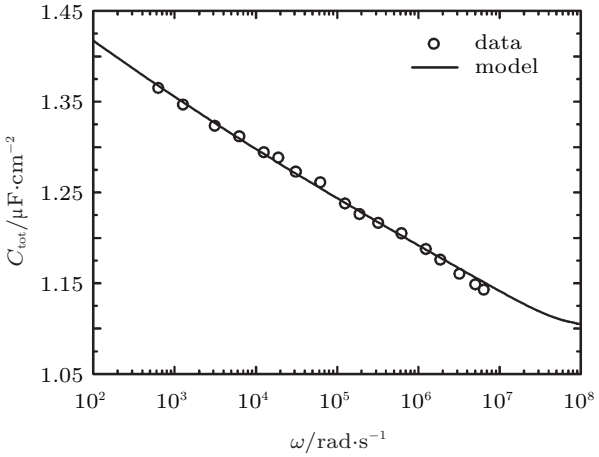


Fig. 3. Comparison between simulated results (solid line) and experimental data (open circles) for a Pd/4.5-nm Al_2O_3/p-InGaAs MOS device with the gate biased at −1.8 V.

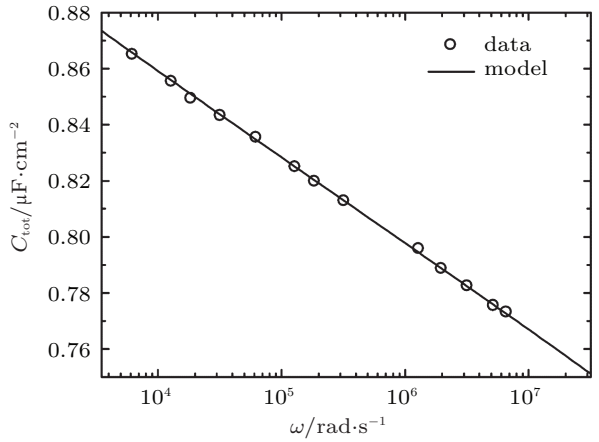


Fig. 4. Comparison between simulated results (solid line) and experimental data (open circles) for a 7-nm Al_2O_3/n-InGaAs MOS device biased in the accumulation region.

Table 1. The parameters used in simulation for different gate biases corresponding to Figs. 2–4.

Figure	Voltage /V	N_{bt} /cm^{-3}·eV^{-1}	C_s /μF·cm^{-2}	κ /nm^{-1}	τ /s
2	2.9	4.5×10^{19}	2.8	5.0	2.8×10^{-10}
2	0.3	2.2×10^{19}	0.64	5.5	5.0×10^{-8}
3	−1.8	4.1×10^{20}	5.5	6.0	1.7×10^{-8}
4	unknown	1.3×10^{20}	2.3	5.1	1.0×10^{-10}

The experimental data in Fig. 3 are from Ref. [19], where a Pd/4.5-nm Al_2O_3/p-InGaAs MOS device was fabricated with a channel concentration of 1×10^{17} cm^{-3}. The gate voltage applied to the device is −1.8 V to render it under accumulation. The dielectric constant of the oxide is 7; hence, the value of C_{ox} is 1.3 μF/cm^2. Other parameters for simulation are $N_{bt}=4.1\times10^{20}$ cm^{-3}·eV^{-1}, $C_s=5.5$ μF/cm^2, $\kappa=6$ nm^{-1}, and $\tau_0=1.7\times10^{-8}$ s. All of the parameters are the same as those in Ref. [19], except for N_{bt}, which is a fitting parameter in the proposed model and in the same order of magnitude as that in Ref. [19]. Usually, the Al_2O_3/p-InGaAs MOS

device has more severe oxide-trap frequency dispersion in accumulation than the Al_2O_3/n-InGaAs MOS device, implying that for the oxide, there are more hole traps in the valence band than electron traps in the conduction band.[19]

The experimental data in Fig. 4 are also from Ref. [19], where a 7-nm Al_2O_3/n-InGaAs MOS device was fabricated with a dielectric constant of 7.4 for the oxide. In this case, the MOS device is biased in accumulation but the exact gate voltage is not known. By fitting to the experimental data, the other parameters used in the simulation are $N_{bt} = 1.27\times10^{20}$ cm^{-3}·eV^{-1}, $C_s = 2.3$ μF/cm^2, $\kappa = 5.1$ nm^{-1}, and $\tau_0 = 1.0\times10^{-10}$ s, which are very close or equal to those in Ref. [19]. As shown in Fig. 4, the simulated results are also in good agreement with the experimental data.

As can be seen from Figs. 2–4, all of the simulated results can match well with the experiment data, regardless of the type of semiconductor or gate bias voltage, thus confirming the validity of the proposed model. Therefore, it can be suggested that the proposed model is sufficiently accurate to describe the source of the frequency dispersion in the *C*–*V* curve, especially in the accumulation region.

Figure 5 shows the numerical solution to Eq. (13). It suggests that the capacitance of the MOS device varies with ω, but when ω is small or large enough, the total capacitance is a constant: when ω is large enough to reach the high-frequency limit of $\omega\tau_0 \geq 1$, no oxide traps can respond to the ac signal;[23,24] when ω is small enough, equation (13) becomes independent of ω and all of the oxide traps can respond to the ac signal, making the total capacitance independent of ω. The results are consistent with the simulation results of the distributed circuit model,[19] as shown in Fig. 5.

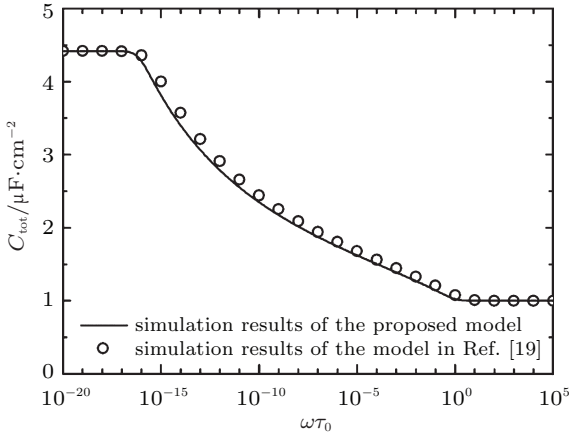


Fig. 5. Comparison between the proposed model (Eq. (13)) and the distributed circuit model in Ref. [19]. The parameters used are $N_{bt} = 2\times10^{20}$ cm^{-3}·eV^{-1}, $C_{ox} = C_s = 2$ μF/cm^2, $t_{ox} = 4.5$ nm, $\kappa = 6$ nm^{-1}, and $\tau_0 = 1\times10^{-7}$ s.

It is worth pointing out that the effect of the parasitic resistance in series with the MOS capacitor is not considered in the model because it plays no role when the measurement frequency is only a few kilohertz.[24] However, dispersion is still observed in the measurement, indicating that the dispersion is indeed mainly from the capacitance effect of the oxide traps rather than the parasitic resistance.

Also, the capacitance from the interface states (C_{it}) can be expressed as

$$C_{it} = \frac{q^2 N_{it}}{1+\omega^2\tau_0^2}, \tag{14}$$

where N_{it} is the density of the interface states in units of cm^{-2}·eV^{-1}. Owing to the fact that the interface states are located at the oxide/semiconductor interface, C_{it} will be incorporated into the equivalent distributed capacitance model presented in Fig. 1 in parallel with C_s, and so C_s can be replaced by $(C_s + C_{it})$. Figure 6(a) shows the relation between C_{it} and ω (in a range of 1 krad/s to 10 Mrad/s) with $N_{it} = 5\times10^{12}$ cm^{-2}·eV^{-1} and different τ_0. As can be seen, when τ_0 is very small (1×10^{-10} to 1×10^{-8} s, from accumulation to flatband), C_{it} will almost not vary with ω, i.e., C_{it} does

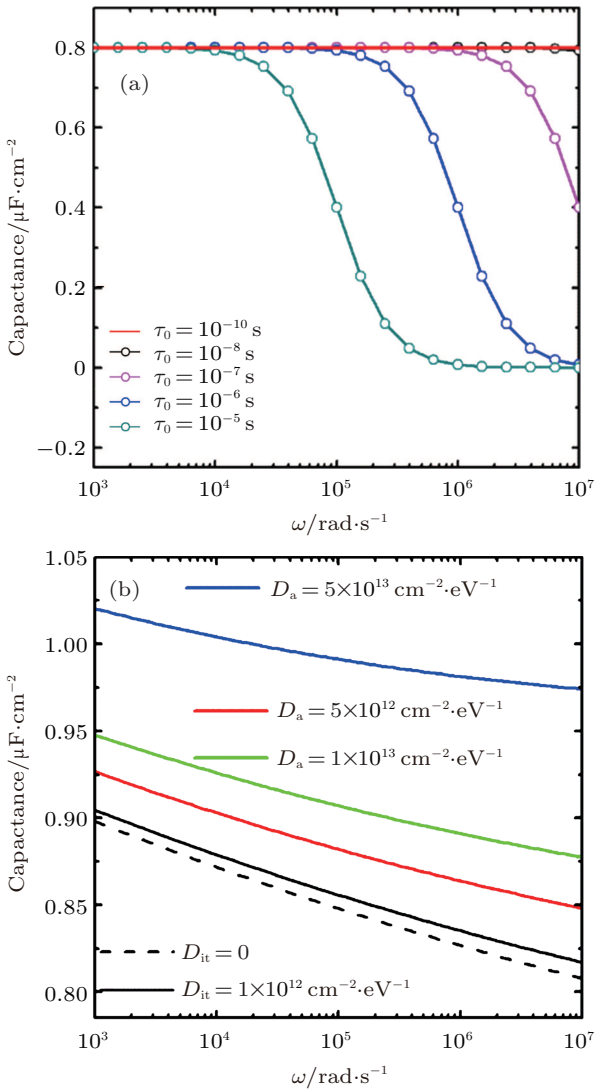


Fig. 6. (color online) Relationship between C_{it} and ω with $N_{it} = 5\times10^{12}$ cm^{-2}·eV^{-1} and different τ_0 (a) and effect of the interface-state density on the total gate capacitance (b).

not contribute to the frequency dispersion of the total gate capacitance in the accumulation region or near the flatband and the effect of the interface states on the total gate capacitance is simply to increase the value of C_s (from C_s to $C_s + C_{it}$). However, as τ_0 increases to 1×10^{-7} s or 1×10^{-5} s and the device is probably biased at depletion, C_{it} will vary with ω, thus causing the frequency dispersion of the total gate capacitance. On the other hand, the effect of the interface-state density on the frequency dispersion of the capacitance can be discussed by incorporating the capacitance of the interface states into the model presented in Fig. 1, and the simulated results are shown in Fig. 6(b), where the same parameters as those in Fig. 2 are used in the simulation with the gate biased at 2.9 V in accumulation. It can be found that the total gate capacitance will increase by C_{it}, which is equivalent to increasing the value of C_s to $C_s + C_{it}$.

3.2. Effects of oxide-trap location on dispersion

As expressed in Eq. (5), the time constant of the oxide trap varies with its location. As the distance x increases, the time constant increases. Usually, if $\omega\tau(x) >\sim 1$ [$\tau(x) = \tau_0 e^{2\kappa x}$], the capacitance of the traps becomes very small. Obviously, with decreasing frequency, the location at which the oxide traps can still contribute to the total capacitance becomes farther from the oxide/semiconductor interface. Figure 7 shows the relationship between the trap distance from the interface and the interface-state time constant τ_0 under the condition of $\omega\tau(x) = 1$. It can be seen that the maximum distance, at which the oxide trap can still contribute to the total capacitance, decreases as κ, ω, or τ_0 increases. Typically, the values of κ and τ_0 will decrease when the gate is biased from depletion to accumulation, and thus from Fig. 7 it can be seen that in the accumulation region (κ and τ_0 have lower values), the maximum distance will have a larger value; however, this maximum distance is still much smaller than the oxide thickness used above (e.g., 5 nm in Fig. 2, 4.5 nm in Fig. 3, and 7 nm in Fig. 4).

Figure 8 shows the simulated results considering that only a portion of the oxide adjacent to the interface (the relevant thickness is denoted as t_d) has defects and the remaining portion is ideal. It can be seen that as t_d decreases, the difference between the simulation results and experimental data becomes larger, especially at low frequencies. On the contrary, as t_d increases to exceed a certain value e.g., 1.8 nm in Fig. 8(a), the simulated total capacitance hardly changes within the given frequency range, implying that the contribution of those traps beyond 1.8 nm to the total capacitance is negligible.

Figure 9 shows the change of $1/(1+\omega^2\tau_0^2 e^{4\kappa x})$ with the distance (x) from the interface, reflecting the size of the oxide-trap capacitance effect at x in the oxide. For given ω, τ_0, and κ, as x increases, the oxide-trap capacitance almost remains constant initially, but then decreases rapidly when x exceeds a certain value, e.g., 1.0 nm under the condition of $\kappa = 5$ nm^{-1}, $\omega = 1$ Mrad/s, $\tau_0 = 1 \times 10^{-8}$ s, or 1.5 nm under the condition of $\kappa = 5$ nm^{-1}, $\omega = 1$ krad/s, $\tau_0 = 1 \times 10^{-10}$ s. Further simulations indicate that for $N_{bt} = 4.5 \times 10^{19}$ cm^{-3}·eV^{-1} (equal to that biased at 2.9 V in Fig. 2), when the value of $1/(1+\omega^2\tau_0^2 e^{4\kappa x})$ is smaller than 1×10^{-4} (as shown by the horizontal line in Fig. 9), the capacitance effect of the oxide traps can be neglected, and thus the relevant x value can be achieved, e.g., 1.04 nm for the condition of $\kappa = 5$ nm^{-1}, $\omega = 1$ Mrad/s, $\tau_0 = 1 \times 10^{-8}$ s; 2.19 nm for the condition of $\kappa = 5$ nm^{-1}, $\omega = 1$ krad/s, $\tau_0 = 1 \times 10^{-10}$ s; and especially 1.85 nm for the gate voltage of 2.9 V in Fig. 2 and Fig. 8(a) under the condition of $\kappa = 5$ nm^{-1}, $\omega = 1 \times 10^{3.5}$ rad/s, $\tau_0 = 2.8 \times 10^{-10}$ s. Therefore, it can be concluded that only those traps near the interface can enhance the frequency dispersion of the capacitance in accumulation and near flatband, and the effects of the traps far from the interface on the capacitance dispersion can be neglected.

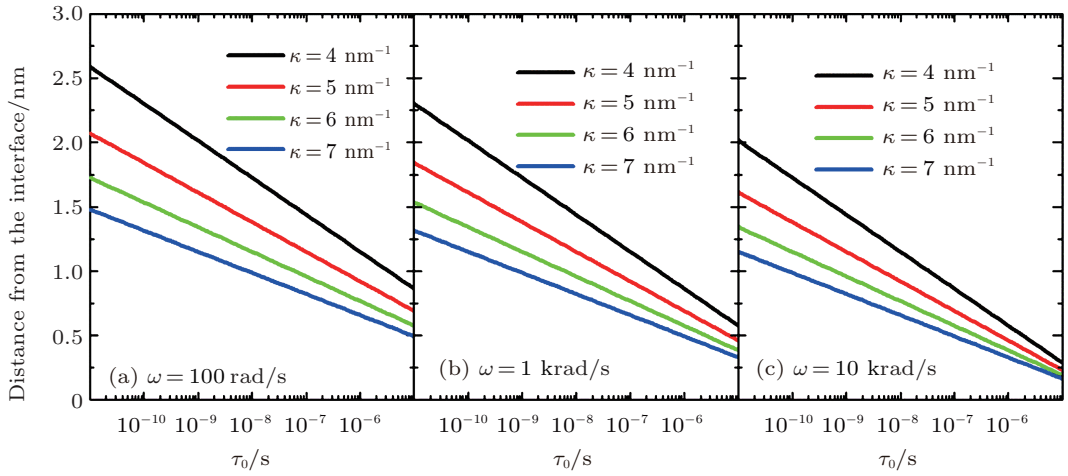


Fig. 7. (color online) Relation between the trap distance from the interface and the interface-state time constant τ_0 with $\omega\tau(x) = 1$.

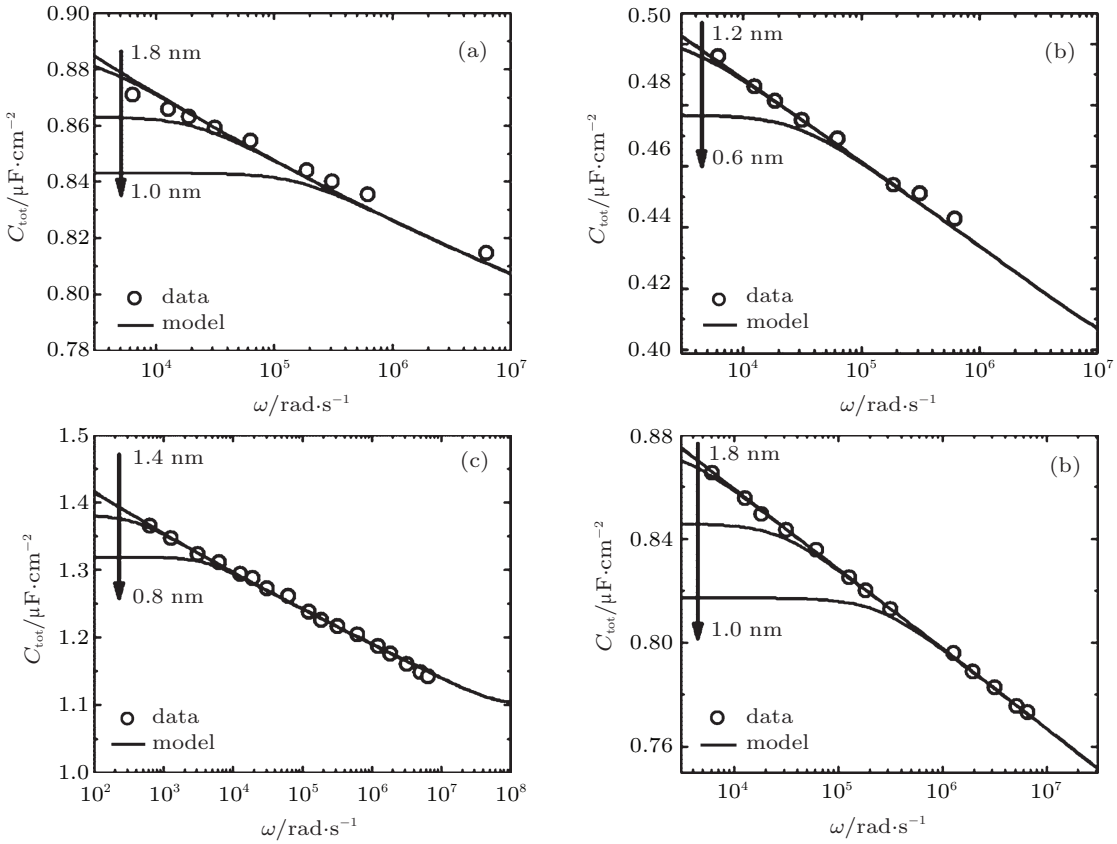


Fig. 8. Variation of capacitance with frequency when considering only a portion of the oxide adjacent to the interface has defects. The values of the parameters used in the simulation and the experimental data in (a)–(d) are equal to those in Figs. 2–4, respectively. Thickness of the oxide with defects adjacent to the interface decreases at a step of 0.2 nm.

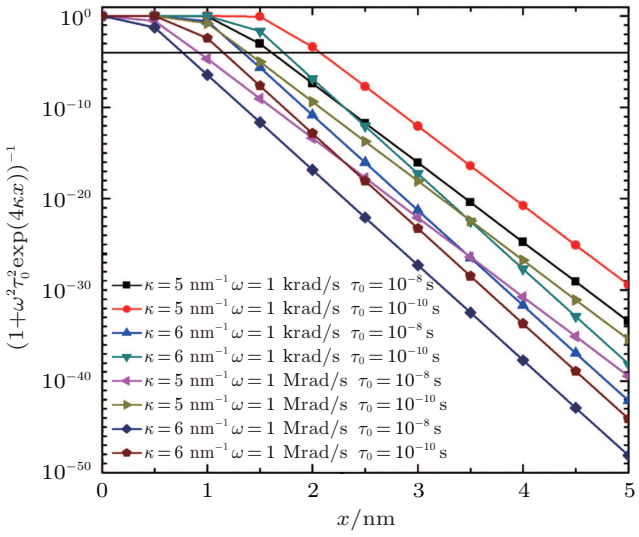


Fig. 9. (color online) Change of $1/(1+\omega^2\tau_0^2\,\mathrm{e}^{4\kappa x})$ with the distance from the oxide/semiconductor interface.

4. Summary

An equivalent distributed capacitance model considering only the oxide-trap capacitance is built to explain the frequency dispersion in the measured capacitance of Al_2O_3/InGaAs MOS capacitors, especially in accumulation and near flatband. The model is based on the Fermi–Dirac statistics and the charging/discharging effects of the oxide traps induced by a small ac signal, and differs from other models based on the interface-state theory. The simulated results are in good agreement with experimental data, confirming the validity of the proposed model. The model can explain the frequency-dispersion phenomenon in the *C*–*V* curve of both n- and p-type devices under different gate biases. In addition, it is fundamentally different from the conventional interface-state models in which the time constant is too small for the oxide traps to respond to ac signals with frequency from 1 kHz to 1 MHz. Moreover, the proposed model is simple and intuitive (owing to its limited consideration of only trap capacitance), and is sufficiently accurate, implying that the conductance effect of the oxide traps has a smaller contribution to the frequency dispersion of the *C*–*V* curve. The simulated results indicate that only those traps adjacent to the oxide/semiconductor interface can enhance the capacitance dispersion of MOS capacitor under accumulation and near flatband, while the effects of the traps far from the interface are negligible.

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